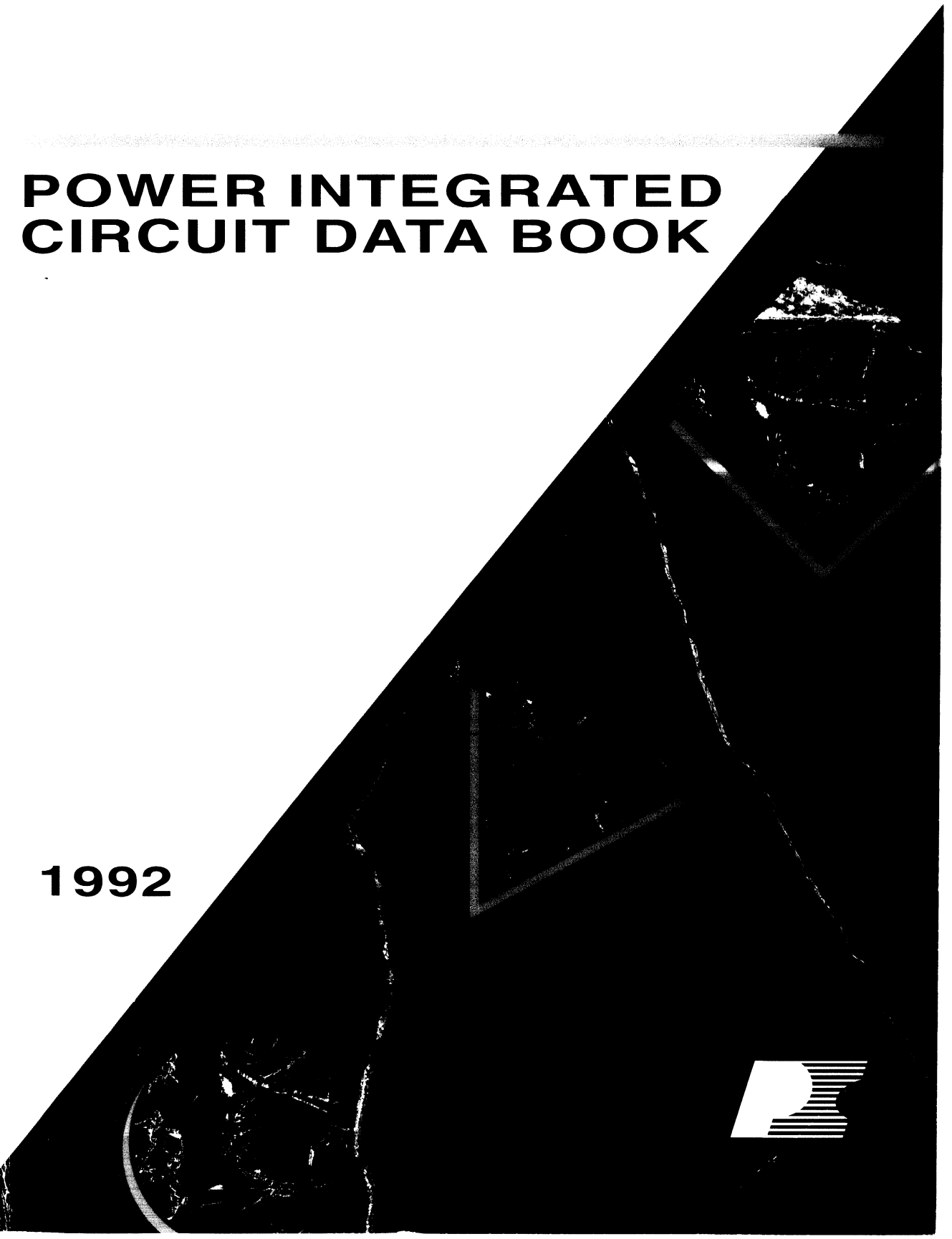
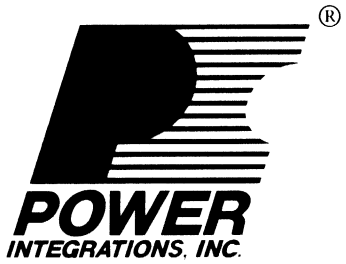
POWER INTEGRATED CIRCUIT DATA BOOK

1992





MAY 1992

POWER

INTEGRATED CIRCUIT

DATA BOOK

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Stresses listed under the Absolute Maximum Ratings section of each data sheet may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein, nor does it convey any license under its patent rights or the rights of others.

Power Integrations, Inc.
Quality Pledge

Our goal is to produce power integrated circuits which cost-effectively combine digital and analog building-blocks with high-voltage power transistors for products required by the commercial/industrial marketplace.

We at Power Integrations, Inc. will be judged by our customers based on our ability to satisfy their needs. Only by diligently pursuing the highest standards of component quality, customer support, and on-time delivery can we succeed in satisfying and maintaining long-term relationships with our customers.

Dr. Edward C. Ross
President and CEO

POWER INTEGRATIONS, INC.
Ordering Information

PWR-XXX #ZZZ##

NOTE: PWR PREFIX WILL NOT BE INCLUDED IN MARKING ON THE FINISHED PRODUCT

PART DESCRIPTOR = ALPHA CHARACTER

EVAL - Product evaluation tools
INT - Interface products
SMP - Switched-mode power supply products

SERIES NUMBER = NUMERICAL CHARACTER

PACKAGE TYPE = ALPHA CHARACTER

PACKAGE	CODE	PACKAGE	CODE
PLASTIC BATWING DIP	B	PLASTIC DIP	P
PLASTIC QFP	E	PLASTIC BATWING SOIC	S
PLASTIC SIP	W	PLASTIC SOIC	T
DICE	X		

LEAD COUNT = ALPHA CHARACTER

PINS	CODE	PINS	CODE
8	F	23	T
16	N	80	Y
20	R		

TEMPERATURE RANGE

C	0 TO 70°C
I	-40 TO 85°C

LEAD BEND,VOLTAGE, OR OTHER PRODUCT OPTIONS
(See data sheet)

TABLE OF CONTENTS

Power Supply IC Products 1

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PWR-SMP3

PWM Power Supply IC

120 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 3 W from 120 VAC input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for 120 VAC off-line applications
- Can also be used with DC inputs from 36 V to 200 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC during start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Inherent current limiting protects from short-circuits
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

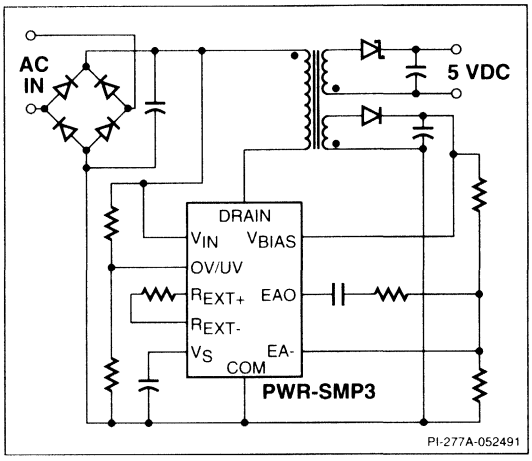


Figure 1. Typical Application

Description

The PWR-SMP3, intended for off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance, and lower gate threshold voltage results in a reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP3 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference voltage, error amplifier, gate driver, undervoltage lockout, over-temperature protection, and current limiting. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies.

The PWR-SMP3 is available in a 16-pin plastic DIP package.

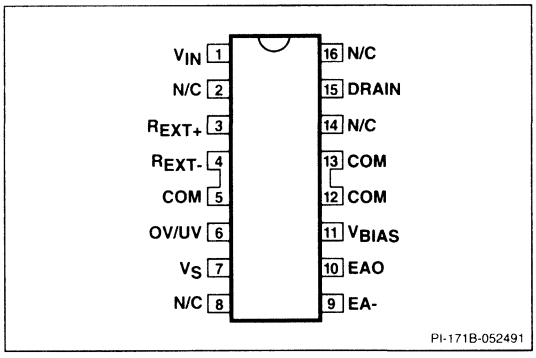


Figure 2. Pin Configuration

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP3BNC	16-pin PWR PDIP	0 to 70°C

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13:
COM connections. Ground or reference point for the circuit.

Pin 6:
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8:
N/C

Pin 9:
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10:
EAO is the error amplifier output for connection to the external compensation network.

Pin 11:
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15:
Open **DRAIN** of the output MOSFET.

Pin 16:
N/C for creepage distance.

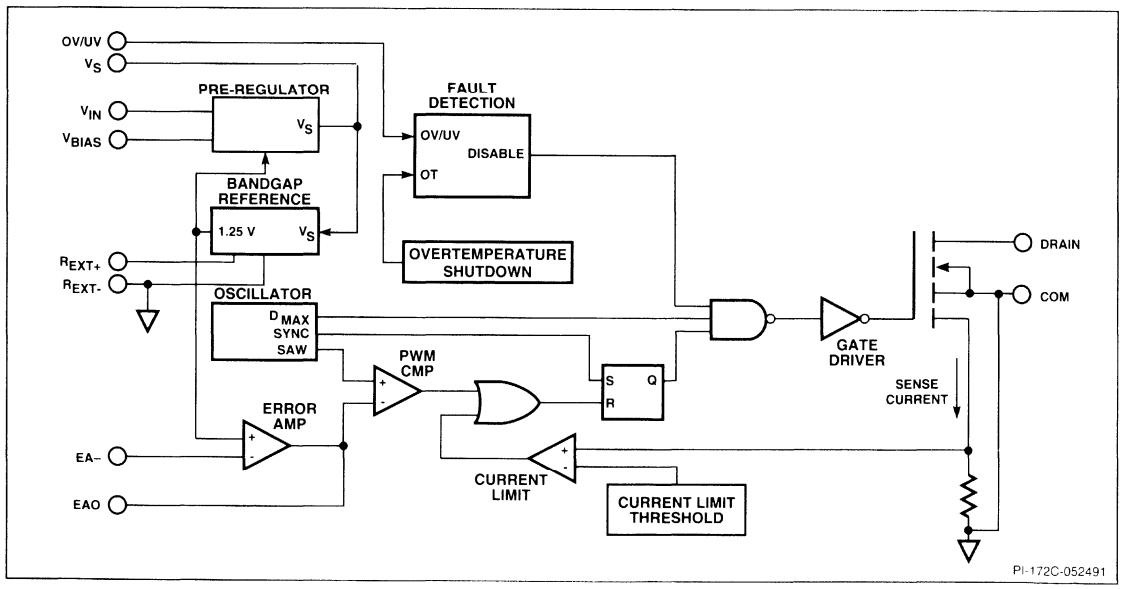


Figure 3. Functional Block Diagram of the PWR-SMP3.

PWR-SMP3 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit connected to V_{BIAS}.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of around 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Current Limit Protection
The current limit sense consists of a current mirror on the power device and a sense resistor. The current mirror produces a current proportional to the drain current of the power switch. A sense voltage is generated by passing the mirror current through a sense resistor. This voltage is then compared to a reference voltage using an internal comparator.

3 W, 110 VAC Input Power Supply with Feedback Winding Regulation

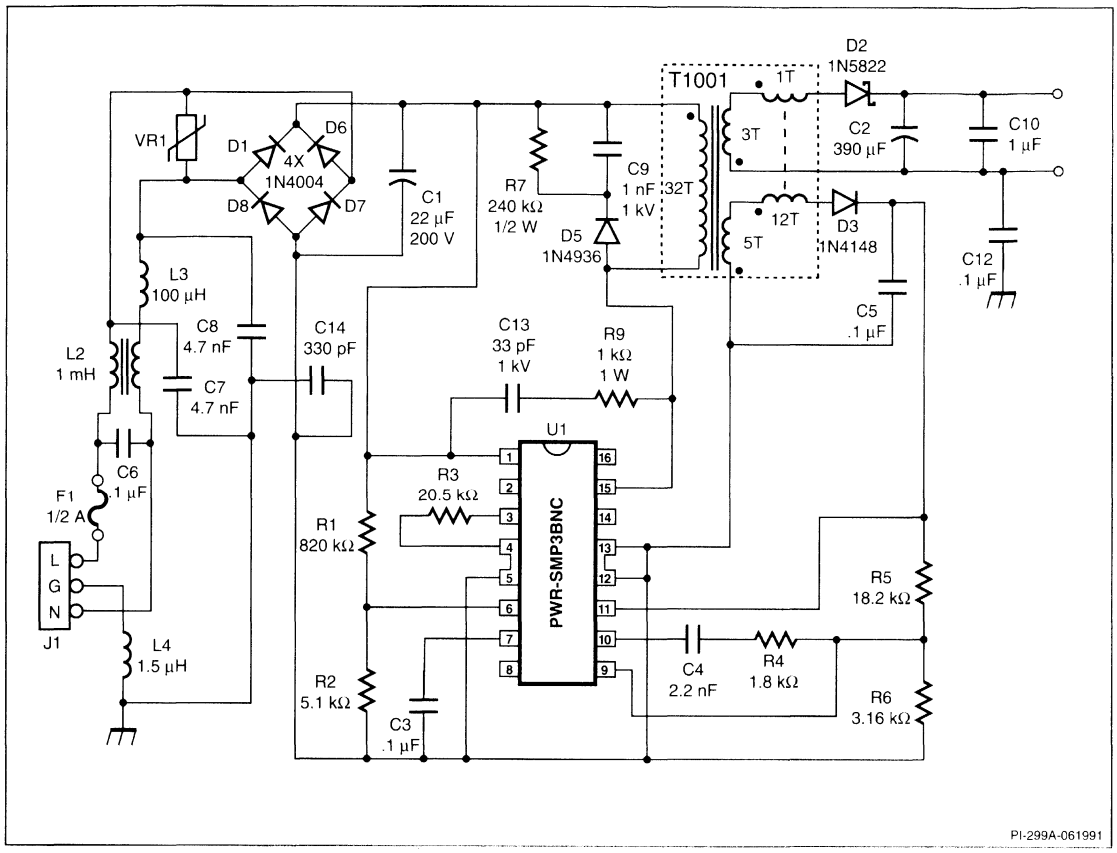


Figure 4. Schematic Diagram of a 3 W Off-line Power Supply Utilizing the PWR-SMP3. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1001 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 140 V(rms) AC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP3 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective turns ratio can be fine-tuned if necessary by the number of junctions in D3. Three elements affect the regulation of the output voltage; maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

L2, L3, L4, C6, C7, C8, C12 and C14 form an EMI filter. D1, D6, D7, D8, and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. D5, C9, and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C13 and R9 damps the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP3. C3 and C5 are bypass capacitors. R1 and R2 form a voltage divider network that sets the input undervoltage and overvoltage lockout trip points.

General Circuit Operation (cont.)

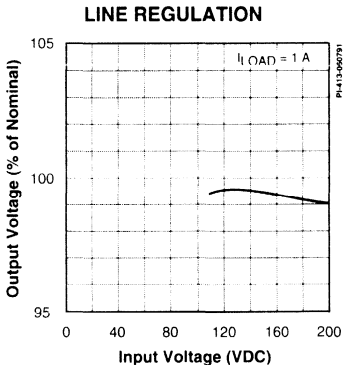
This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

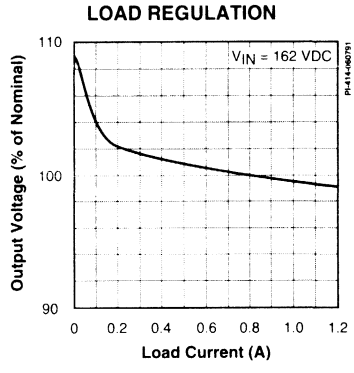
The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL1 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP3. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

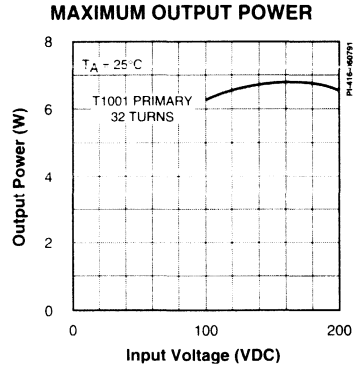
The line and load regulation graphs shown below were measured on a PWR-EVAL1 board operated from a DC source. The switching frequency of the power supply was measured at 950 kHz.

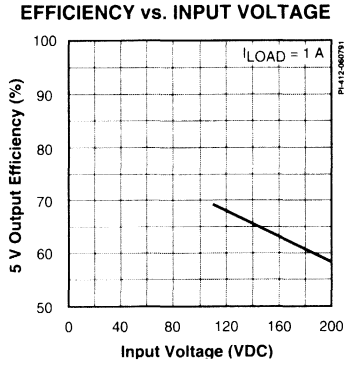
The maximum output power curve shows the power output capability for the standard transformer T1001. See DA-3 for further information on ordering transformers for use with the PWR-SMP3.

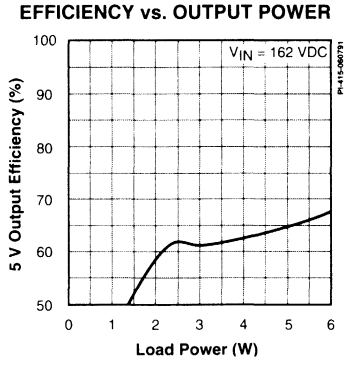
Typical Performance Characteristics (Figure 4 Power Supply)











ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage ..... 350 V
V_{IN} Voltage ..... 350 V
V_{BIAS} Voltage ..... 11 V
Drain Current[2] ..... 700 mA
Input Voltage[3] ..... - 0.3 V to V_S + 0.3 V
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C
Junction Temperature[2] ..... 150°C
Lead Temperature[4] ..... 260°C

Power Dissipation (T_A = 25°C) ..... 2.1 W
(T_A = 70°C) ..... 1.05 W
Thermal Impedance (θ_{JA}) ..... 43°C/W
Thermal Impedance (θ_{JC})[5] ..... 6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}		800	950	1100	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC		0-35	0-39		%
CIRCUIT PROTECTION						
Current Limit Threshold			350	425	500	mA
Input UV Trip-off			0.29	0.34	0.39	V
Input UV Hysteresis			35	50	70	mV
Input OV Trip-off		See Note 1	1.17	1.25	1.33	V
Input OV Hysteresis			40	60	80	mV
OV/UV Turn-off Delay Time	$t_{d(off)}$	See Figure 5		250	500	ns
Thermal Shutdown Temperature			115	135		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		14	16	Ω
			T_j = 115°C		21	25	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		280			mA
OFF-State Current	I_{DSS}	V_{DRAIN} = 280 V, T_A = 115°C			10	25	µA
Breakdown Voltage	BV_{DSS}	I_D = 100 µA, T_A = 25°C		350			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			22		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 200 V			170		nJ
Rise Time	t_R	See Figure 5			33	100	ns
Fall Time	t_F	See Figure 5			8	15	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		350	V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
SUPPLY (cont.)						
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$		6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected		4	5.0	mA
		V_{BIAS} > 8.25 V			0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback	8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback		4	5.0	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP3 is connected to a high voltage power source when the test circuit is activated.

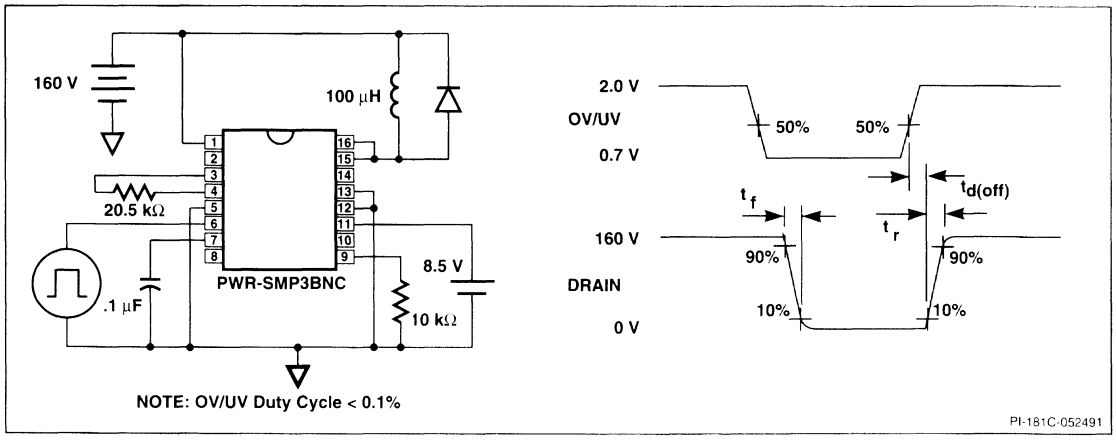
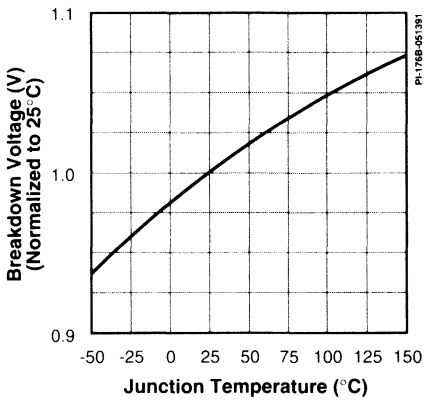
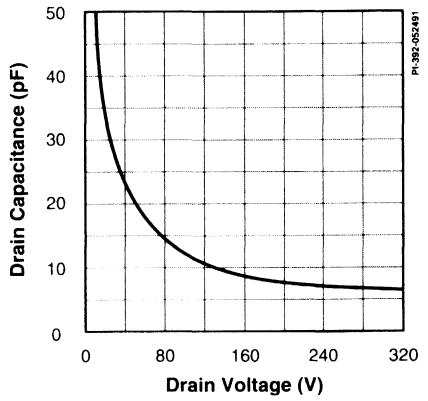


Figure 7. Switching Time Test Circuit

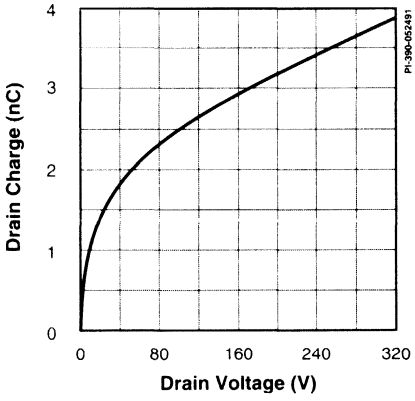
BREAKDOWN vs. TEMPERATURE



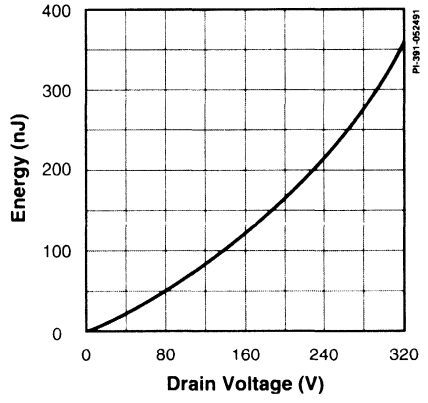
C_{OSS} vs. DRAIN VOLTAGE



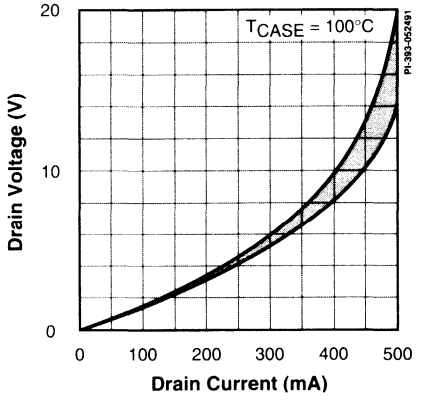
DRAIN CHARGE vs. DRAIN VOLTAGE



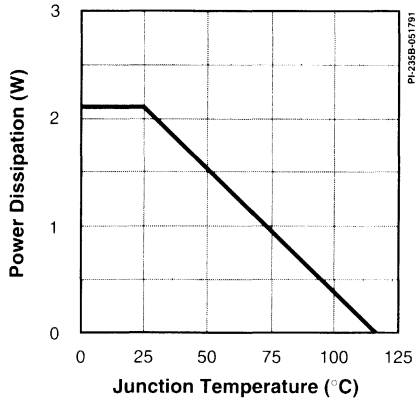
DRAIN CAPACITANCE ENERGY



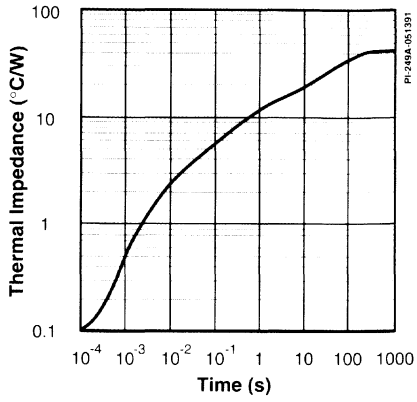
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP110

PWM Power Supply IC

120 VAC Input
Isolated, Regulated DC Output

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from 120 VAC input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for 120 VAC off-line applications
- Can also be used with DC inputs from 36 V to 200 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC during start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

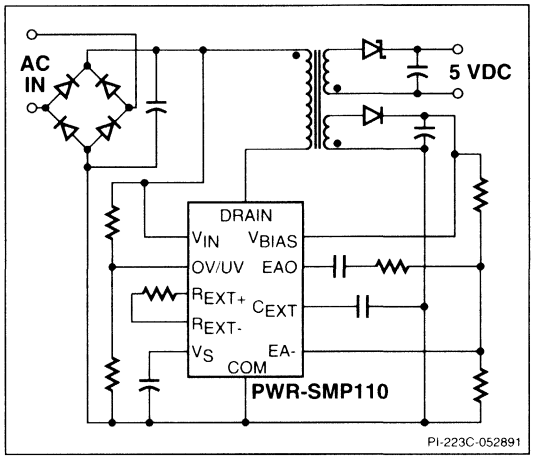


Figure 1. Typical Application

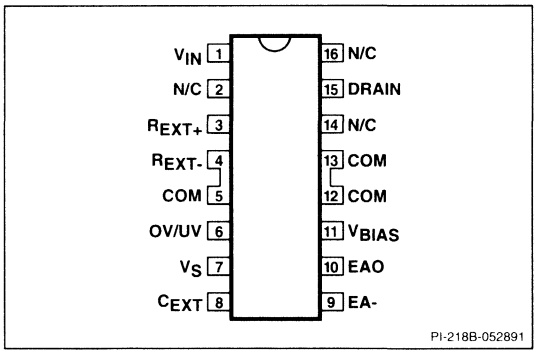


Figure 2. Pin Configuration

Description

The PWR-SMP110, intended for off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance, and lower gate threshold voltage results in a reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP110 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference voltage, error amplifier, gate driver, undervoltage lockout, and over-temperature protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies.

The PWR-SMP110 is available in a 16-pin plastic DIP package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP110BNC	16-pin PWR PDIP	0 to 70°C

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13:
COM connections. Ground or reference point for the circuit.

Pin 6:
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9:
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10:
EAO is the error amplifier output for connection to the external compensation network.

Pin 11:
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15:
Open **DRAIN** of the output MOSFET.

Pin 16:
N/C for creepage distance.

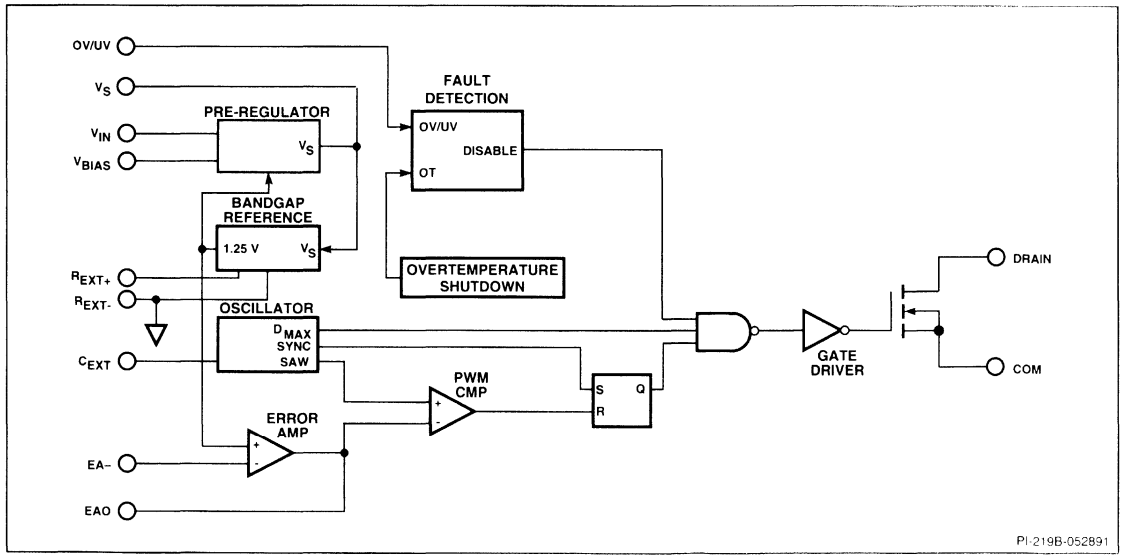


Figure 3. Functional Block Diagram of the PWR-SMP110.

PWR-SMP110 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit connected to V_{BIAS}.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. The oscillator frequency can be lowered by adding additional capacitance at the C_{EXT} pin.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of about 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

10 W, 110 VAC Input Power Supply with Feedback Winding Regulation

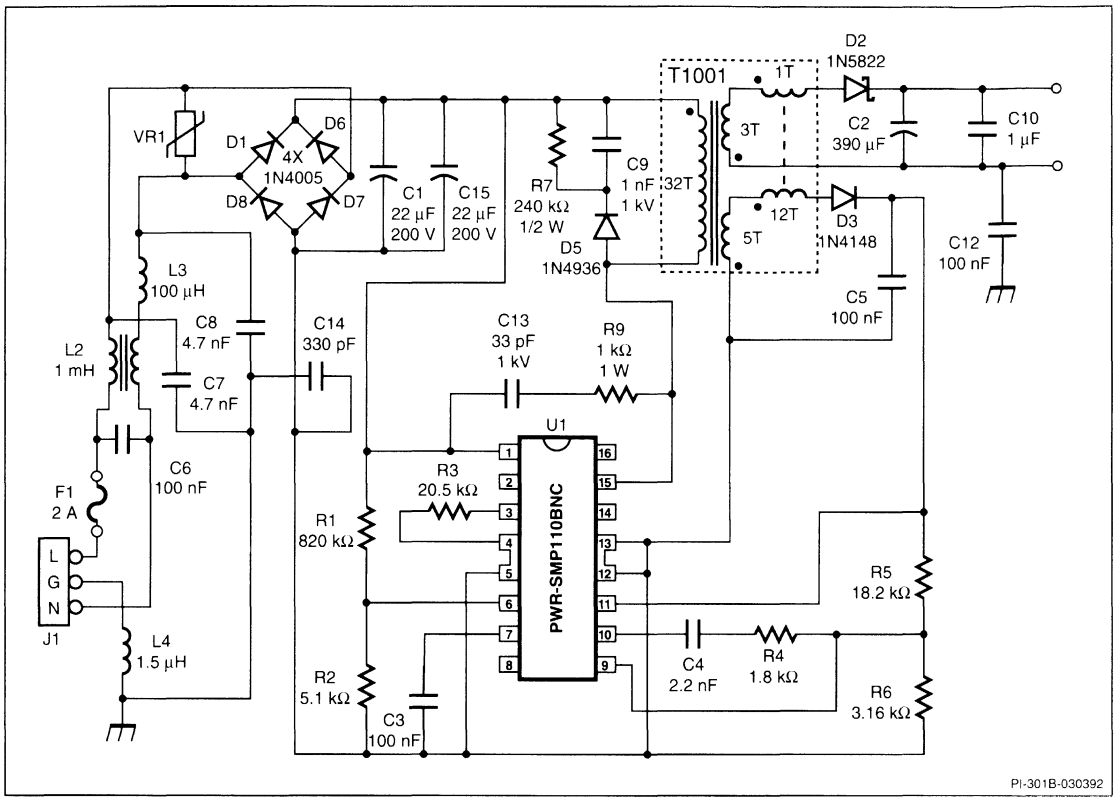


Figure 4. Schematic Diagram of a 10 W Off-line Power Supply Utilizing the PWR-SMP110. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1001 standard transformer (see DA-3), will produce a 5 volt, 10 watt power supply that will operate from 85 to 140 V(rms) AC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP110 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective turns ratio can be fine-tuned if necessary by the number of junctions in D3. Three elements affect the regulation of the output voltage; maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

L2, L3, L4, C6, C7, C8, C12, and C14 form an EMI filter. D1, D6, D7, D8, and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. D5, C9, and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C13 and R9 damps the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP3. C3 and C5 are bypass capacitors. R1 and R2 form a voltage divider network that sets the input undervoltage and overvoltage lockout trip points.

General Circuit Operation (cont.)

This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL2 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP110. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

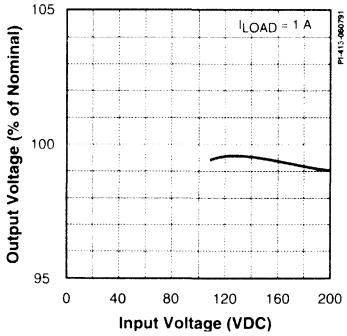
The line and load regulation graphs shown below were measured on a PWR-EVAL2 board operated from a DC source. The switching frequency of the power supply was measured at 850 kHz.

The maximum output power curve shows the power output capability for the standard transformer T1001, and the performance with half the normal number of primary turns. See DA-3 for further information on ordering transformers for use with the PWR-SMP110.

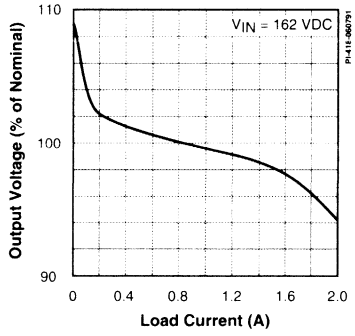
The output power versus frequency curve was generated by characterization of the PWR-SMP110 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

Typical Performance Characteristics (Figure 4 Power Supply)

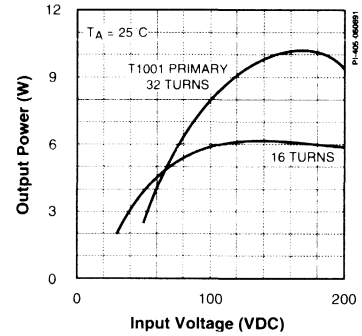
LINE REGULATION



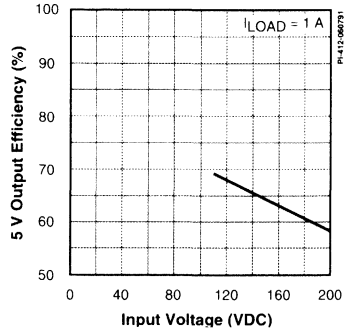
LOAD REGULATION



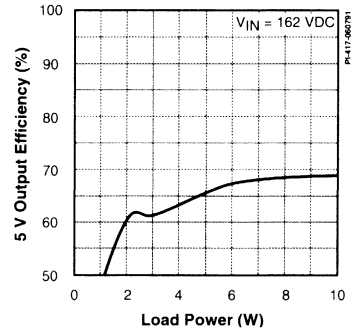
MAXIMUM OUTPUT POWER



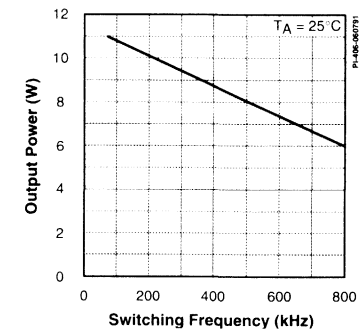
EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



OUTPUT POWER vs. FREQUENCY



ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	390 V
V_{IN} Voltage	350 V
V_{BIAS} Voltage	11 V
Drain Current[2]	800 mA
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 125°C
Ambient Temperature	0 to 70°C
Junction Temperature[2]	150°C
Lead Temperature[4]	260°C
Power Dissipation (T_A = 25°C)	2.1 W
(T_A = 70°C)	1.05 W
Thermal Impedance (θ_{JA})	43°C/W
Thermal Impedance (θ_{JC})[5]	6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	800	950	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC	C_{EXT} = Open	0-35	0-39		%
		f_{OSC} = 200 kHz	0-48	0-50		
CIRCUIT PROTECTION						
Input UV Trip-off			0.29	0.34	0.39	V
Input UV Hysteresis			35	50	70	mV
Input OV Trip-off		See Note 1	1.17	1.25	1.33	V
Input OV Hysteresis			40	60	80	mV
OV/UV Turn-off Delay Time		See Figure 5		250	500	ns
Thermal Shutdown Temperature	$t_{d(off)}$		115	135		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	TYP	MAX	Units
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C		14	16	Ω
			T_J = 115°C		21	25	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		350			mA
OFF-State Current	I_{DSS}	V_{DRAIN} = 280 V, T_A = 115°C			10	25	µA
Breakdown Voltage	BV_{DSS}	I_D = 100 µA, T_A = 25°C		350			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			22		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 200 V			170		nJ
Rise Time	t_R	See Figure 5			33	100	ns
Fall Time	t_F	See Figure 5			8	15	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		350	V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
SUPPLY (cont.)						
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$		6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected		4	5.0	mA
		V_{BIAS} > 8.25 V			0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback	8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback		4	5.0	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP110 is connected to a high voltage power source when the test circuit is activated.

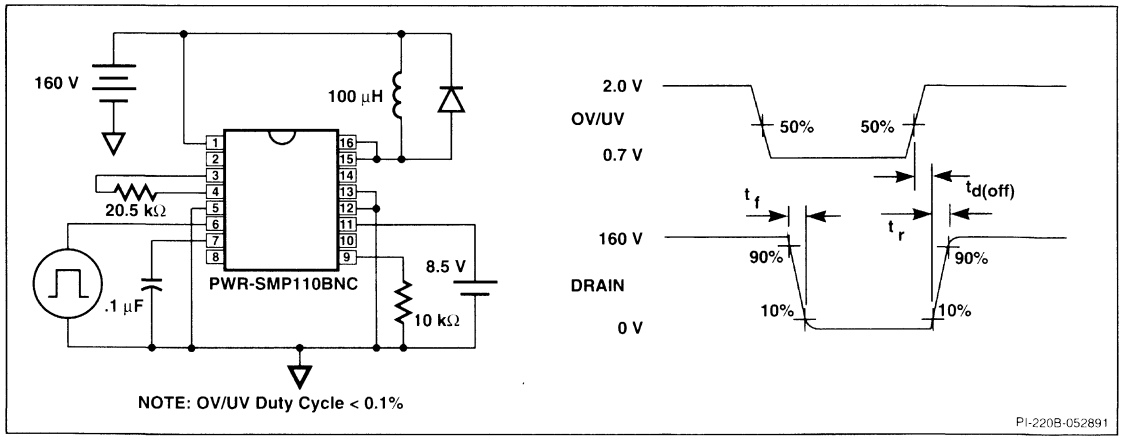
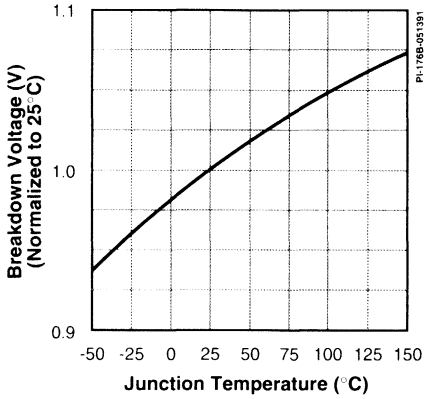
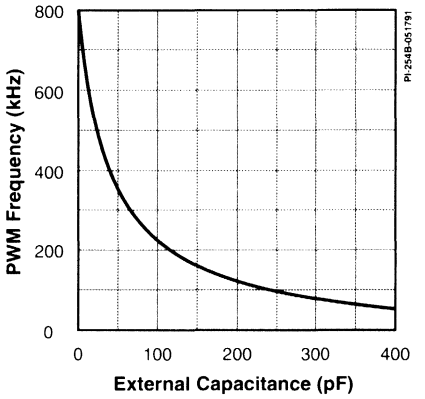


Figure 5. Switching Time Test Circuit

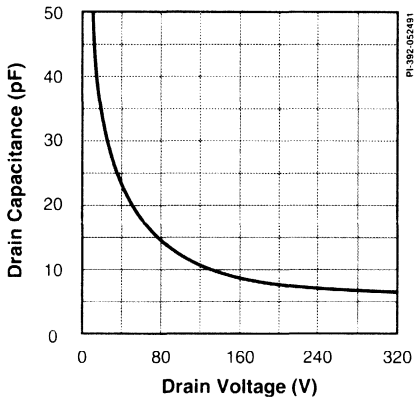
BREAKDOWN vs. TEMPERATURE



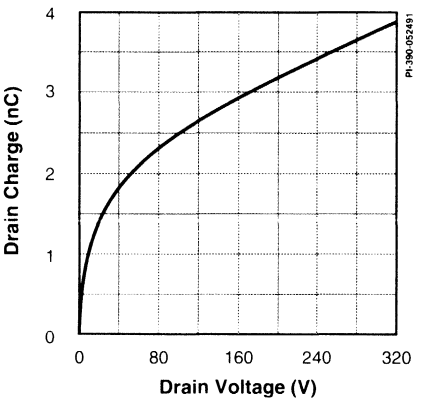
f_{PWM} vs. EXTERNAL CAPACITANCE



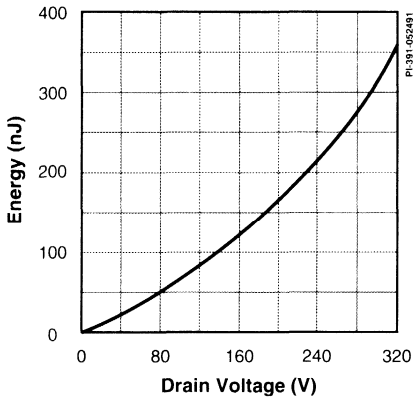
C_{OSS} vs. DRAIN VOLTAGE



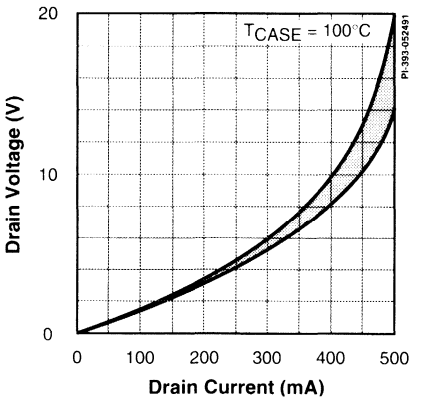
DRAIN CHARGE vs. DRAIN VOLTAGE



DRAIN CAPACITANCE ENERGY



TRANSFER CHARACTERISTICS



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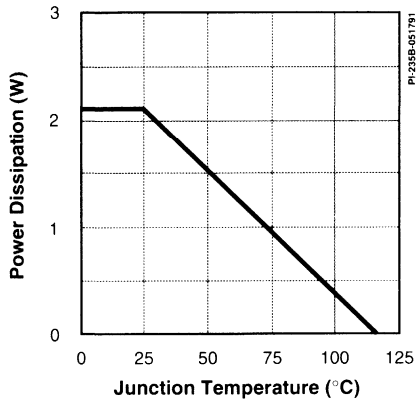
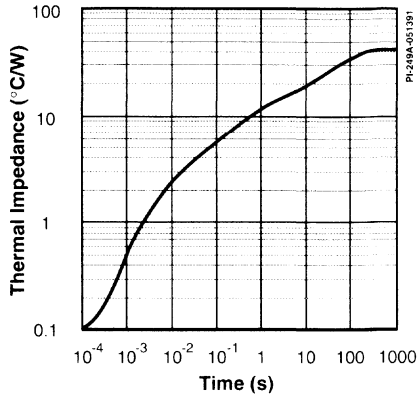
PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP120

PWM Power Supply IC

120 VAC Input
Isolated, Regulated DC Output

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 20 W from rectified 120 VAC input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for 120 V off-line applications
- Can also be used with DC inputs from 36 V to 200 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Inherent current limiting protects from short-circuits
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

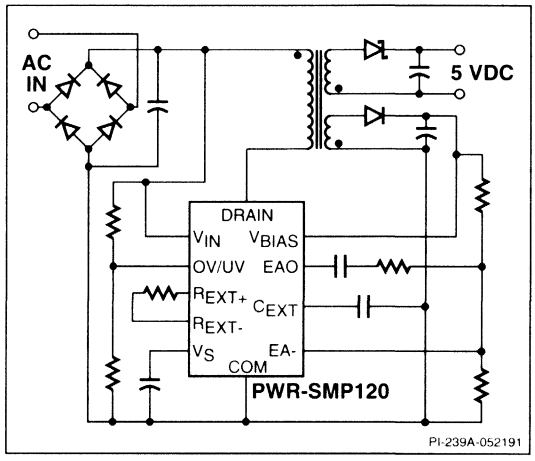


Figure 1. Typical Application

Description

The PWR-SMP120, intended for off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance and lower gate threshold voltage results in a tenfold reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP120 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference voltage, error amplifier, gate driver, undervoltage lockout, over-temperature protection, and current limiting. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies.

The PWR-SMP120 is available in a 16-pin plastic DIP package.

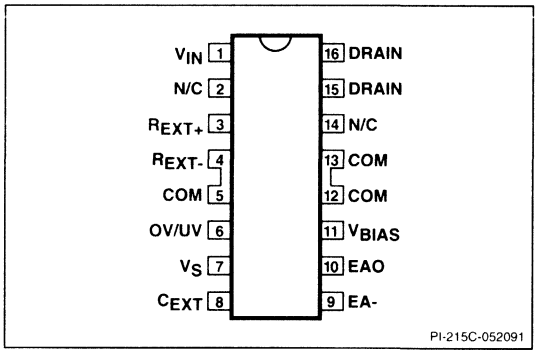


Figure 2. Pin Configuration

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP120BNC	16-pin PWR PDIP	0 to 70°C

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13:
COM connections. Ground or reference point for the circuit.

Pin 6:
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9:
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10:
EAO is the error amplifier output for connection to the external compensation network.

Pin 11:
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15, 16:
Open **DRAIN** of the output MOSFET. Both pins must be externally connected.

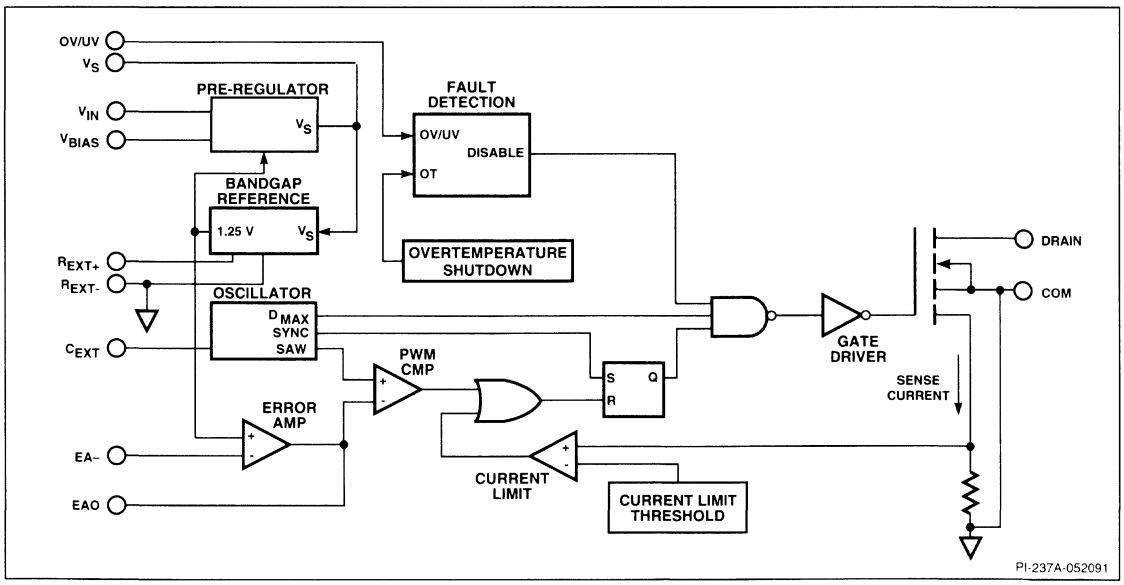


Figure 3. Functional Block Diagram of the PWR-SMP120.

PWR-SMP120 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit connected to V_{BIAS}.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. The oscillator frequency can be lowered by adding additional capacitance at the C_{EXT} pin.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of around 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Current Limit Protection
The current limit sense consists of a current mirror on the power device and a sense resistor. The current mirror produces a current proportional to the drain current of the power switch. A sense voltage is generated by passing the mirror current through a sense resistor. This voltage is then compared to a reference voltage using an internal comparator.

20 W, 110 VAC Input Power Supply with Feedback Winding Regulation

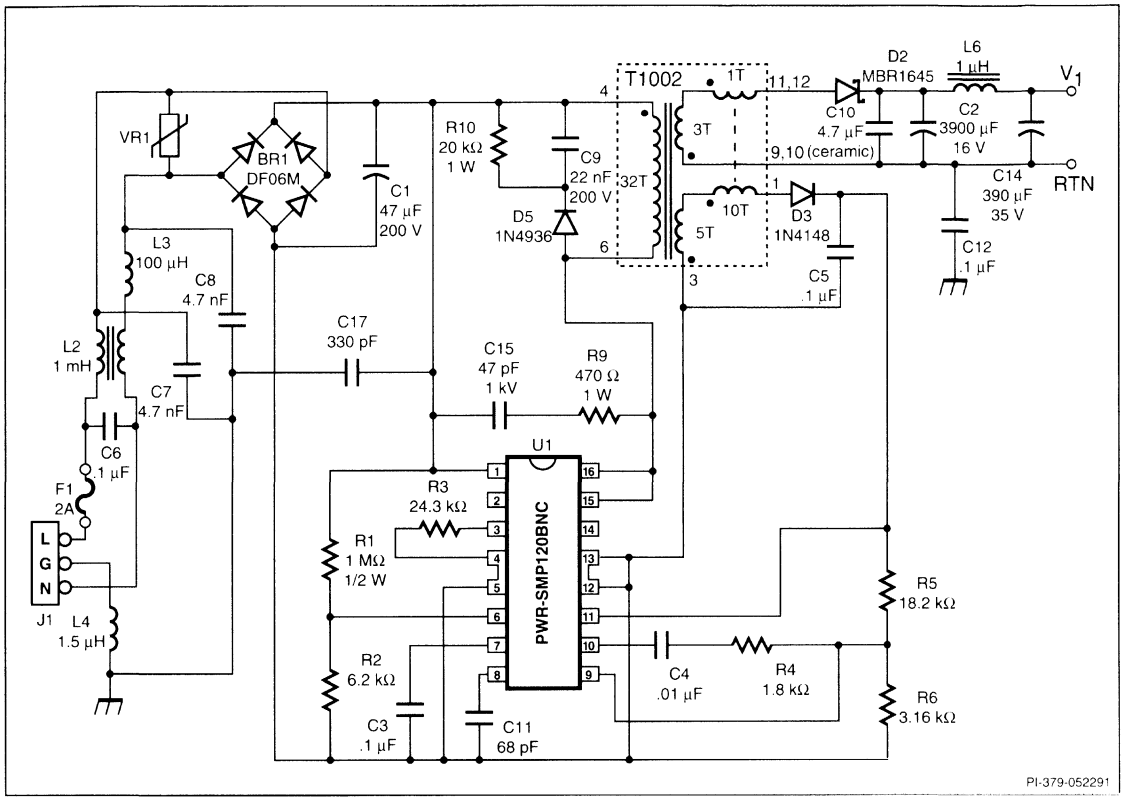


Figure 4. Schematic Diagram of a dual output 20 W Supply Utilizing the PWR-SMP120. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 20 watt power supply that will operate from 85 to 140 V(rms) AC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP120 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective turns ratio can be fine-tuned if necessary by the number of junctions in D3. Three elements affect the regulation of the output voltage; maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

L2, L3, L4, C6, C7, C8, C12, and C17 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damps the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP120. C11 sets the frequency of operation. If no capacitor is connected to pin 8, the internal capacitor will set the frequency to approximately 850 kHz. C3 and C5 are bypass capacitors. R1 and R2 form a voltage divider network that sets the input undervoltage and overvoltage lockout trip points.

General Circuit Operation (cont.)

To achieve full output power and reliable operation of the PWR-SMP120, both DRAIN connections (pin 15 and 16) must be connected together at the printed circuit board.

This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL3 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP120. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

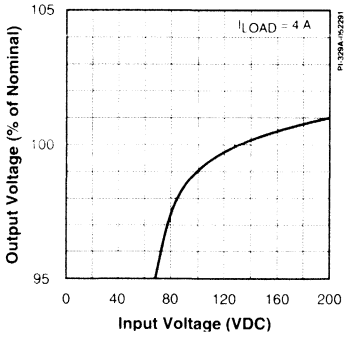
The line and load regulation graphs shown below were measured on a PWR-EVAL3 board operated from a DC source. The switching frequency of the power supply was measured at 310 kHz.

The maximum output power curve shows the power output capability for the standard transformer T1002, and the performance with half the normal number of primary turns. See DA-3 for further information on ordering transformers for use with the PWR-SMP120.

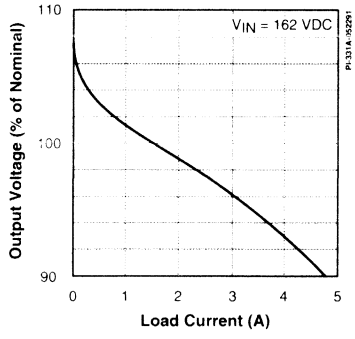
The output power versus frequency curve was generated by characterization of the PWR-SMP120 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

Typical Performance Characteristics (Figure 4 Power Supply)

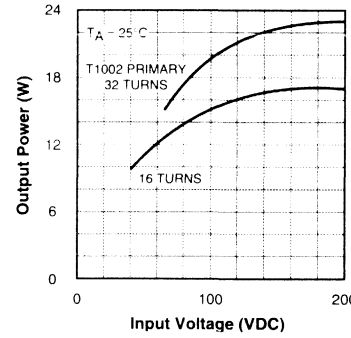
LINE REGULATION



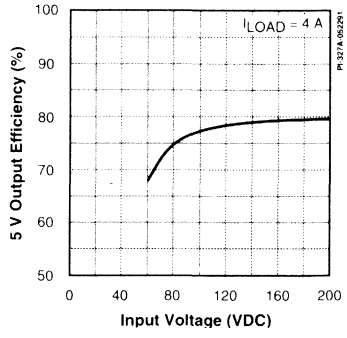
LOAD REGULATION



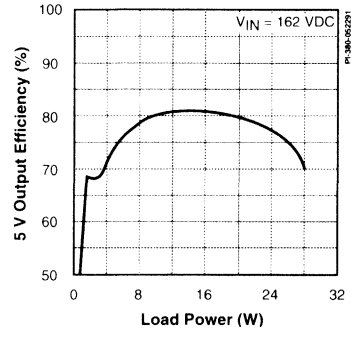
MAXIMUM OUTPUT POWER



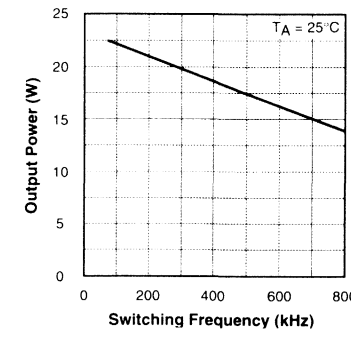
EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



OUTPUT POWER vs. FREQUENCY



ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	350 V
V_{IN} Voltage	350 V
V_{BIAS} Voltage	11 V
Drain Current[2]	2.5 A
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	-65 to 125°C
Ambient Temperature	0 to 70°C
Junction Temperature[2]	150°C
Lead Temperature[4]	260°C
Power Dissipation (T_A = 25°C)	2.1 W
(T_A = 70°C)	1.05 W
Thermal Impedance (θ_{JA})	43°C/W
Thermal Impedance (θ_{JC})[5]	6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	825	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC	C_{EXT} = Open	0-35	0-45		%
		f_{OSC} = 200 kHz	0-45	0-50		
CIRCUIT PROTECTION						
Current Limit Threshold			0.9	1.1	1.25	A
Input UV Trip-off Voltage			0.29	0.34	0.39	V
Input UV Hysteresis			35	50	70	mV
Input OV Trip-off		See Note 1	1.17	1.25	1.33	V
Input OV Hysteresis			40	60	80	mV
OV/UV Turn-off Delay Time	$t_{d(off)}$	See Figure 5		250	500	ns
Thermal Shutdown Temperature			115	135		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 500 mA	T_J = 25°C		3	4.1	Ω
			T_J = 115°C		5.3	6.4	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		0.9	1.1		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 280 V, T_A = 115°C			10	25	µA
Breakdown Voltage	BV_{DSS}	I_D = 100 µA, T_A = 25°C		350			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			75		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 200 V			480		nJ
Rise Time	t_R	See Figure 5			5	20	ns
Fall Time	t_F	See Figure 5			50	100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		350	V

1

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = 0 to 70°C	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
SUPPLY (cont.)						
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$		6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open		4	5.0	mA
		V_{BIAS} >8.25 V			0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback	8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback		4	5.0	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP120 is connected to a high voltage power source when the test circuit is activated.

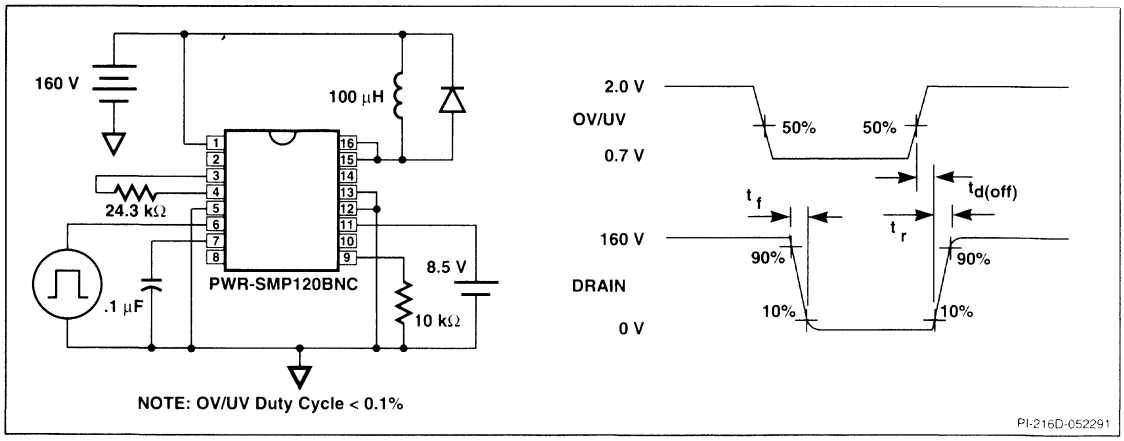
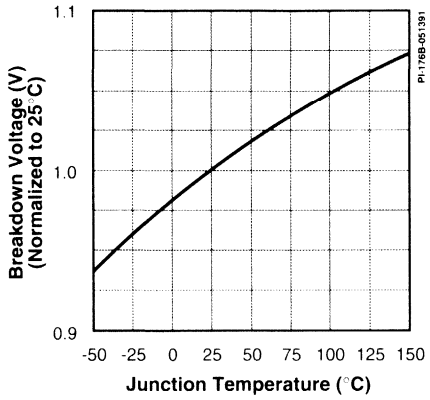
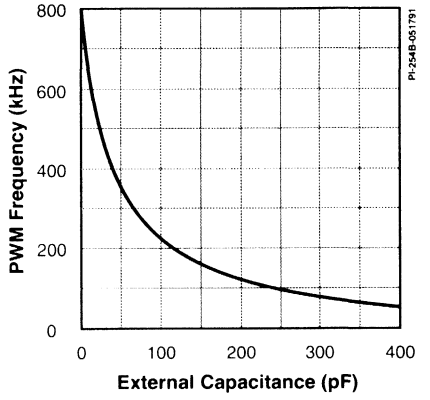


Figure 5. Switching Time Test Circuit.

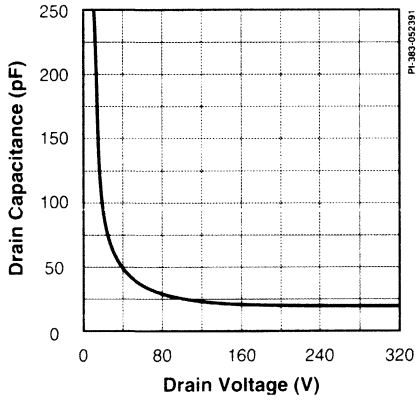
BREAKDOWN vs. TEMPERATURE



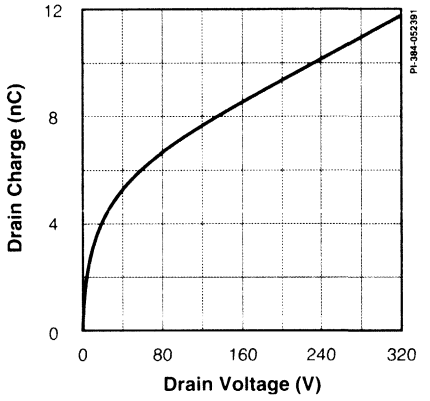
f_{PWM} vs. EXTERNAL CAPACITANCE



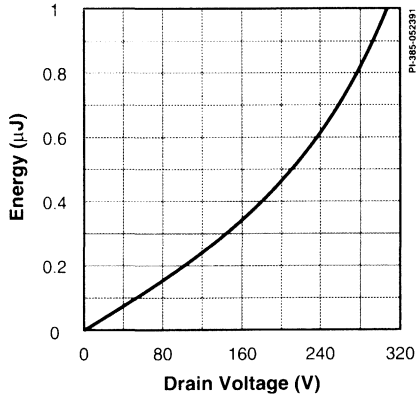
C_{OSS} vs. DRAIN VOLTAGE



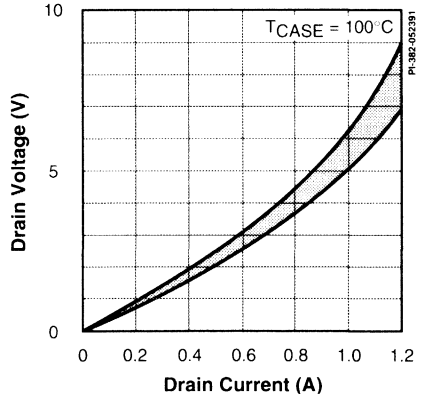
DRAIN CHARGE vs. DRAIN VOLTAGE



DRAIN CAPACITANCE ENERGY

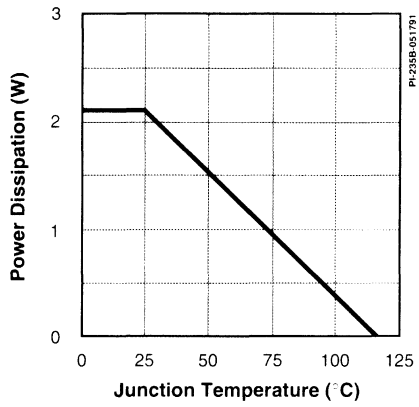


TRANSFER CHARACTERISTICS

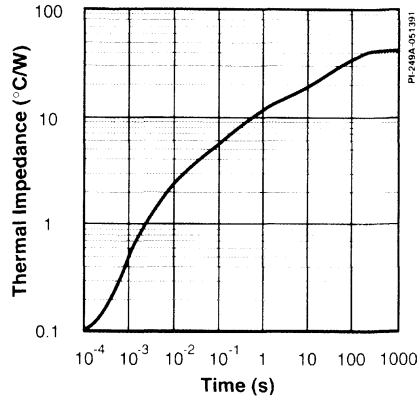


1

PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP121

PWM Power Supply IC

120 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 20 W from rectified 120 VAC input
- External transformer provides isolated output voltages
- Configurable for transformer winding or optocoupler feedback

High-voltage, Low-capacitance MOSFET Output
- Designed for 120 V off-line applications
- Can also be used with DC inputs from 36 V to 200 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Optimized for optocoupler feedback

Built-In Self-protection Circuits
- Cycle-by-cycle current limit
- Output overvoltage protection
- Shutdown/auto-restart cycling
- Input undervoltage lockout
- Thermal shutdown

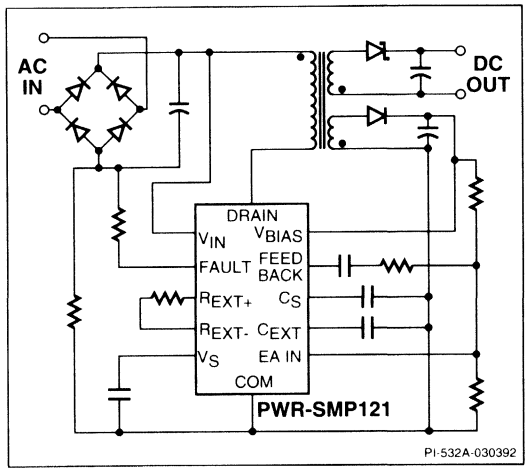


Figure 1. Typical Application

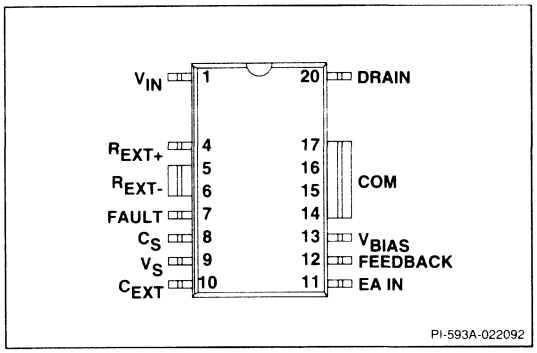


Figure 2. Pin Configuration

Description

The PWR-SMP121, intended for 120 V power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The PWR-SMP121 has been designed for maximum flexibility in feedback techniques. An error amplifier has been included for use with feedback winding regulation, or it can be bypassed for direct optical feedback to the PWM comparator.

The controller section of the PWR-SMP121 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The PWR-SMP121 is available in a 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP121SRI	20-pin PWR SOIC	-40 to 85°C

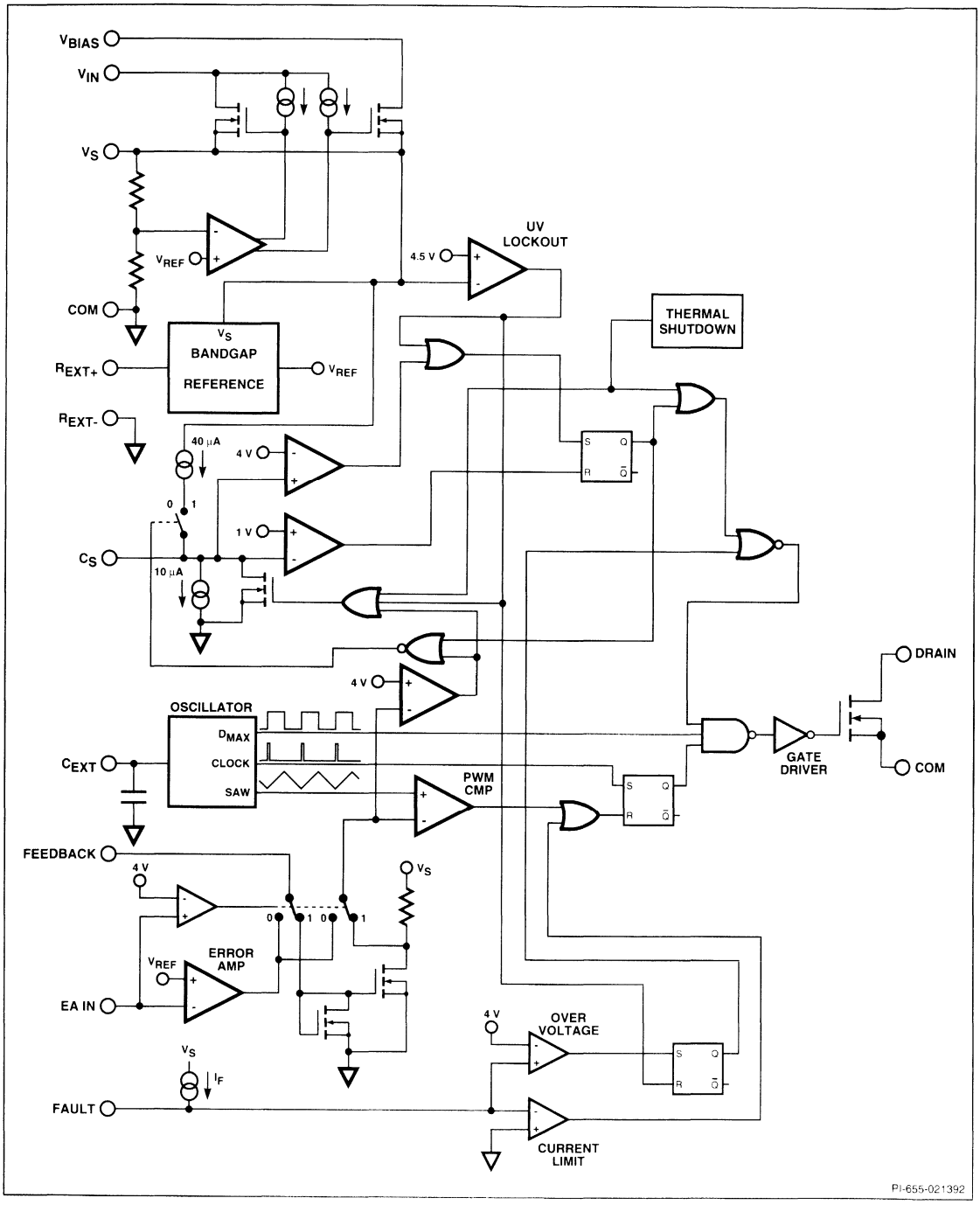


Figure 3. Functional Block Diagram of the PWR-SMP121.

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 4:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 5, 6:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 7:
The **FAULT** pin is used with an external resistor to provide protection of the output during overcurrent and overvoltage conditions.

Pin 8:
C_S is used to set the shutdown/auto-restart cycle time.

Pin 9:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 10:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 11:
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks. Connecting this pin to V_S disables the error amplifier when using optocoupler feedback.

Pin 12:
FEEDBACK can be driven directly by an optocoupler output, bypassing the internal error amplifier. When using transformer winding feedback control, this pin is used as the error amplifier output for connection to the external compensation network.

Pin 13:
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14, 15, 16, 17:
COM connections. Ground or reference point for the circuit.

Pin 20:
Open **DRAIN** of the output MOSFET.

1

PWR-SMP121 Functional Description

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the current limit comparator at the beginning of each cycle. The maximum duty cycle is equal to the ratio of the charge time to the total period of the oscillator waveform.

PWR-SMP121 Functional Description (cont.)

Optional Error Amplifier Circuitry
The control loop circuitry is configurable for either secondary-referenced optocoupler control or primary-referenced feedback winding control. In both cases, a control voltage is generated and sent to the pulse width modulator for conversion to a duty cycle.

Connecting the EA IN input to V_S configures the control loop for connection to an external optocoupler. In this mode the internal error amplifier is disabled. The optocoupler output transistor emitter connects directly to FEEDBACK, which is configured as an N-channel MOSFET transistor "diode". This connection presents a low impedance and wide collector-emitter voltage to the optocoupler transistor for improved frequency response and speed. The diode current is converted to the control voltage by a mirror transistor and resistor.

For primary-referenced feedback winding control, the EA IN input is simply connected through a resistor divider to the feedback voltage. The internal error amplifier is automatically configured and connected to the pulse width modulator. EA IN is the inverting input to the error amplifier. The non inverting input is internally connected to the 1.25 V bandgap reference. FEEDBACK is connected to an external feedback compensation network for tailoring the frequency response for proper bandwidth, gain margins, and phase margins.

Pulse Width Modulator
The pulse width modulator implements a voltage mode control loop by driving the power MOSFET with a duty cycle proportional to a control voltage. The duty cycle signal is generated by a comparator which compares the control voltage with a sawtooth waveform. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the driver.

Fault Protection
The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output overvoltage protection.

The FAULT pin latches off the power switch when an overcurrent condition causes the voltage on this pin to drop to zero. The DRAIN current is sensed by an external resistor. An internal current source biases the FAULT signal during normal operation. During an overcurrent condition, current flows in the current sense resistor, causing the voltage on the FAULT pin to decrease. If the voltage on the FAULT pin falls below COM for longer than the delay time, the power switch will be latched off until the beginning of the next clock cycle. If this condition persists, the output voltage will fall out of regulation, triggering a shutdown/auto-restart cycle.

For latching overvoltage protection, an external optocoupler can be used to drive the FAULT pin above the 4 V threshold of the overvoltage comparator. This comparator sets a latch that will turn off the power MOSFET until the latch is reset by removing and restoring input power.

Shutdown/Auto-restart
The PWR-SMP121 contains an auto-restart function which will shut off the power supply if the output voltage falls out of regulation. The PWR-SMP121 will try to restart and will test the output after a delay. The PWR-SMP121 will remain shut off for the amount of time determined by the value of C_S, and will then begin the auto-restart cycle. The power supply will resume normal operation if the fault condition has been removed. The power supply will continuously cycle if the output is not regulated within the turn-on delay as determined by C_S. During normal operation, C_S is quickly discharged to 0 V. This function can be disabled by connecting the C_S pin to COM.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysterisis temperature, normal operation resumes.

20 W, 120 VAC Off-line Power Supply with Optocoupler Feedback

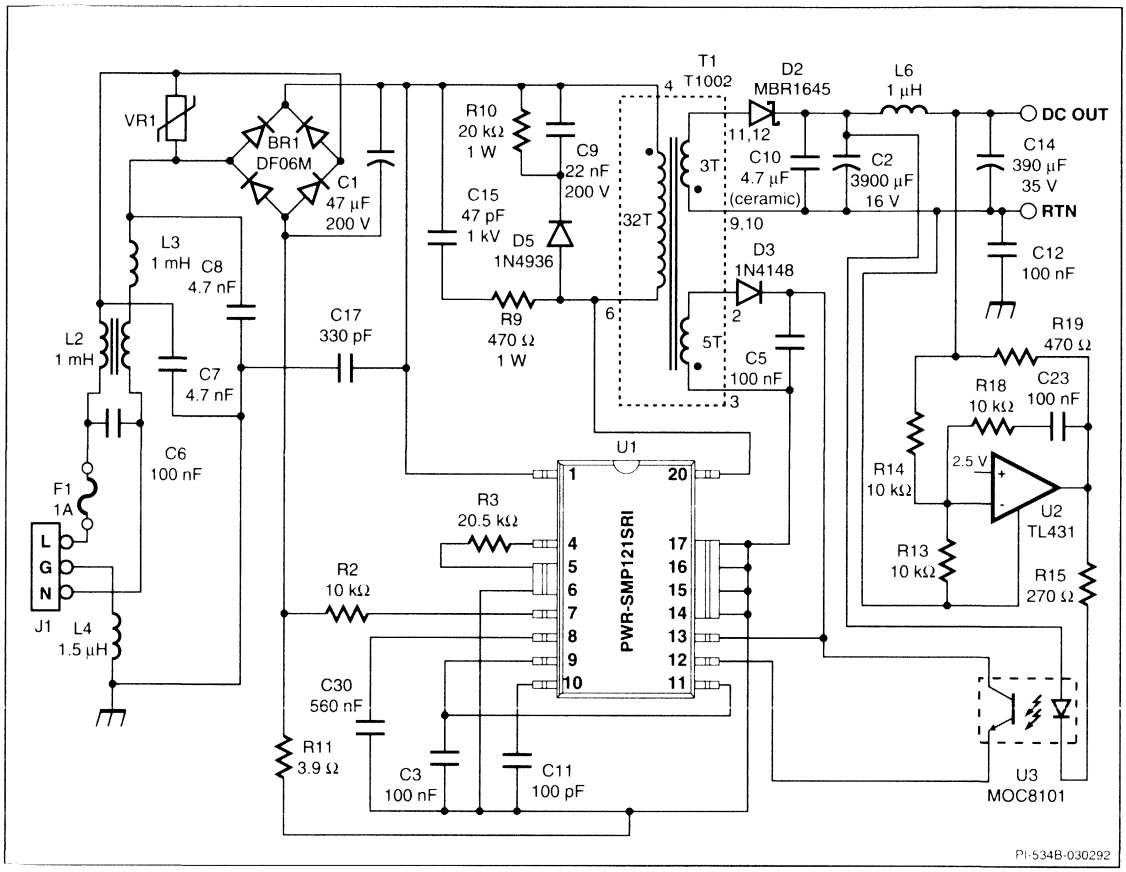


Figure 4. Schematic Diagram of a 5 V, 20 W 120 VAC Power Supply Utilizing the PWR-SMP121.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 20 watt power supply that will operate from 85 to 140 V(rms) AC input voltage. The output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the PWR-SMP121, which directly controls the duty cycle of the integrated high voltage MOSFET switch.

The effective output voltage can be fine-tuned by adjusting the resistive divider formed by R13 and R14. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of transformer T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the PWR-SMP121. The clamp circuit implemented by R10, C9, and D5 clamps the leading edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The power secondary winding is rectified and filtered by D2, C2, C14, C10, and L6 to create the desired output voltage. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the PWR-SMP121, which

General Circuit Operation (cont.)

effectively cuts off the high voltage internal linear regulator. Common mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C12, C17, C7, C8, and L2. Differential mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L3. Voltage spikes on the AC line are clamped by VR1.

Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_S. The oscillator frequency is determined by C11. Transistor switch current is sensed by resistor R11. The initial voltage level at the fault pin is determined by resistor R2. C30 determines the auto-restart time interval.

The secondary-referenced error amplifier control system is implemented with the TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference , error amplifier, and driver. The output voltage is sensed , divided by R13 and R14, and applied to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R18, C23, and the high frequency gain setting resistor R14. Bias current of 2 mA minimum for U2 is provided by resistor R19. The LED current in the optocoupler is limited by resistor R15. Optocoupler U3 drives the error signal into the FEEDBACK pin of the PWR-SMP121. Note that the EA IN pin must be connected to the V_S pin to properly configure the PWR-SMP121 for this type of control.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high voltage linear regulator. Ensure that the maximum specified voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

Implementing Output Overvoltage Protection

If the load is extremely sensitive to overvoltage conditions, an overvoltage shutdown function can be implemented as shown in Figure 5. The output voltage is fed back to the PWR-SMP121 via an op amp and optocoupler. If the voltage at pin 7 is greater than 4 V, the internal latch will shut off the output.

The PWR-SMP121 must be restarted by removing the input voltage and then reapplying it, causing the latch to reset and the circuit to begin a new startup cycle.

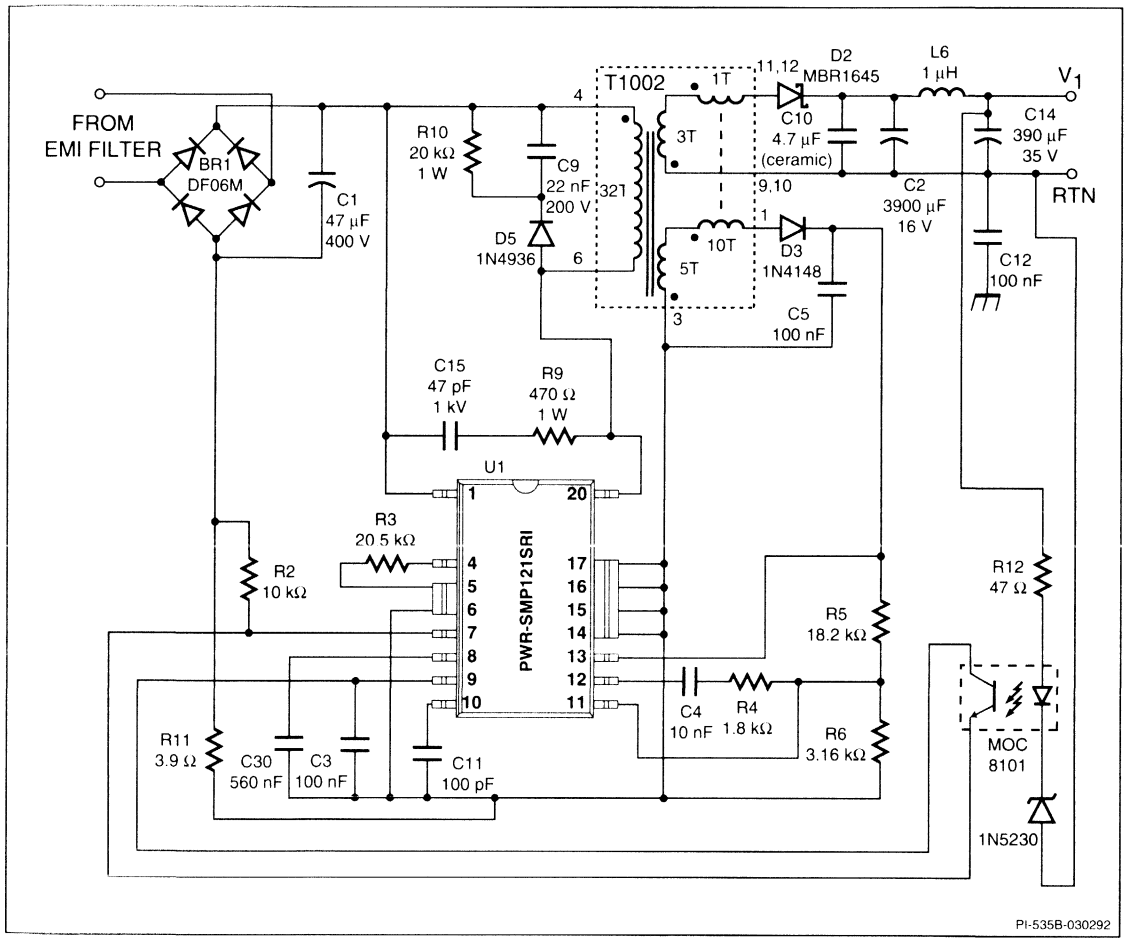


Figure 5. Implementing Feedback Winding Regulation and Output Overvoltage Protection.

ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	350 V
V_{IN} Voltage	350 V
V_{BIAS} Voltage	35 V
Drain Current[2]	2.5 A
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 125°C
Ambient Temperature	-40 to 85°C
Junction Temperature[4]	150°C
Lead Temperature[5]	260°C
Power Dissipation (T_A = 25°C)	3.0 W
(T_A = 70°C)	1.5 W
Thermal Impedance (θ_{JA})	30°C/W
Thermal Impedance (θ_{JC})[6]	6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 15/16.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	850	kHz
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
		f_{OSC} = 200 kHz	0-48	0-50		
Optocoupler Output Current	I_C	EA IN = V_S, Maximum Duty Cycle	400		600	µA
Dynamic Control Current	i_C	0 to Maximum Duty Cycle	50	100	200	µA
CIRCUIT PROTECTION						
FAULT Offset Current				100		µA
FAULT OV Threshold	V_{OV}			4		V
FAULT Current Limit Threshold	V_{ILIMIT}			0		V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
CIRCUIT PROTECTION (cont.)						
Current Limit Delay Time	$t_{d(off)}$	See Figure 6	75	150	250	ns
Thermal Shutdown Temperature			125	140		°C
Thermal Shutdown Hysteresis				15		°C
SHUTDOWN/AUTO-RESTART						
ON Time	t_{ON}	See Figure 7		38		ms
OFF Time	t_{OFF}	See Figure 7		150		ms
Reset Time	t_{RESET}	See Figure 7		12.5		ms
Charge/Discharge Ratio				4:1		
Upper Threshold Voltage	V_{THU}			4.0		V
Lower Threshold Voltage	V_{THL}			1.0		V
ERROR AMPLIFIER						
Reference Voltage	V_{REF}		1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}			50		ppm/°C
Gain-Bandwidth Product				500		kHz
DC Gain	A_{VOL}		60	80		dB
Output Impedance	Z_{OUT}			1.5		kΩ

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 160 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT (cont.)							
ON-State Resistance	$R_{DS(ON)}$	I_D = 200 mA	T_J = 25°C		3	4	Ω
			T_J = 115°C		5.5	6.5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_J = 25°C	1.45	1.7		A
			T_J = 115°C	0.9	1.3		
OFF-State Current	I_{DSS}	V_{DRAIN} = 280 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		350			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			75		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 200 V			480		nJ
Rise Time	t_r	See Figure 6			70	150	ns
Fall Time	t_f	See Figure 6			70	150	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open			3	4.5	mA
		V_{BIAS} > 8.25 V				0.1	
		Thermal Shutdown ON				2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied		8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied			3	4.5	mA
V_S Source Voltage	V_S			5.1		6.0	V
V_S Source Current	I_S					400	µA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP121 is connected to a high voltage power source when the test circuit is activated.

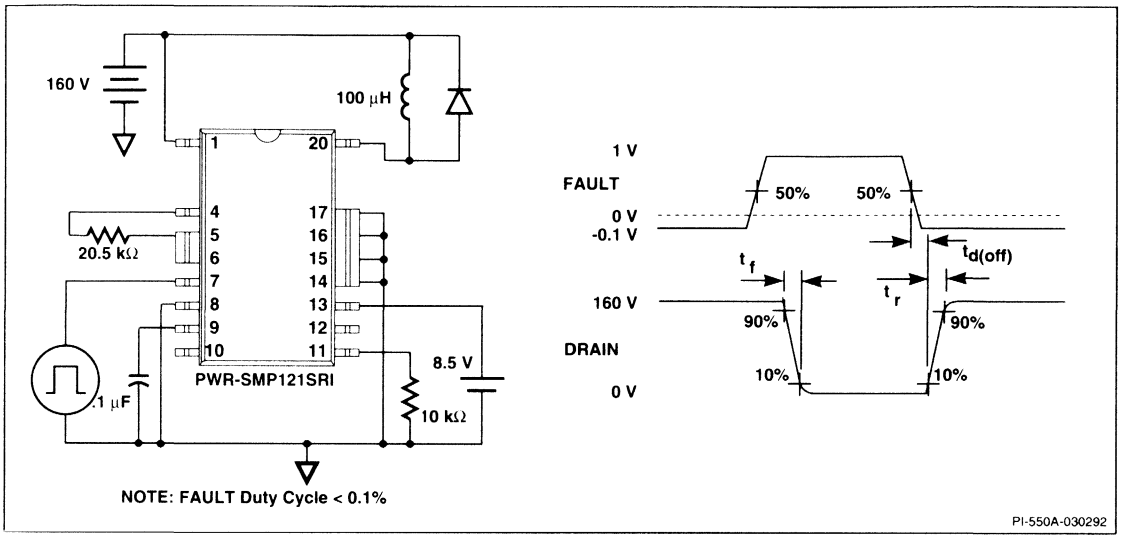


Figure 6. Current Limit Delay/Switching Time Test Circuit.

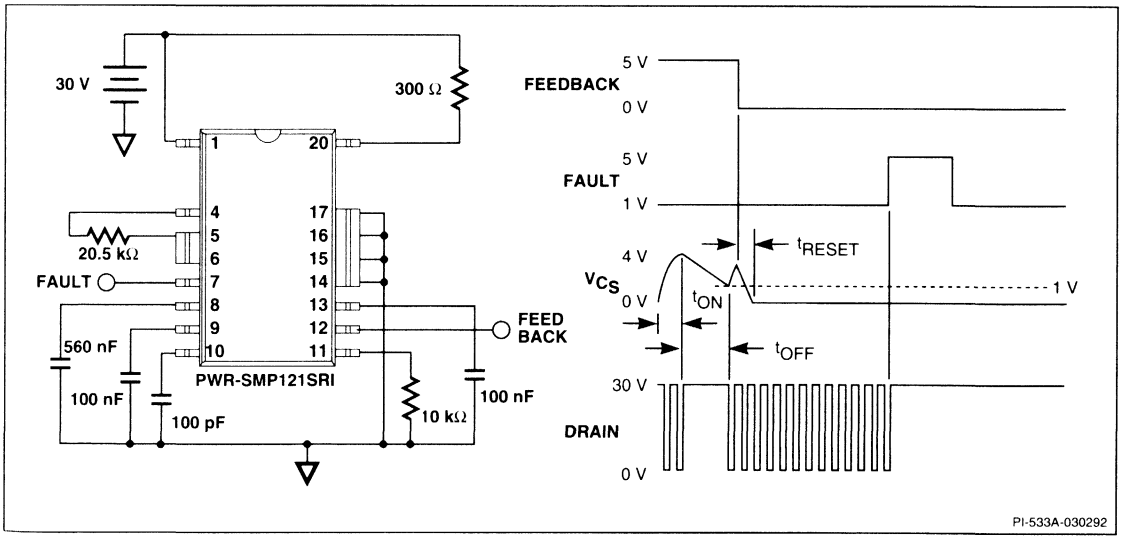
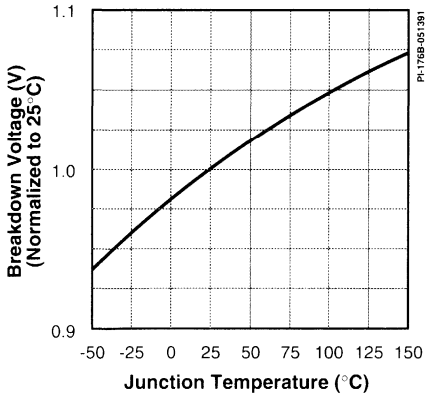
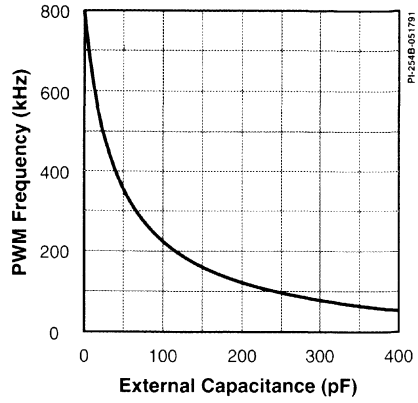


Figure 7. Auto-restart Test Circuit.

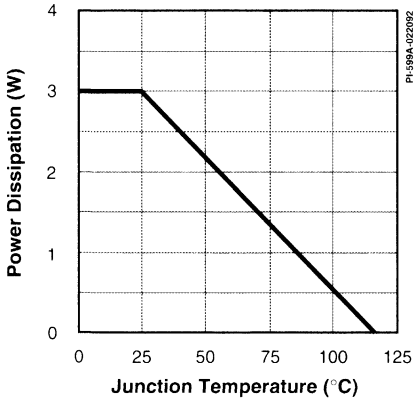
BREAKDOWN vs. TEMPERATURE



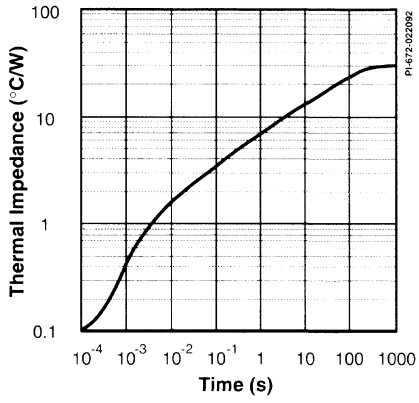
f_{PWM} vs. EXTERNAL CAPACITANCE



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP210

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from rectified 220 VAC input, 5 W from rectified universal (85 to 265 VAC) input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Cycle-by-cycle Current Limit
- Input undervoltage lockout
- Thermal shutdown

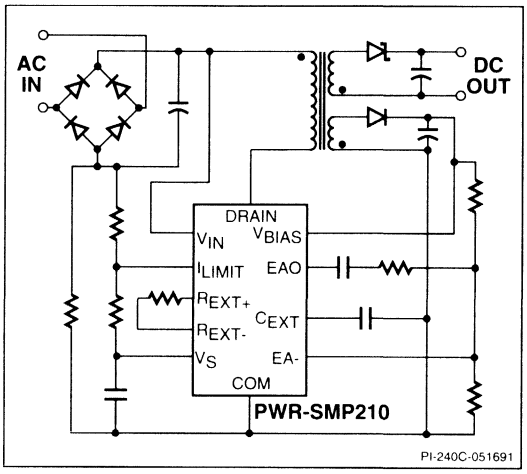


Figure 1. Typical Application

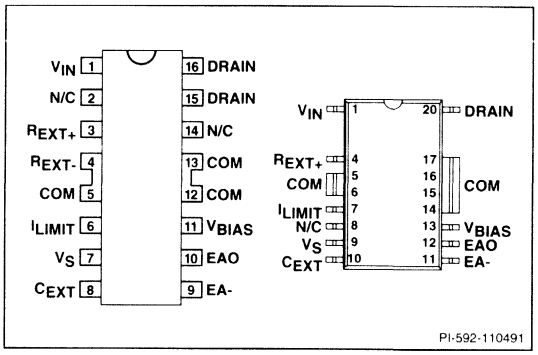


Figure 2. Pin Configuration

Description

The PWR-SMP210, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low-cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance and lower gate threshold voltage results in a tenfold reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP210 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The PWR-SMP210 is available in a 16-pin plastic batwing DIP or 20-pin batwing SOIC package.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP210BNC	16-pin PWR PDIP	0 to 70°C
PWR-SMP210BNI	16-pin PWR PDIP	-40 to 85°C
PWR-SMP210SRI	20-pin PWR SOIC	-40 to 85°C

Pin Functional Description

(Pin Number in Parenthesis is for SOIC Version)

Pin 1(1):
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3(4):
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4(5, 6):
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13(14, 15, 16, 17):
COM connections. Ground or reference point for the circuit.

Pin 6(7):
I_{LIMIT} is used with an external resistor divider provide protection of the output MOSFET from excessive current.

Pin 7(9):
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8(10):
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9(11):
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10(12):
EAO is the error amplifier output for connection to the external compensation network.

Pin 11(13):
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15, 16(20):
Open **DRAIN** of the output MOSFET. Both pins must be externally connected.

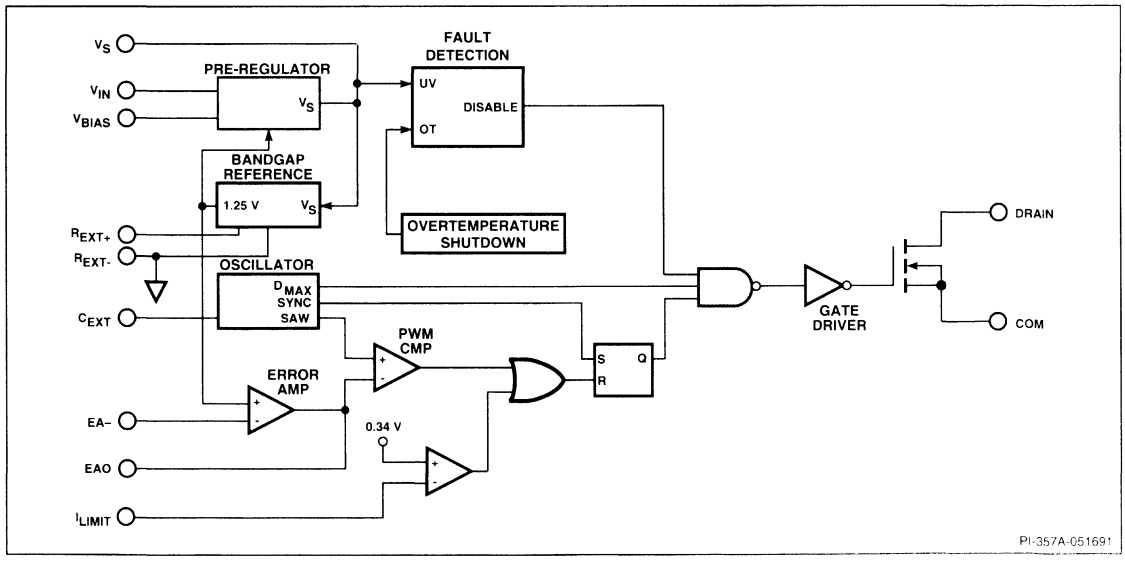


Figure 3. Functional Block Diagram of the PWR-SMP210.

PWR-SMP210 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit connected to V_{BIAS}.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout is maintained whenever V_S is less than 5 V.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. The oscillator frequency can be lowered by adding additional capacitance at the C_{EXT} pin.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of around 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

Current Limit Protection
The I_{LIMIT} signal latches off the power switch when the voltage on this pin drops below its threshold. The DRAIN current is sensed by an external resistor. A voltage divider between the V_S voltage and the current sense resistor biases the I_{LIMIT} signal more positive than its threshold voltage. When current is flowing in the current sense resistor, the voltage on the I_{LIMIT} pin will decrease. If the voltage on the I_{LIMIT} pin is below the threshold for longer than the delay time, the power switch will be latched off until the beginning of the next clock cycle.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

5 W Universal Off-line Power Supply with Feedback Winding Regulation

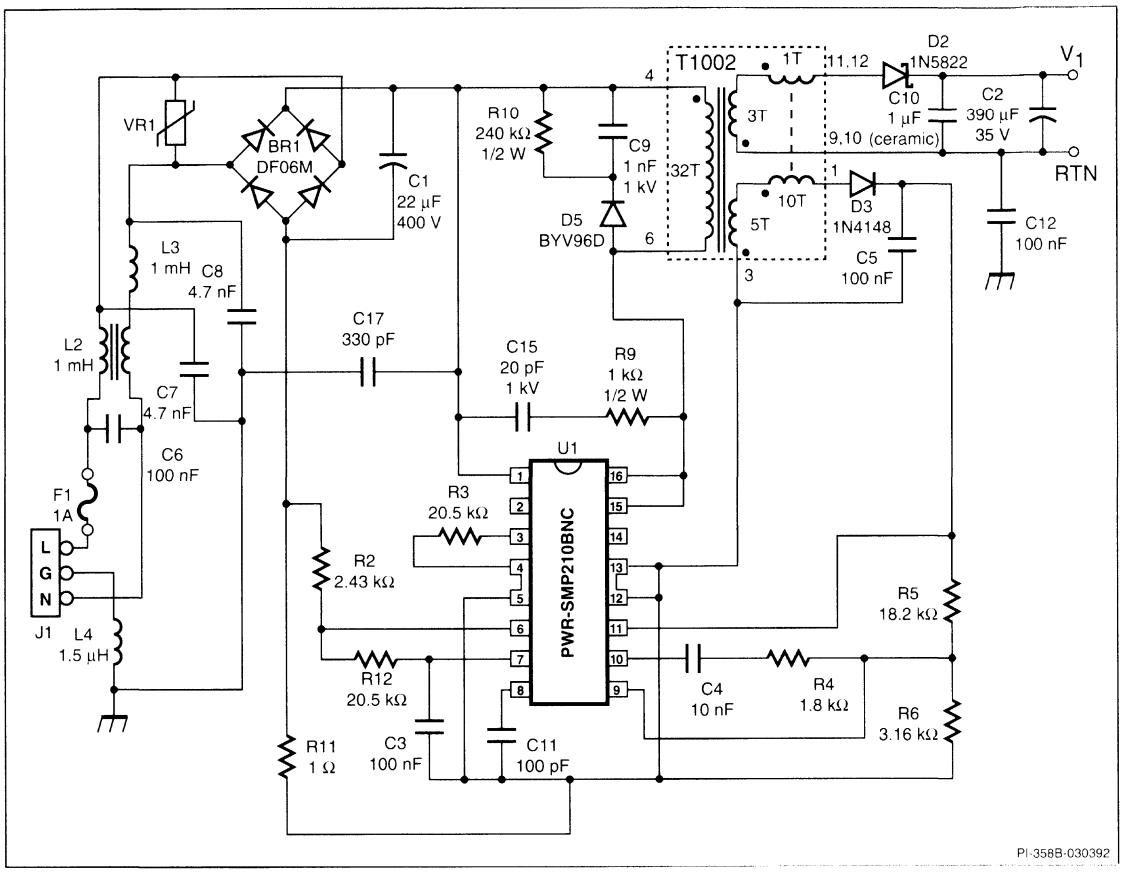


Figure 4. Schematic Diagram of a 5 V, 5 W Universal Input Power Supply Utilizing the PWR-SMP210. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP210 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective turns ratio can be fine-tuned if necessary by the number of junctions in D3. Three elements affect the regulation of the output voltage; maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

L2, L3, L4, C6, C7, C8, C12 and C17 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damps the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP210. C11 sets the frequency of operation. If no capacitor is connected to pin 8, the internal capacitor will set the frequency to approximately 850 kHz. C3 and C5 are bypass capacitors. R2, R11, and R12 form the cycle-by-cycle current limit circuitry. These values provide maximum power output while maintaining short circuit protection.

General Circuit Operation (cont.)

To achieve full output power and reliable operation of the PWR-SMP210, both DRAIN connections on the batwing DIP package (pin 15 and 16) must be connected together at the printed circuit board. Pin 15 and 16 are not connected within the package.

This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL5 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP210. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

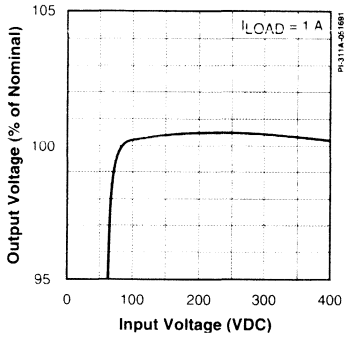
The line and load regulation graphs shown below were measured on a PWR-EVAL5 board operated from a DC source. The switching frequency of the power supply was measured at 250 kHz.

The maximum output power curve shows the power output capability for the standard transformer T1002, and the performance with twice and half the normal number of primary turns. See DA-3 for further information on ordering transformers for use with the PWR-SMP210.

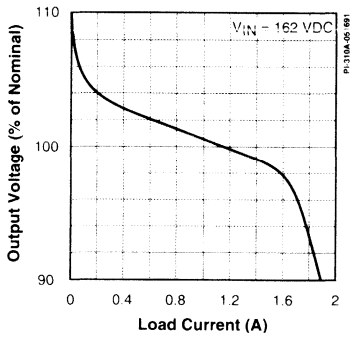
The output power versus frequency curve was generated by characterization of the PWR-SMP210 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

Typical Performance Characteristics (Figure 4 Power Supply)

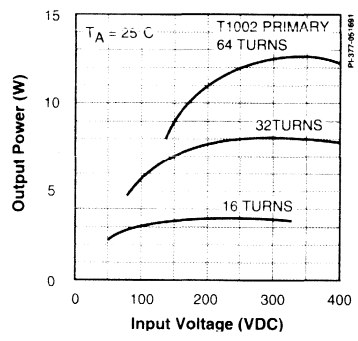
LINE REGULATION



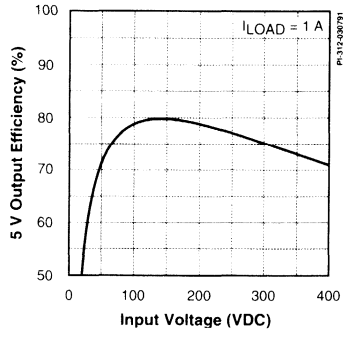
LOAD REGULATION



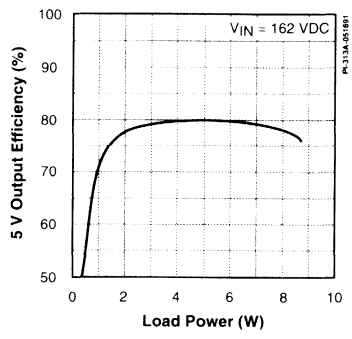
MAXIMUM OUTPUT POWER



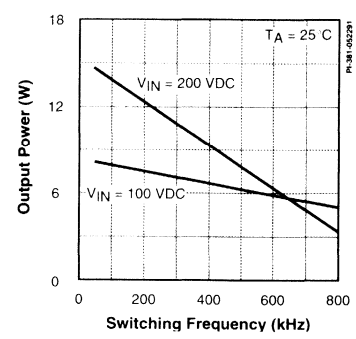
EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



OUTPUT POWER vs. FREQUENCY



ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage ..... 800 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 11 V
Drain Current ..... 800 mA
Input Voltage[2] ..... - 0.3 V to V_S + 0.3 V
Storage Temperature ..... –65 to 125°C
Ambient Temperature (C Suffix) ..... 0 to 70°C
(I Suffix) ..... -40 to 85°C
Junction Temperature[3] ..... 150°C
Lead Temperature[4] ..... 260°C
Power Dissipation
BN Suffix (T_A = 25°C) ..... 2.1 W
(T_A = 70°C) ..... 1.05 W
Power Dissipation
SR Suffix (T_A = 25°C) ..... 3.0 W
(T_A = 70°C) ..... 1.5 W
Thermal Impedance (θ_{JA})(BN Suffix) ..... 43°C/W
(SR Suffix) ..... 30°C/W
Thermal Impedance (θ_{JC})[5](BN Suffix) ..... 6°C/W
(SR Suffix) ..... 6°C/W

1. Unless noted, all voltages referenced to COM.
2. Does not apply to V_{IN} or DRAIN.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, (T_A = Full Operating Range (see Note 1)	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	850	kHz
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
		f_{OSC} = 200 kHz	0-48	0-50		
CIRCUIT PROTECTION						
Current Limit Voltage Range		See Note 2	0		1	V
Current Limit Threshold			0.31	0.34	0.37	V
Current Limit Delay Time	$t_{d(off)}$	See Figure 5		250	500	ns
Thermal Shutdown Temperature			115	135		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, (T_A = Full Operating Range (see Note 1))		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product					500		kHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		20	35	Ω
			T_j = 115°C		32	42	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		200	380		mA
OFF-State Current	I_{DSS}	V_{DRAIN} = 640 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		800	900		V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			70		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V			1000		nJ
Rise Time	t_r	See Figure 5			70	150	ns
Fall Time	t_f	See Figure 5			70	150	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		500	V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ (T_A = Full Operating Range (see Note 1))		Test Limits MIN	TYP	MAX	Units
SUPPLY (cont.)							
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open	C Suffix		3	4.5	mA
			I Suffix		3	5.0	
		V_{BIAS} > 8.25 V				0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback	C Suffix		3	4.5	mA
			I Suffix		3	5.0	
V_S Source Voltage	V_S			5.1		6.0	V
V_S Source Current	I_S					400	µA

NOTES:

1. Those specifications having only one limit number apply over the entire temperature range for both C Suffix (0 to 70°C), and I Suffix (-40 to 85°C) versions. Those specifications with a split limit showing each temperature range separately are as marked.

2. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP210 is connected to a high voltage power source when the test circuit is activated.

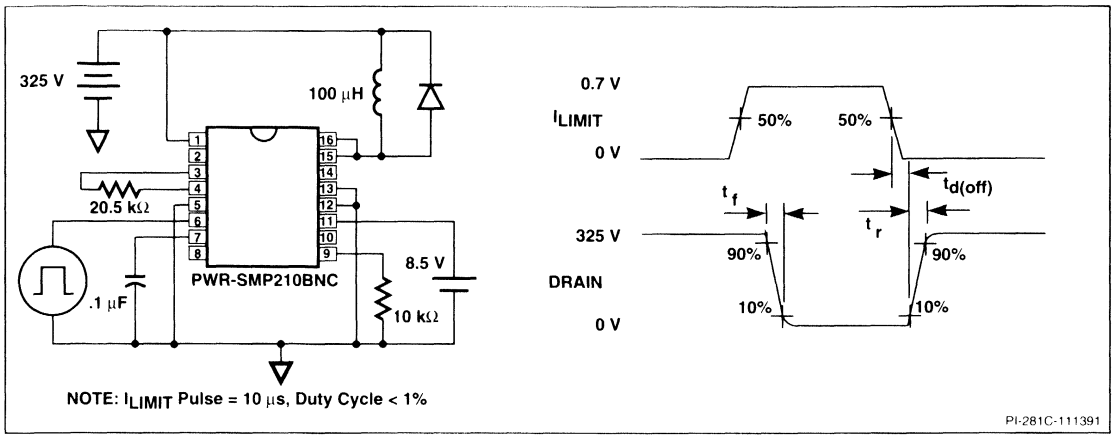
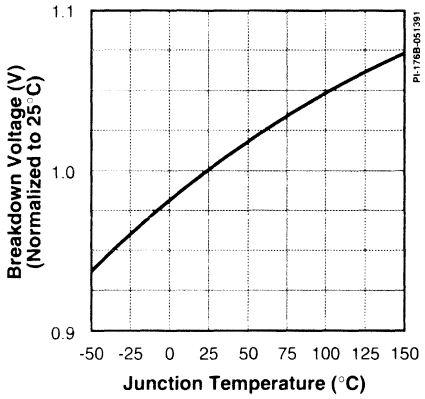
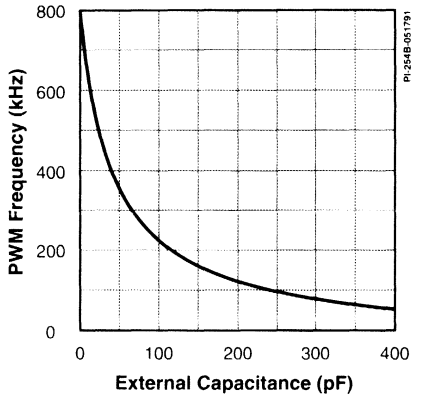


Figure 5. Switching Time Test Circuit.

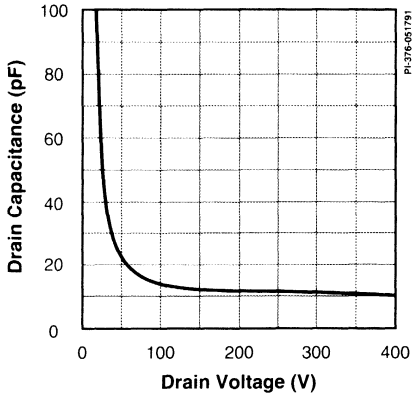
BREAKDOWN vs. TEMPERATURE



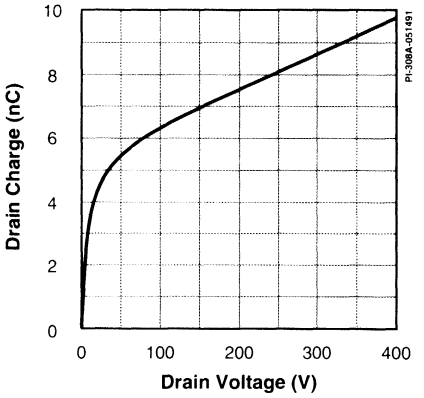
f_{PWM} vs. EXTERNAL CAPACITANCE



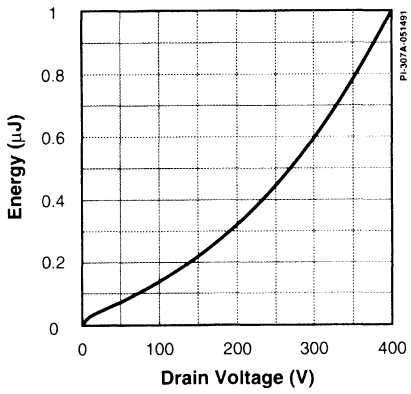
C_{OSS} vs. DRAIN VOLTAGE



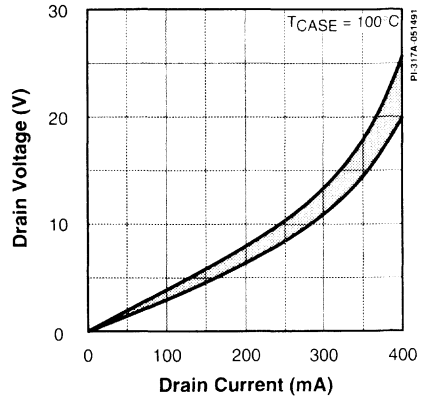
DRAIN CHARGE vs. DRAIN VOLTAGE



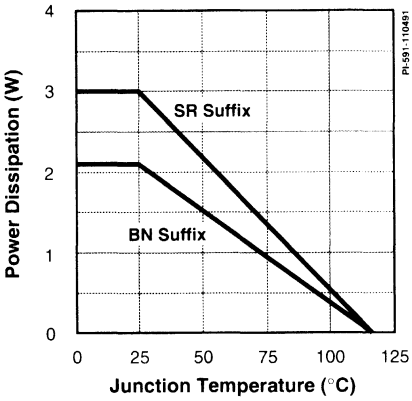
DRAIN CAPACITANCE ENERGY



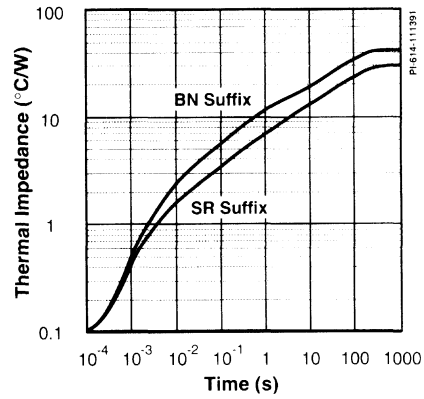
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP211

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from rectified 220 VAC input, 5 W from rectified universal (85 to 265 VAC) input
- External transformer provides isolated output voltages
- Configurable for transformer winding or optocoupler feedback

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Optimized for optocoupler feedback

Built-In Self-protection Circuits
- Cycle-by-cycle current limit
- Latching shutdown feature can be used for output overvoltage protection
- Input undervoltage lockout
- Thermal shutdown

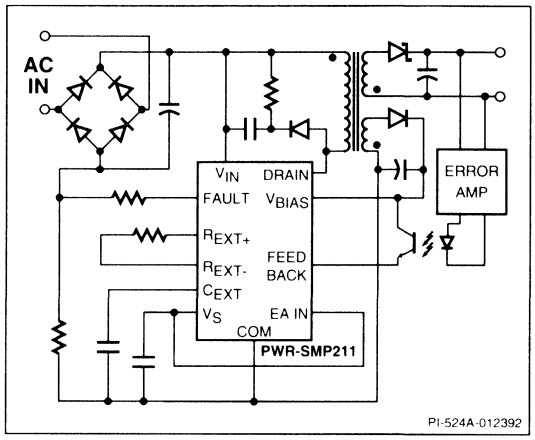


Figure 1. Typical Application

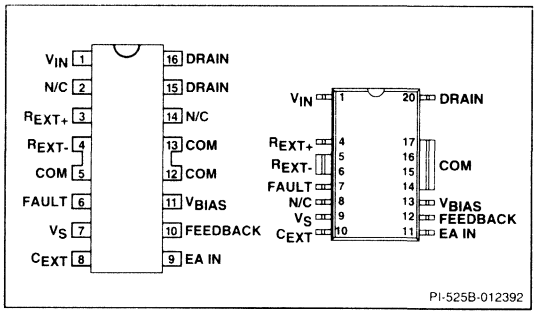


Figure 2. Pin Configuration

Description

The PWR-SMP211, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The PWR-SMP211 has been designed for maximum flexibility in feedback techniques. An error amplifier has been included for use with feedback winding regulation, or it can be bypassed for direct optical feedback to the PWM comparator.

The controller section of the PWR-SMP211 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The PWR-SMP211 is available in a 16-pin plastic batwing DIP or 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP211BNI	16-pin PWR PDIP	-40 to 85°C
PWR-SMP211SRI	20-pin PWR SOIC	-40 to 85°C

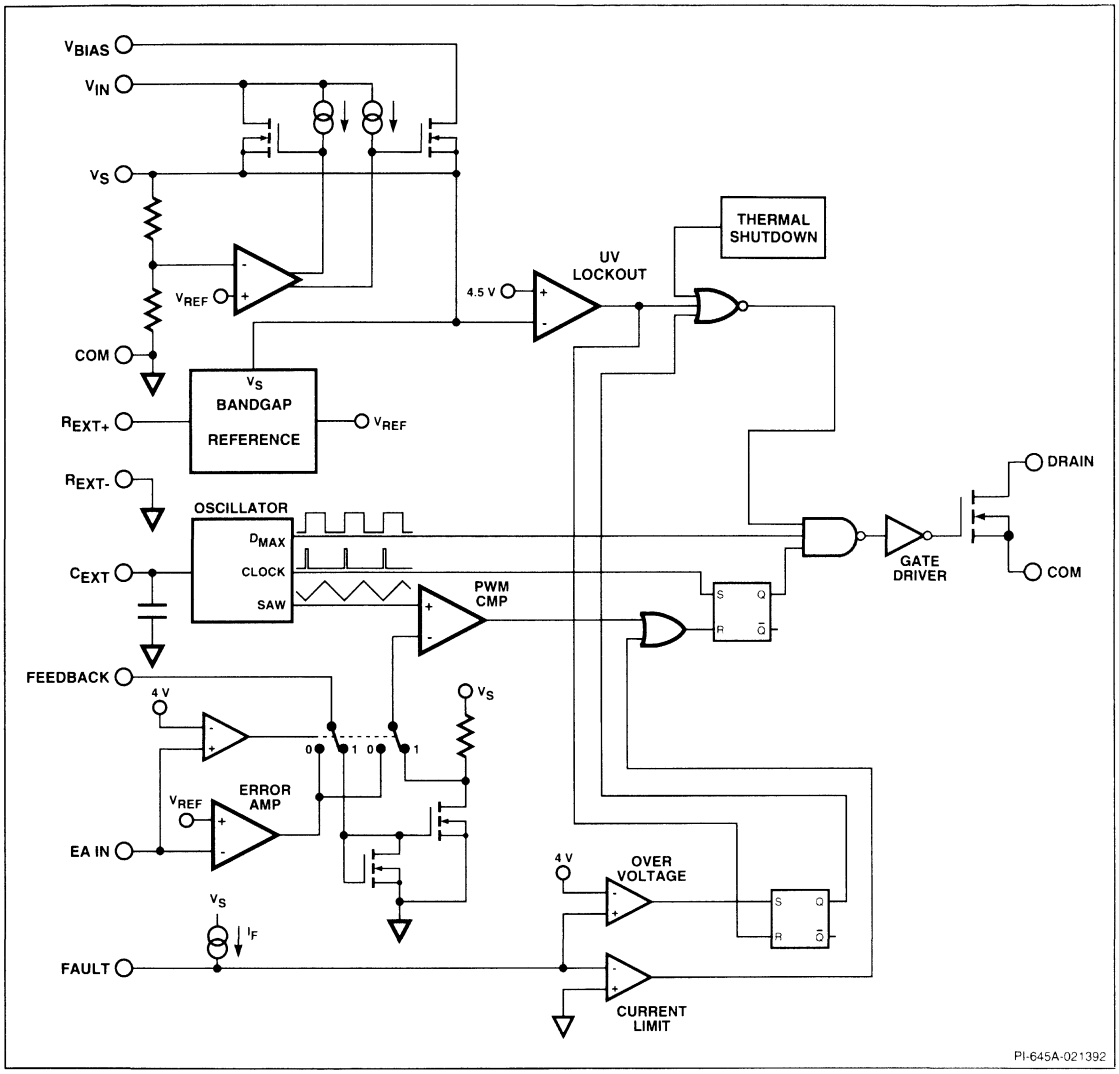


Figure 3. Functional Block Diagram of the PWR-SMP211.

Pin Functional Description

(Pin Number in Parenthes for SOIC version)

Pin 1(1):
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3(4):
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4(5, 6):
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13(14, 15, 16, 17):
COM connections. Ground or reference point for the circuit.

Pin 6(7):
The **FAULT** pin is used with an external resistor to implement current limit. This pin may also driven by an optocoupler to implement over voltage protection of the power supply output.

Pin 7(9):
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8(10):
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9(11):
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks. Connecting this pin to V_S disables the error amplifier when using optocoupler feedback.

Pin 10(12):
FEEDBACK can be driven directly by an optocoupler output, bypassing the internal error amplifier. When using transformer winding feedback control, this pin is used as the error amplifier output for connection to the external compensation network.

Pin 11(13):
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15, 16(20):
Open **DRAIN** of the output MOSFET. Both pins must be externally connected.

1

PWR-SMP211 Functional Description

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the current limit comparator at the beginning of each cycle. The maximum duty cycle is equal to the ratio of the charge time to the total period of the oscillator waveform.

PWR-SMP211 Functional Description (cont.)

Optional Error Amplifier Circuitry

The control loop circuitry is configurable for either secondary-referenced optocoupler control or primary-referenced feedback winding control. In both cases, a control voltage is generated and sent to the pulse width modulator for conversion to a duty cycle.

Connecting the EA IN input to V_S configures the control loop for connection to an external optocoupler. In this mode the internal error amplifier is disabled. The optocoupler output transistor emitter connects directly to FEEDBACK, which is configured as an N-channel MOSFET transistor "diode". This connection presents a low impedance and wide collector-emitter voltage to the optocoupler transistor for improved frequency response and speed. The diode current is converted to the control voltage by a mirror transistor and resistor.

For primary-referenced feedback winding control, the EA IN input is simply connected through a resistor divider to the feedback voltage. The internal error amplifier is automatically configured and connected to the pulse width modulator. EA IN is the inverting input to the error amplifier. The non inverting input is internally connected to the 1.25 V bandgap reference. FEEDBACK is connected to an external feedback compensation network for tailoring the frequency response for proper bandwidth, gain margins, and phase margins.

Pulse Width Modulator

The pulse width modulator implements a voltage mode control loop by driving the power MOSFET with a duty cycle proportional to a control voltage. The duty cycle signal is generated by a comparator which compares the control voltage with a sawtooth waveform. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the driver.

Fault Protection

The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output overvoltage protection.

For cycle-by-cycle current limiting, a COM (ground) referenced comparator senses the voltage at the FAULT pin which is determined by the FAULT current source, external resistors, and the MOSFET current. When the voltage at FAULT reaches or goes below COM, the current limit comparator resets the pulse width modulator latch which turns off the power MOSFET until the start of the next switching cycle.

For latching overvoltage protection, an external optocoupler is used to drive the FAULT pin above the 4V threshold of the overvoltage comparator. This comparator sets a latch that will turn off the power MOSFET until the latch is reset by removing and restoring input power.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysterisis temperature, normal operation resumes.

5 W Universal Off-line Power Supply with Optocoupler Feedback

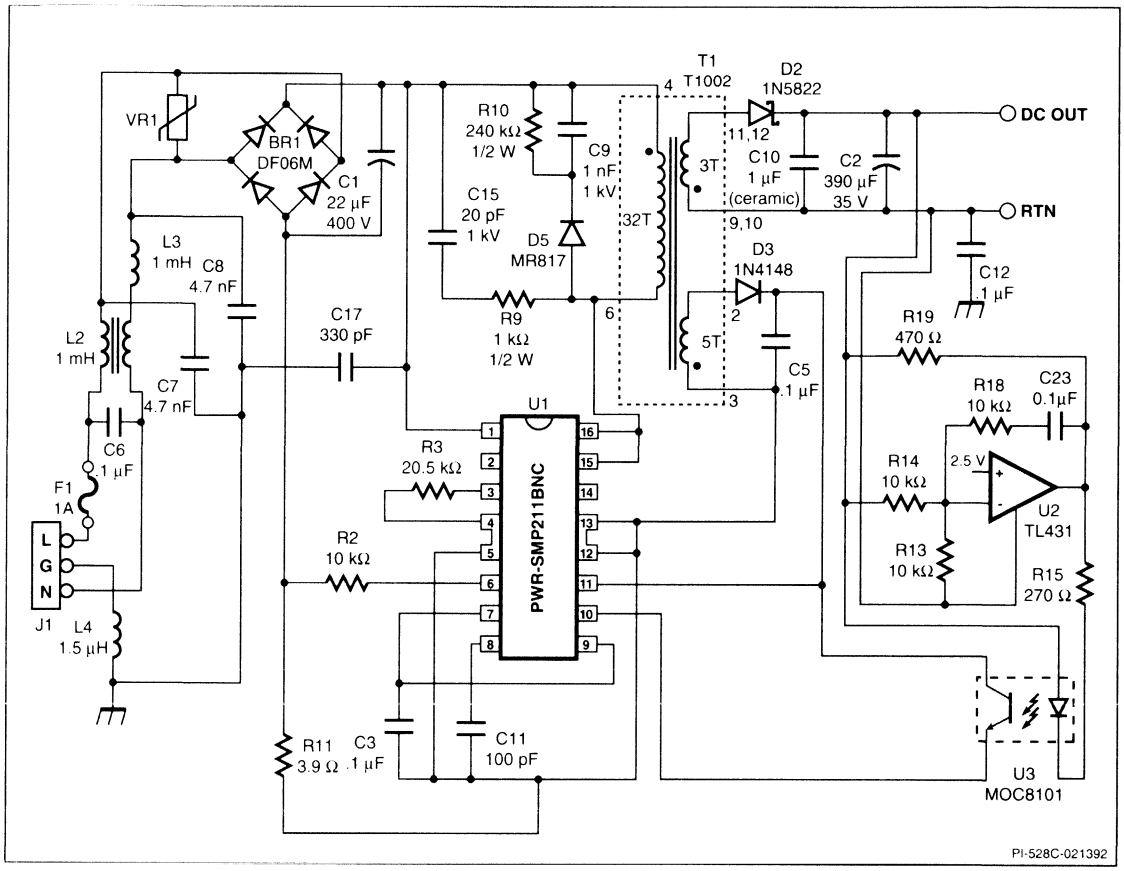


Figure 4. Schematic Diagram of a 5 V, 5 W Universal Input Power Supply Utilizing the PWR-SMP211 with Optocoupler Feedback.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the PWR-SMP211, which directly controls the duty cycle of the integrated high voltage MOSFET switch.

The effective output voltage can be fine-tuned by adjusting the resistive divider formed by R13 and R14. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of transformer T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the PWR-SMP211. The clamp circuit implemented by R10, C9, and D5 clamps the leading edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The power secondary winding is rectified and filtered by D2, C2, and C10 to create the desired output voltage. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the PWR-SMP211 which effectively cuts

General Circuit Operation (cont.)

off the high voltage internal linear regulator. Common mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C12, C17, C7, C8, and L2. Differential mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L3. Voltage spikes on the AC line are clamped by VR1.

Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_S. The oscillator frequency is determined by C11. Transistor switch current is sensed by resistor R11. The initial voltage level at the fault pin is determined by resistor R2.

The secondary-referenced error amplifier control system is implemented with the TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference , error amplifier, and driver. The output voltage is sensed , divided by R13 and R14, and applied to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R18, C23, and the high frequency gain setting resistor R14. Bias current of 2 mA minimum for U2 is provided by resistor R19. The LED current in the optocoupler is limited by resistor R15. Optocoupler U3 drives the error signal into the FEEDBACK pin of the PWR-SMP211. Note that the EA IN pin must be connected to the V_S pin to properly configure the PWR-SMP211 for this type of control.

To achieve full output power and reliable operation of the PWR-SMP211, both DRAIN outputs on the plastic batwing DIP version must be connected together at the printed circuit board. These pins are not connected within the package.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high voltage linear regulator. Ensure that the maximum specified voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

Upgrading Existing PWR-SMP210 Designs to the PWR-SMP211

The PWR-SMP211 is compatible with PC boards designed for the PWR-SMP210. The resistor required between V_S and I_{LIMIT} on the PWR-SMP210 has been eliminated on the PWR-SMP211. The I_{LIMIT} pin on the PWR-SMP210 has been renamed to FAULT on the PWR-SMP211 due to the additional over voltage protection feature. External resistor R2 will have a different value when using the PWR-SMP211.

EA- and EAO on the PWR-SMP210 have been renamed EA IN and FEEDBACK on the PWR-SMP211 because the use of the internal error amplifier is optional. When using primary-referenced feedback winding control the functionality is the same for both devices. An example of this method using the PWR-SMP211 is shown in Figure 5.

Implementing Output Overvoltage Protection

If the load is extremely sensitive to overvoltage conditions, an overvoltage shutdown function can be implemented as shown in Figure 5. The output voltage is fed back to the PWR-SMP211 via an op amp and optocoupler. If the voltage at pin 6 is greater than 4 V, the internal latch will shut off the output. The PWR-SMP211 must be restarted by removing the input voltage and then reapplying it, causing the latch to reset and the circuit to begin a new startup cycle.

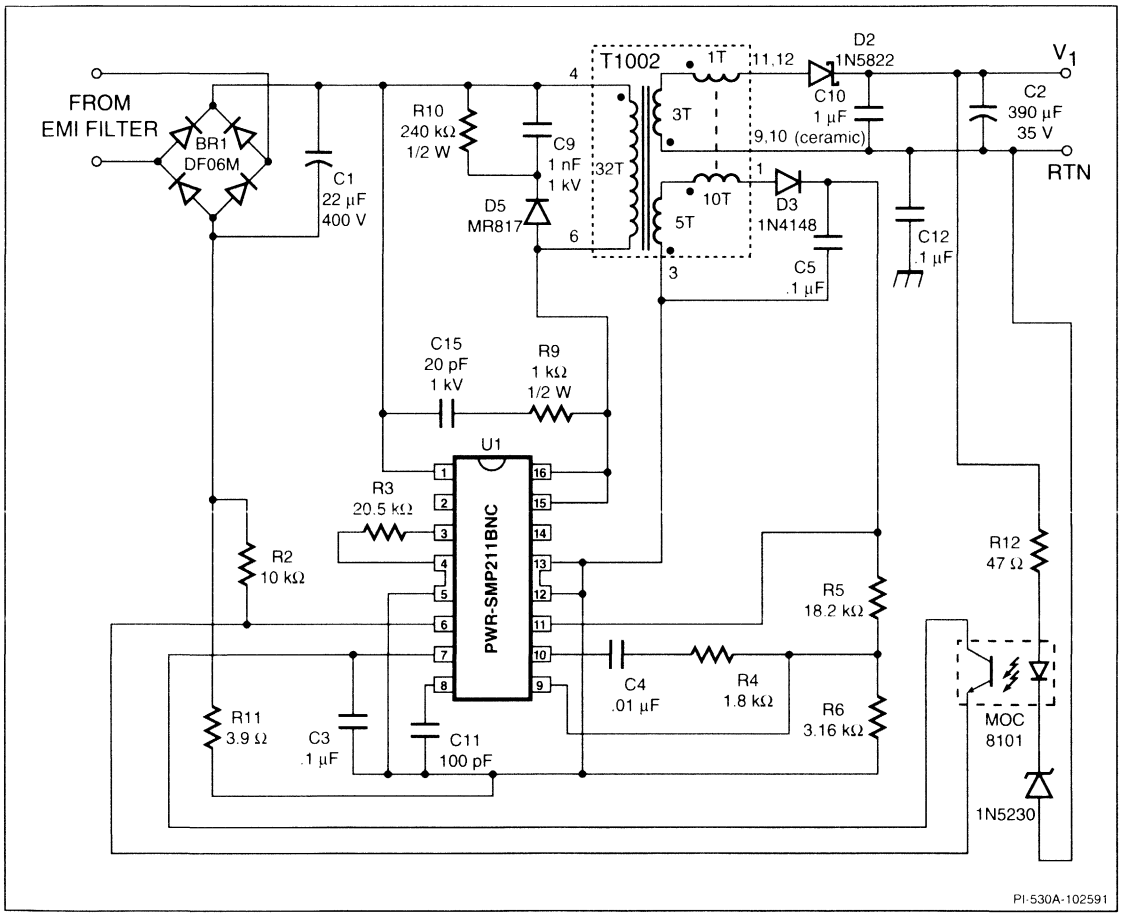


Figure 5. Implementing Feedback Winding Regulation and Output Overvoltage Protection.

ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage ..... 800 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
Drain Current[2] ..... 800 mA
Input Voltage[3] ..... - 0.3 V to V_S + 0.3 V
Storage Temperature ..... -65 to 125°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature[4] ..... 150°C
Lead Temperature[5] ..... 260°C
Power Dissipation
BN Suffix (T_A = 25°C) ..... 2.1 W
(T_A = 70°C) ..... 1.05 W
SR Suffix (T_A = 25°C) ..... 3.0 W
(T_A = 70°C) ..... 1.5 W

Thermal Impedance (θ_{JA})(BN Suffix) ..... 43°C/W
(SR Suffix) ..... 30°C/W
Thermal Impedance (θ_{JC})[6](BN Suffix) ..... 6°C/W
(SR Suffix) ..... 6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 12/13 (BN Suffix), or pin 15/16 (SR Suffix).

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	850	kHz
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
		f_{OSC} = 200 kHz	0-48	0-50		
Optocoupler Output Current	I_C	EA IN = V_S, Maximum Duty Cycle	400		600	µA
Dynamic Control Current	i_C	0 to Maximum Duty Cycle	50	100	200	µA
CIRCUIT PROTECTION						
FAULT Offset Current				100		µA
FAULT OV Threshold	V_{OV}			4		V
FAULT Current Limit Threshold	V_{ILIMIT}			0		V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = -40 to 85°C (See Note 1)		Test Limits MIN	TYP	MAX	Units
CIRCUIT PROTECTION (cont.)							
Current Limit Delay Time	$t_{d(off)}$	See Figure 6		75	150		ns
Thermal Shutdown Temperature				125	140		°C
Thermal Shutdown Hysteresis					15		°C
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product					500		kHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C		20	25	Ω
			T_J = 115°C		33	43	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_J = 25°C	300	380		mA
			T_J = 115°C	200	240		
OFF-State Current	I_{DSS}	V_{DRAIN} = 640 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		800			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			60		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V			800		nJ

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	TYP	MAX	Units
OUTPUT (cont.)						
Rise Time	t_r	See Figure 6		70	150	ns
Fall Time	t_f	See Figure 6		70	150	ns
SUPPLY						
Pre-regulator Voltage	V_{IN}		36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open		3	4.5	mA
		V_{BIAS} > 8.25 V			0.1	
		Thermal Shutdown ON			2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied	8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied		3	4.5	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP211 is connected to a high voltage power source when the test circuit is activated.

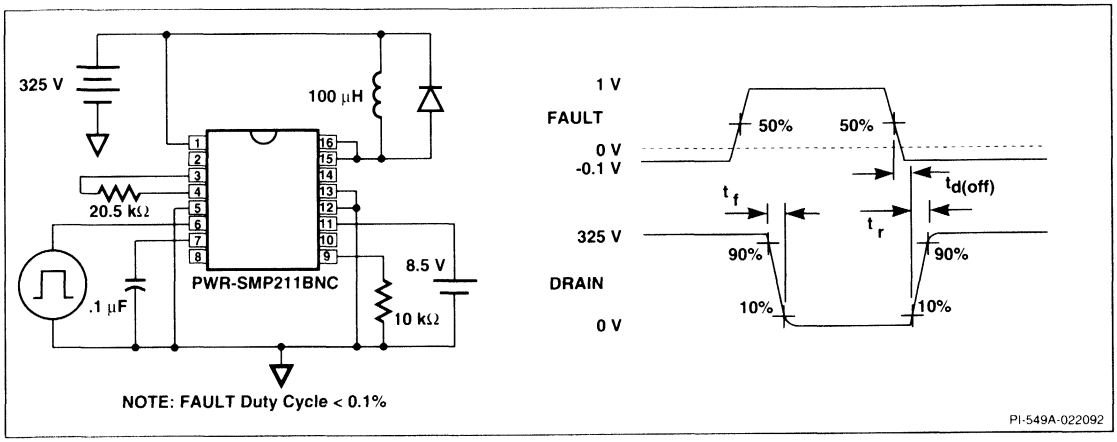
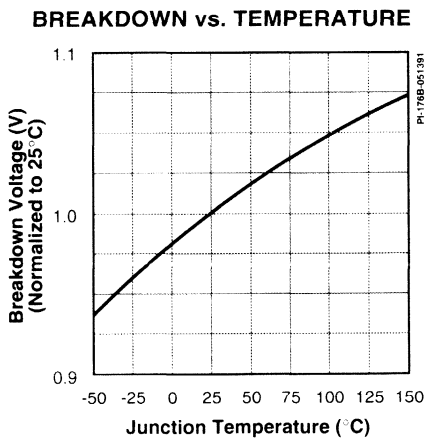
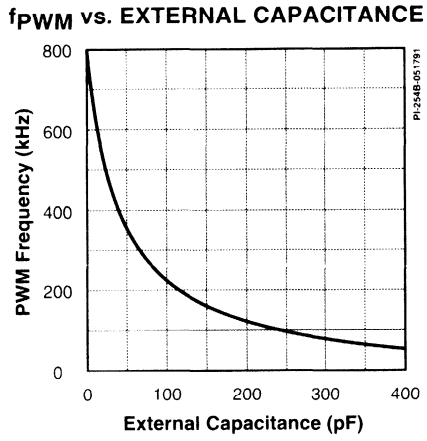
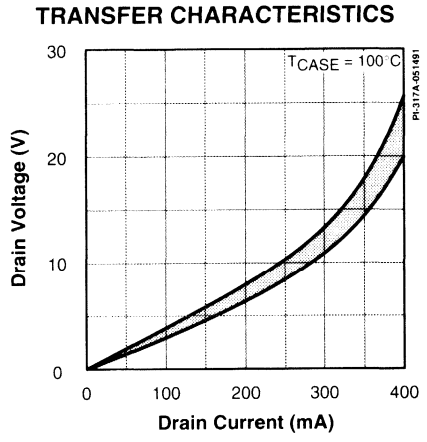


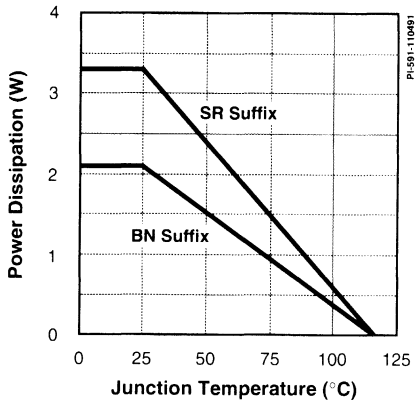
Figure 6. Current Limit Delay/Switching Time Test Circuit.



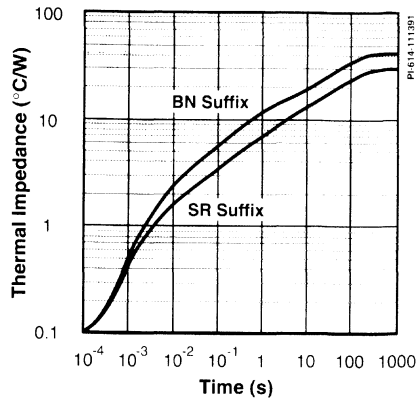




PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP212

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from rectified 220 VAC input, 5 W from rectified universal (85 to 265 VAC) input
- External transformer provides isolated output voltages
- Configurable for transformer winding or optocoupler feedback

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Optimized for optocoupler feedback

Built-In Self-protection Circuits
- Cycle-by-cycle current limit
- Output overvoltage protection
- Shutdown/auto-restart cycling
- Input undervoltage lockout
- Thermal shutdown

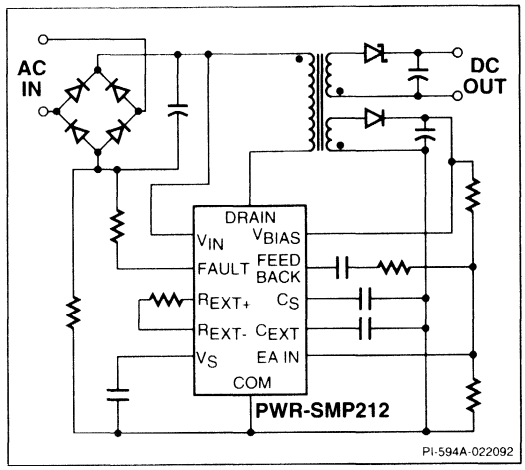


Figure 1. Typical Application

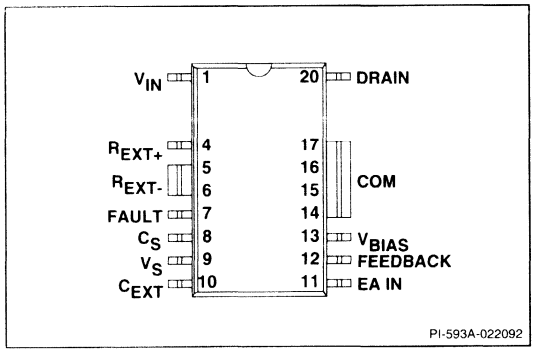


Figure 2. Pin Configuration

Description

The PWR-SMP212, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The PWR-SMP212 has been designed for maximum flexibility in feedback techniques. An error amplifier has been included for use with feedback winding regulation, or it can be bypassed for direct optical feedback to the PWM comparator.

The controller section of the PWR-SMP212 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The PWR-SMP212 is available in a 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP212SRI	20-pin PWR SOIC	-40 to 85°C

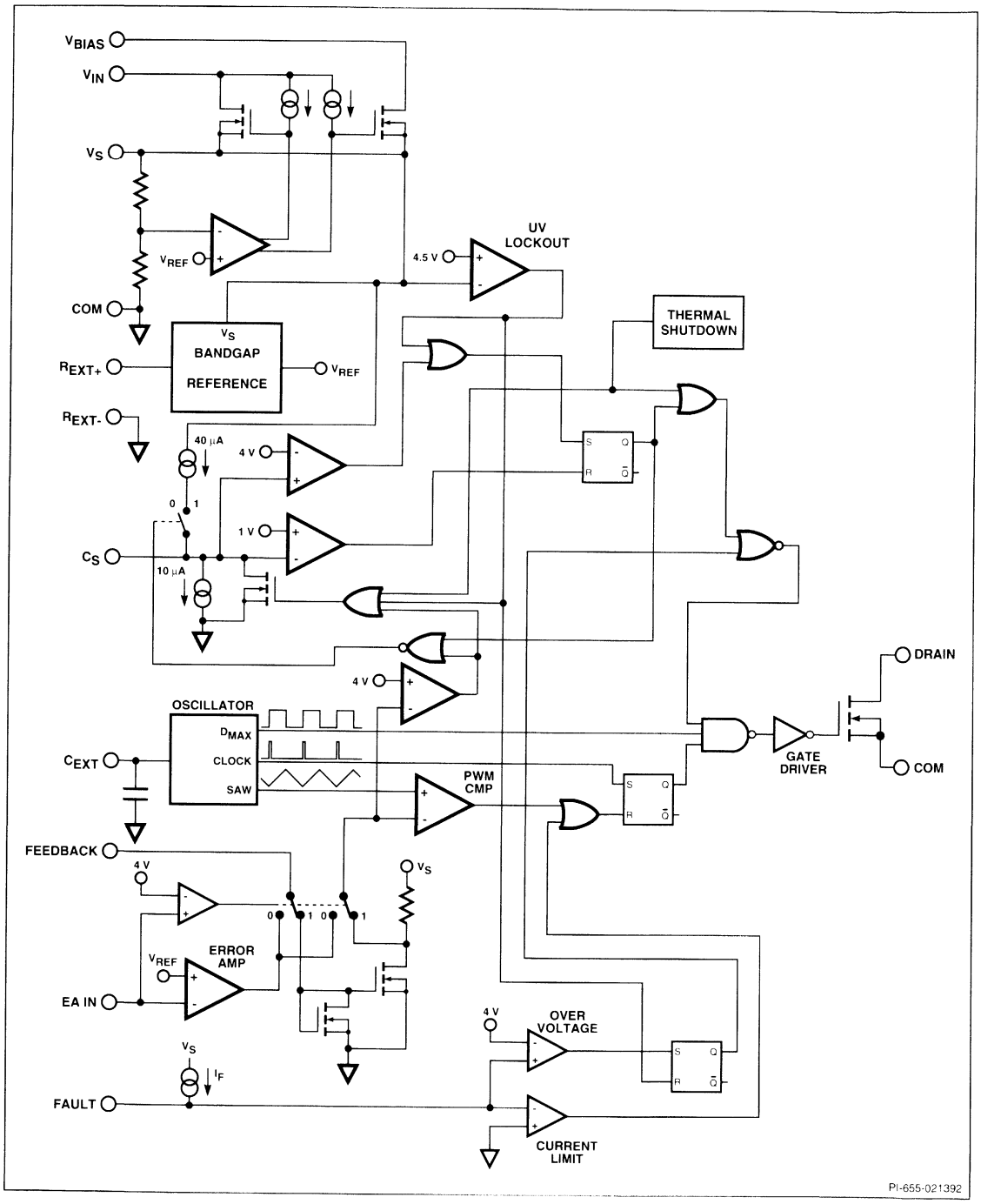


Figure 3. Functional Block Diagram of the PWR-SMP212.

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 4:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 5, 6:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 7:
The **FAULT** pin is used with an external resistor to provide protection of the output during overcurrent and overvoltage conditions.

Pin 8:
C_S is used to set the shutdown/auto-restart cycle time.

Pin 9:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 10:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 11:
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks. Connecting this pin to V_S disables the error amplifier when using optocoupler feedback.

Pin 12:
FEEDBACK can be driven directly by an optocoupler output, bypassing the internal error amplifier. When using transformer winding feedback control, this pin is used as the error amplifier output for connection to the external compensation network.

Pin 13:
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14, 15, 16, 17:
COM connections. Ground or reference point for the circuit.

Pin 20:
Open **DRAIN** of the output MOSFET.

1

PWR-SMP212 Functional Description

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the current limit comparator at the beginning of each cycle. The maximum duty cycle is equal to the ratio of the charge time to the total period of the oscillator waveform.

PWR-SMP212 Functional Description (cont.)

Optional Error Amplifier Circuitry
The control loop circuitry is configurable for either secondary-referenced optocoupler control or primary-referenced feedback winding control. In both cases, a control voltage is generated and sent to the pulse width modulator for conversion to a duty cycle.

Connecting the EA IN input to V_S configures the control loop for connection to an external optocoupler. In this mode the internal error amplifier is disabled. The optocoupler output transistor emitter connects directly to FEEDBACK, which is configured as an N-channel MOSFET transistor "diode". This connection presents a low impedance and wide collector-emitter voltage to the optocoupler transistor for improved frequency response and speed. The diode current is converted to the control voltage by a mirror transistor and resistor.

For primary-referenced feedback winding control, the EA IN input is simply connected through a resistor divider to the feedback voltage. The internal error amplifier is automatically configured and connected to the pulse width modulator. EA IN is the inverting input to the error amplifier. The non inverting input is internally connected to the 1.25 V bandgap reference. FEEDBACK is connected to an external feedback compensation network for tailoring the frequency response for proper bandwidth, gain margins, and phase margins.

Pulse Width Modulator
The pulse width modulator implements a voltage mode control loop by driving the power MOSFET with a duty cycle proportional to a control voltage. The duty cycle signal is generated by a comparator which compares the control voltage with a sawtooth waveform. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the driver.

Fault Protection
The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output overvoltage protection.

The FAULT pin latches off the power switch when an overcurrent condition causes the voltage on this pin to drop to zero. The DRAIN current is sensed by an external resistor. An internal current source biases the FAULT signal during normal operation. During an overcurrent condition, current flows in the current sense resistor, causing the voltage on the FAULT pin to decrease. If the voltage on the FAULT pin falls below COM for longer than the delay time, the power switch will be latched off until the beginning of the next clock cycle. If this condition persists, the output voltage will fall out of regulation, triggering a shutdown/auto-restart cycle.

For latching overvoltage protection, an external optocoupler can be used to drive the FAULT pin above the 4 V threshold of the overvoltage comparator. This comparator sets a latch that will turn off the power MOSFET until the latch is reset by removing and restoring input power.

Shutdown/Auto-restart
The PWR-SMP212 contains an auto-restart function which will shut off the power supply if the output voltage falls out of regulation. The PWR-SMP212 will try to restart and will test the output after a delay. The PWR-SMP212 will remain shut off for the amount of time determined by the value of C_S, and will then begin the auto-restart cycle. The power supply will resume normal operation if the fault condition has been removed. The power supply will continuously cycle if the output is not regulated within the turn-on delay as determined by C_S. During normal operation, C_S is quickly discharged to 0 V. This function can be disabled by connecting the C_S pin to COM.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysterisis temperature, normal operation resumes.

5 W Universal Off-line Power Supply with Optocoupler Feedback

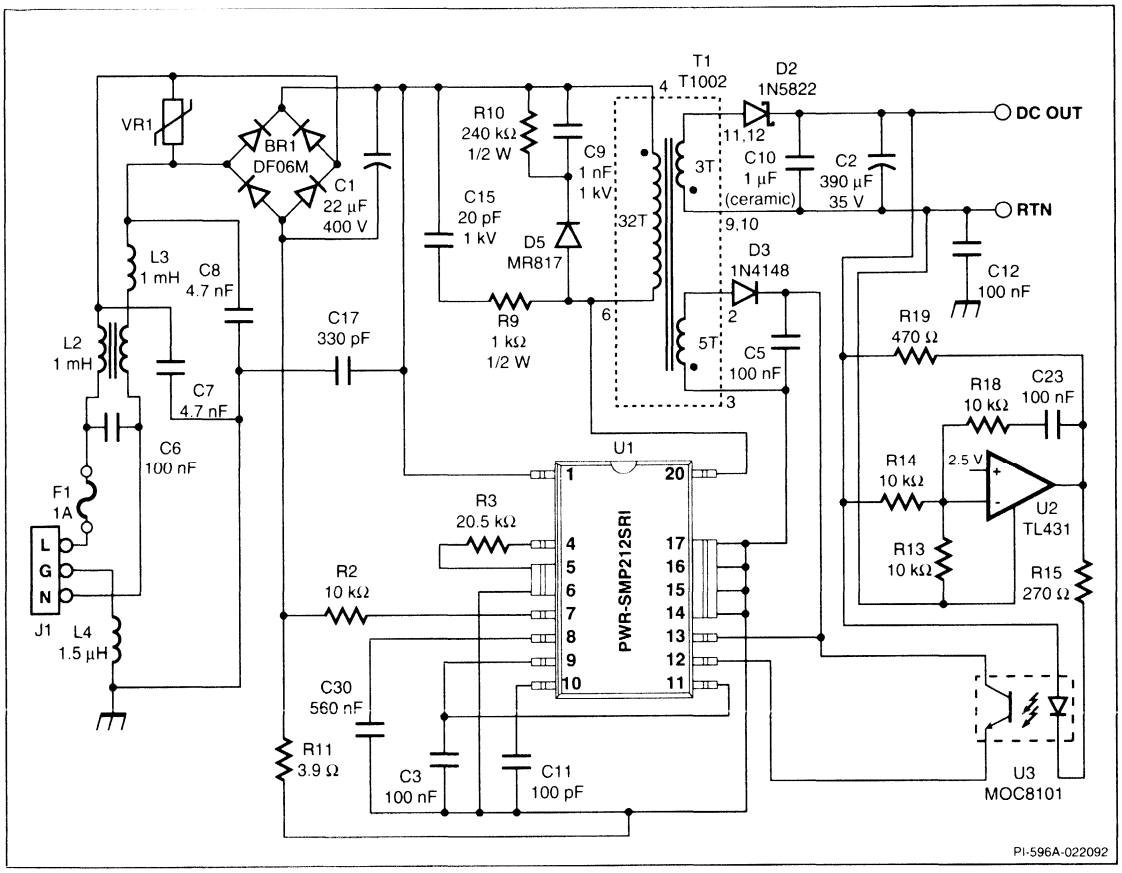


Figure 4. Schematic Diagram of a 5 V, 5 W Universal Input Power Supply Utilizing the PWR-SMP212.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the PWR-SMP212, which directly controls the duty cycle of the integrated high voltage MOSFET switch.

The effective output voltage can be fine-tuned by adjusting the resistive divider formed by R13 and R14. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of transformer T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the PWR-SMP212. The clamp circuit implemented by R10, C9, and D5 clamps the leading edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The power secondary winding is rectified and filtered by D2, C2A, C2B, and C10 to create the desired output voltage. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the PWR-SMP212, which

General Circuit Operation (cont.)

effectively cuts off the high voltage internal linear regulator. Common mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C12, C17, C7, C8, and L2. Differential mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L3. Voltage spikes on the AC line are clamped by VR1.

Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_S. The oscillator frequency is determined by C11. Transistor switch current is sensed by resistor R11. The initial voltage level at the fault pin is determined by resistor R2. C30 determines the auto-restart time interval.

The secondary-referenced error amplifier control system is implemented with the TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference , error amplifier, and driver. The output voltage is sensed , divided by R13 and R14, and applied to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R18, C23, and the high frequency gain setting resistor R14. Bias current of 2 mA minimum for U2 is provided by resistor R19. The LED current in the optocoupler is limited by resistor R15. Optocoupler U3 drives the error signal into the FEEDBACK pin of the PWR-SMP212. Note that the EA IN pin must be connected to the V_S pin to properly configure the PWR-SMP212 for this type of control.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high voltage linear regulator. Ensure that the maximum specified voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

Implementing Output Overvoltage Protection

If the load is extremely sensitive to overvoltage conditions, an overvoltage shutdown function can be implemented as shown in Figure 5. The output voltage is fed back to the PWR-SMP212 via an op amp and optocoupler. If the voltage at pin 7 is greater than 4 V, the internal latch will shut off the output.

The PWR-SMP212 must be restarted by removing the input voltage and then reapplying it, causing the latch to reset and the circuit to begin a new startup cycle.

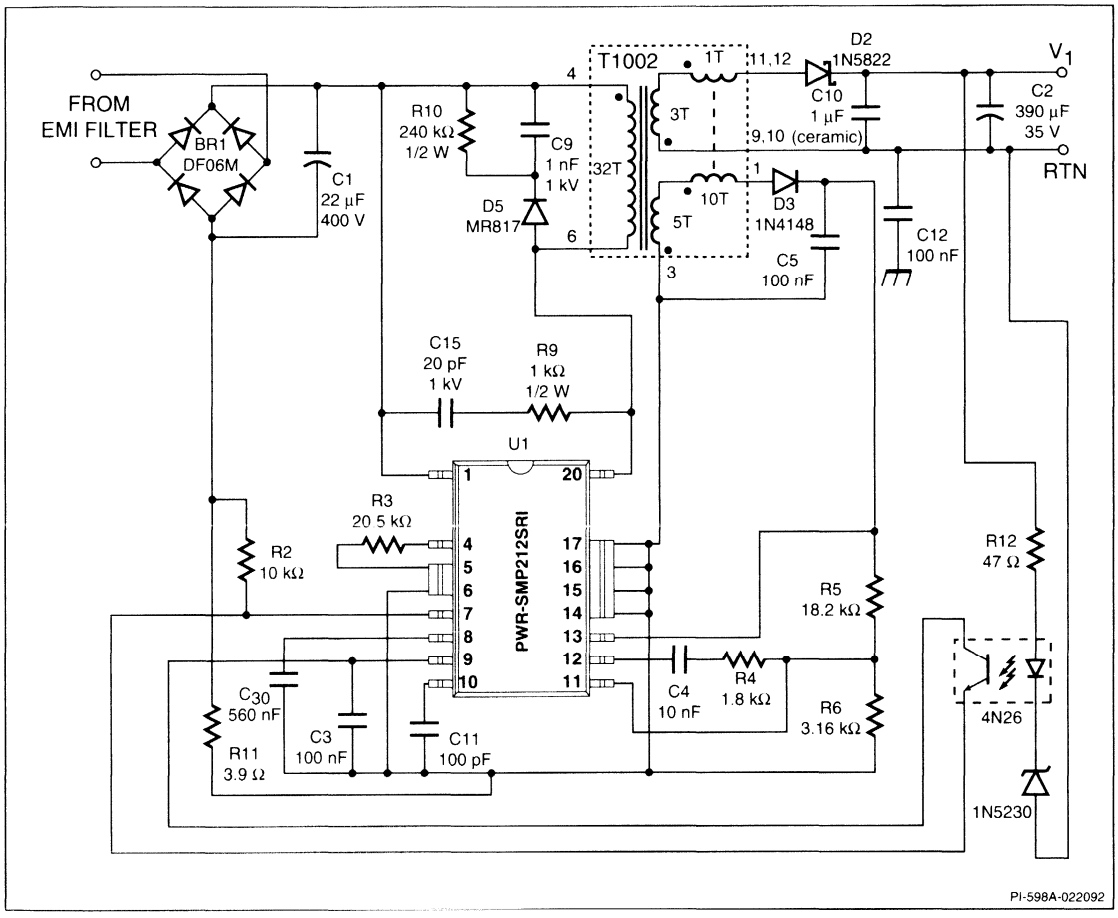


Figure 5. Implementing Feedback Winding Regulation and Output Overvoltage Protection.

ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	800 V
V_{IN} Voltage	500 V
V_{BIAS} Voltage	35 V
Drain Current[2]	800 mA
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	-65 to 125°C
Ambient Temperature	-40 to 85°C
Junction Temperature[4]	150°C
Lead Temperature[5]	260°C
Power Dissipation (T_A = 25°C)	3.0 W
(T_A = 70°C)	1.5 W
Thermal Impedance (θ_{JA})	30°C/W
Thermal Impedance (θ_{JC})[6]	6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 15/16.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	850	kHz
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
		f_{OSC} = 200 kHz	0-48	0-50		
Optocoupler Output Current	I_C	EA IN = V_S, Maximum Duty Cycle	400		600	µA
Dynamic Control Current	i_C	0 to Maximum Duty Cycle	50	100	200	µA
CIRCUIT PROTECTION						
FAULT Offset Current				100		µA
FAULT OV Threshold	V_{OV}			4		V
FAULT Current Limit Threshold	V_{ILIMIT}			0		V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
CIRCUIT PROTECTION (cont.)						
Current Limit Delay Time	$t_{d(off)}$	See Figure 6	75	150	250	ns
Thermal Shutdown Temperature			125	140		°C
Thermal Shutdown Hysteresis				15		°C
SHUTDOWN/AUTO-RESTART						
ON Time	t_{ON}	See Figure 7		38		ms
OFF Time	t_{OFF}	See Figure 7		150		ms
Reset Time	t_{RESET}	See Figure 7		12.5		ms
Charge/Discharge Ratio				4:1		
Upper Threshold Voltage	V_{THU}			4.0		V
Lower Threshold Voltage	V_{THL}			1.0		V
ERROR AMPLIFIER						
Reference Voltage	V_{REF}		1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}			50		ppm/°C
Gain-Bandwidth Product				500		kHz
DC Gain	A_{VOL}		60	80		dB
Output Impedance	Z_{OUT}			1.5		kΩ

1

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT (cont.)							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C		20	25	Ω
			T_J = 115°C		33	43	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_J = 25°C	300	380		A
			T_J = 115°C	200	240		
OFF-State Current	I_{DSS}	V_{DRAIN} = 640 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		800			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			60		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V			800		nJ
Rise Time	t_r	See Figure 6			70	150	ns
Fall Time	t_f	See Figure 6			70	150	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open			3	4.5	mA
		V_{BIAS} > 8.25 V				0.1	
		Thermal Shutdown ON				2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied		8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied			3	4.5	mA
V_S Source Voltage	V_S			5.1		6.0	V
V_S Source Current	I_S					400	µA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP212 is connected to a high voltage power source when the test circuit is activated.

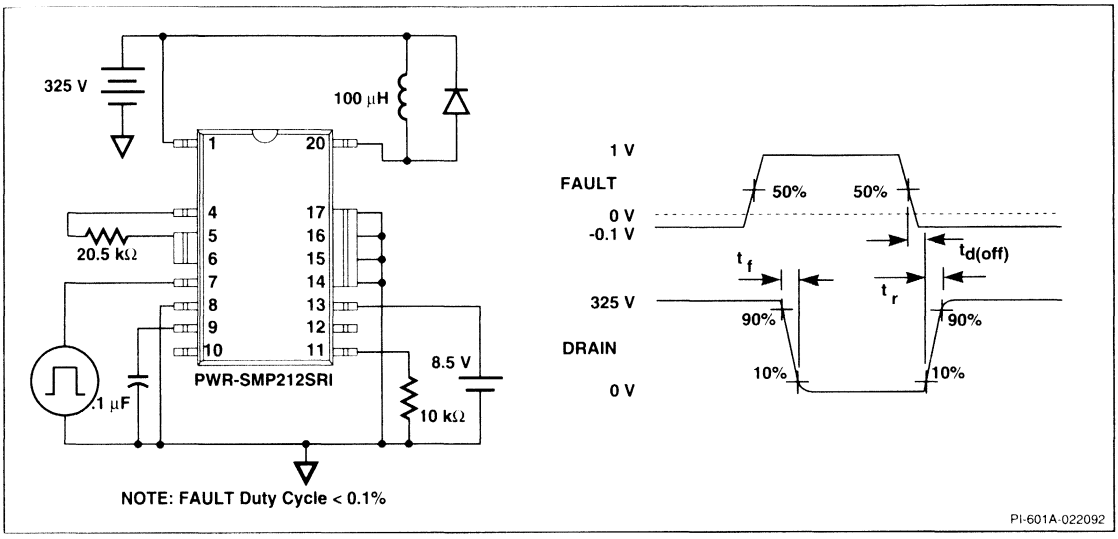


Figure 6. Current Limit Delay/Switching Time Test Circuit.

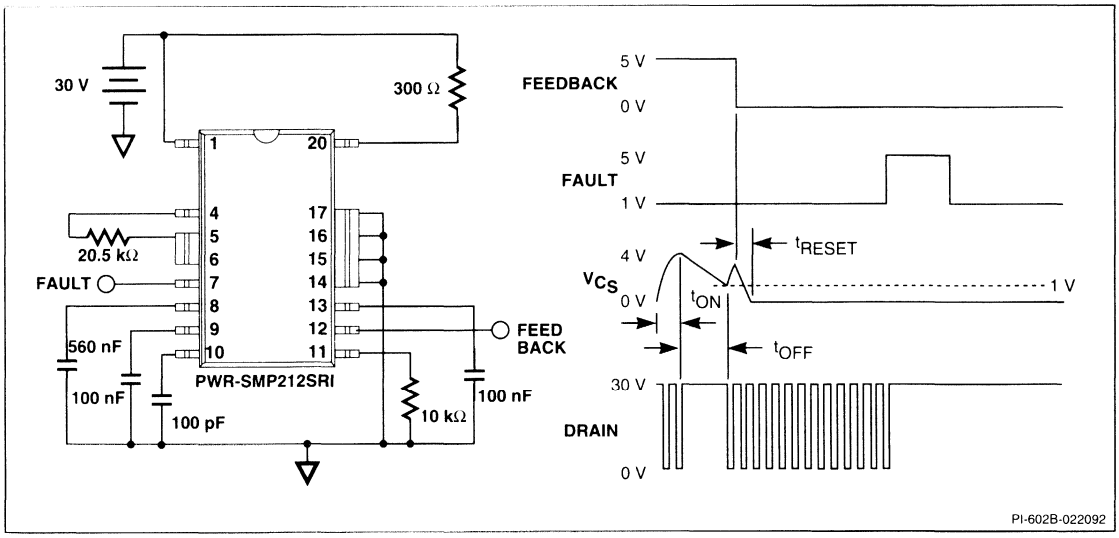
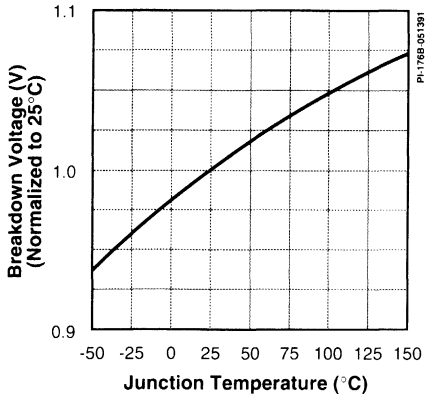
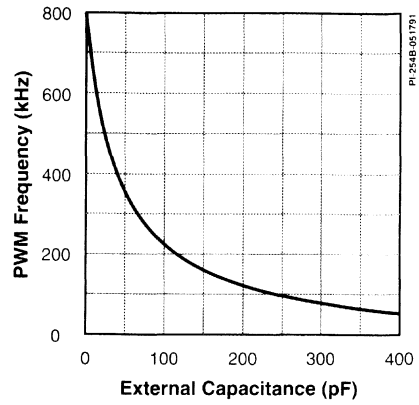


Figure 7. Auto-restart Test Circuit.

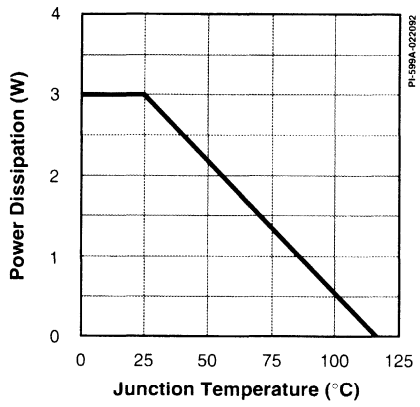
BREAKDOWN vs. TEMPERATURE



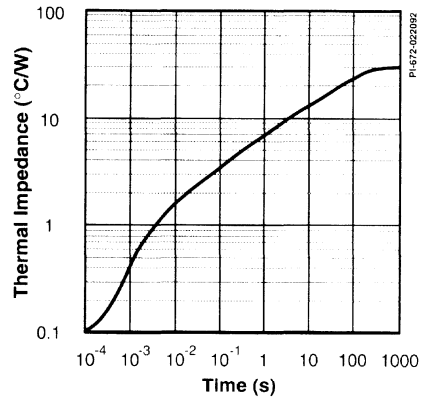
f_{PWM} vs. EXTERNAL CAPACITANCE



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP220

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 20 W from rectified 220 VAC input, 12 W from rectified universal (85 to 265 VAC) input
- External transformer provides isolated output voltages
- Configurable for transformer winding or optocoupler feedback

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Optimized for optocoupler feedback

Built-In Self-protection Circuits
- Cycle-by-cycle current limit
- Output overvoltage protection
- Shutdown/auto-restart cycling
- Input undervoltage lockout
- Thermal shutdown

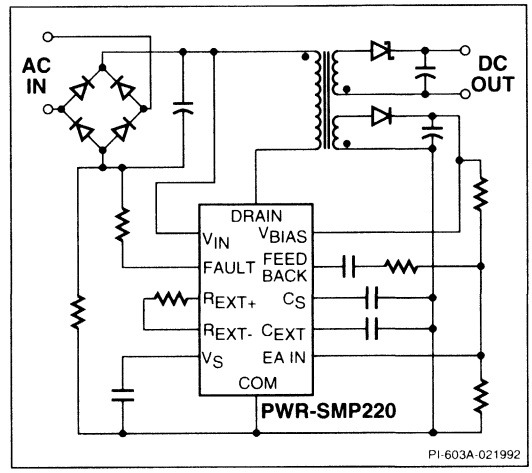


Figure 1. Typical Application

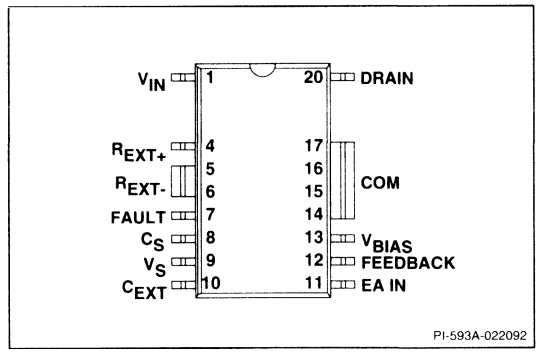


Figure 2. Pin Configuration

Description

The PWR-SMP220, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The PWR-SMP220 has been designed for maximum flexibility in feedback techniques. An error amplifier has been included for use with feedback winding regulation, or it can be bypassed for direct optical feedback to the PWM comparator.

The controller section of the PWR-SMP220 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The PWR-SMP220 is available in a 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP220SRI	20-pin PWR SOIC	-40 to 85°C

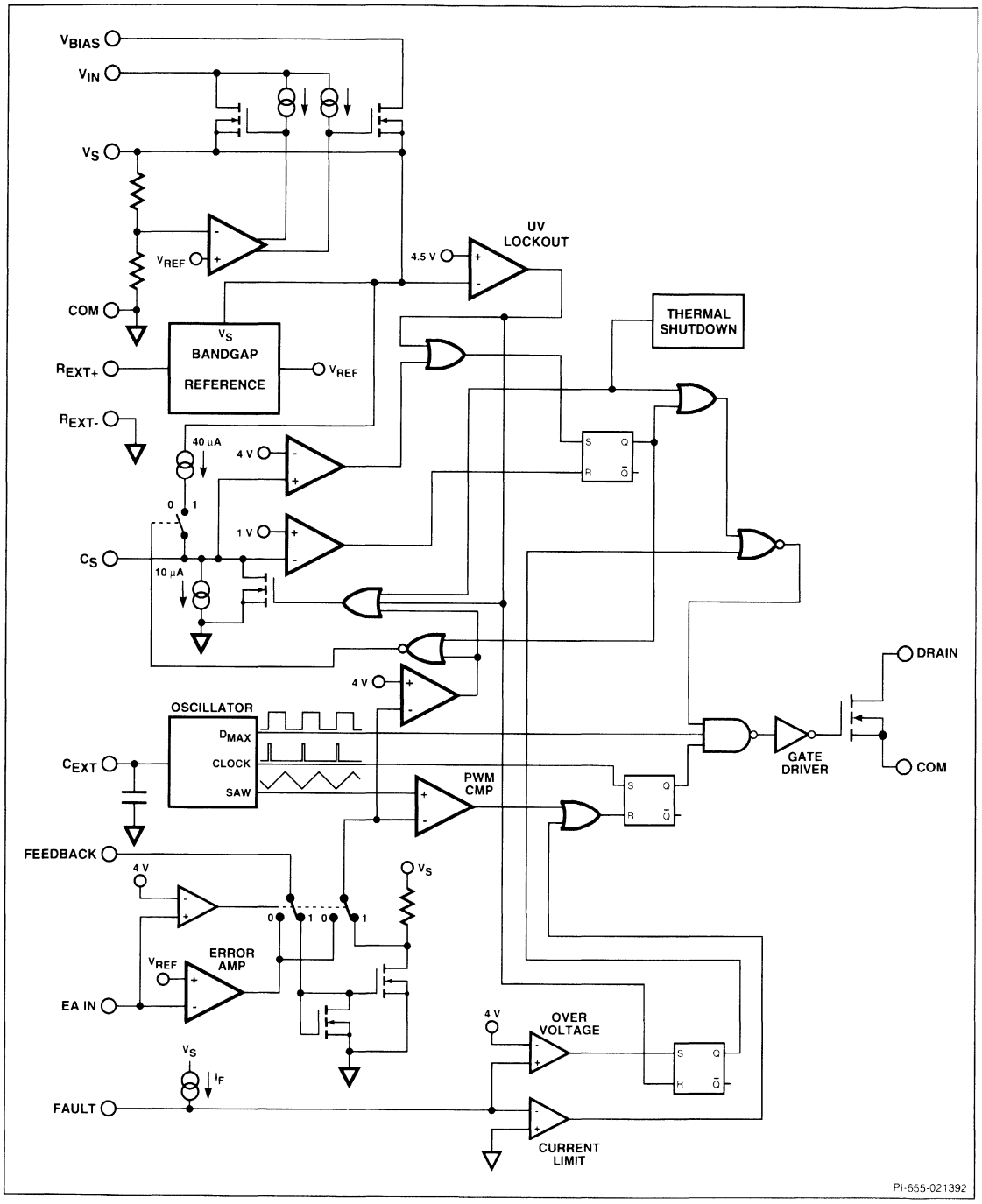


Figure 3. Functional Block Diagram of the PWR-SMP220.

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 4:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 5, 6:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 7:
The **FAULT** pin is used with an external resistor to provide protection of the output during overcurrent and overvoltage conditions.

Pin 8:
C_S is used to set the shutdown/auto-restart cycle time.

Pin 9:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 10:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 11:
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks. Connecting this pin to V_S disables the error amplifier when using optocoupler feedback.

Pin 12:
FEEDBACK can be driven directly by an optocoupler output, bypassing the internal error amplifier. When using transformer winding feedback control, this pin is used as the error amplifier output for connection to the external compensation network.

Pin 13:
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14, 15, 16, 17:
COM connections. Ground or reference point for the circuit.

Pin 20:
Open **DRAIN** of the output MOSFET.

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PWR-SMP220 Functional Description

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the current limit comparator at the beginning of each cycle. The maximum duty cycle is equal to the ratio of the charge time to the total period of the oscillator waveform.

PWR-SMP220 Functional Description (cont.)

Optional Error Amplifier Circuitry
The control loop circuitry is configurable for either secondary-referenced optocoupler control or primary-referenced feedback winding control. In both cases, a control voltage is generated and sent to the pulse width modulator for conversion to a duty cycle.

Connecting the EA IN input to V_S configures the control loop for connection to an external optocoupler. In this mode the internal error amplifier is disabled. The optocoupler output transistor emitter connects directly to FEEDBACK, which is configured as an N-channel MOSFET transistor "diode". This connection presents a low impedance and wide collector-emitter voltage to the optocoupler transistor for improved frequency response and speed. The diode current is converted to the control voltage by a mirror transistor and resistor.

For primary-referenced feedback winding control, the EA IN input is simply connected through a resistor divider to the feedback voltage. The internal error amplifier is automatically configured and connected to the pulse width modulator. EA IN is the inverting input to the error amplifier. The non inverting input is internally connected to the 1.25 V bandgap reference. FEEDBACK is connected to an external feedback compensation network for tailoring the frequency response for proper bandwidth, gain margins, and phase margins.

Pulse Width Modulator
The pulse width modulator implements a voltage mode control loop by driving the power MOSFET with a duty cycle proportional to a control voltage. The duty cycle signal is generated by a comparator which compares the control voltage with a sawtooth waveform. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the driver.

Fault Protection
The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output overvoltage protection.

The FAULT pin latches off the power switch when an overcurrent condition causes the voltage on this pin to drop to zero. The DRAIN current is sensed by an external resistor. An internal current source biases the FAULT signal during normal operation. During an overcurrent condition, current flows in the current sense resistor, causing the voltage on the FAULT pin to decrease. If the voltage on the FAULT pin falls below COM for longer than the delay time, the power switch will be latched off until the beginning of the next clock cycle. If this condition persists, the output voltage will fall out of regulation, triggering a shutdown/auto-restart cycle.

For latching overvoltage protection, an external optocoupler can be used to drive the FAULT pin above the 4 V threshold of the overvoltage comparator. This comparator sets a latch that will turn off the power MOSFET until the latch is reset by removing and restoring input power.

Shutdown/Auto-restart
The PWR-SMP220 contains an auto-restart function which will shut off the power supply if the output voltage falls out of regulation. The PWR-SMP220 will try to restart and will test the output after a delay. The PWR-SMP220 will remain shut off for the amount of time determined by the value of C_S, and will then begin the auto-restart cycle. The power supply will resume normal operation if the fault condition has been removed. The power supply will continuously cycle if the output is not regulated within the turn-on delay as determined by C_S. During normal operation, C_S is quickly discharged to 0 V. This function can be disabled by connecting the C_S pin to COM.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysterisis temperature, normal operation resumes.

12 W Universal Off-line Power Supply with Optocoupler Feedback

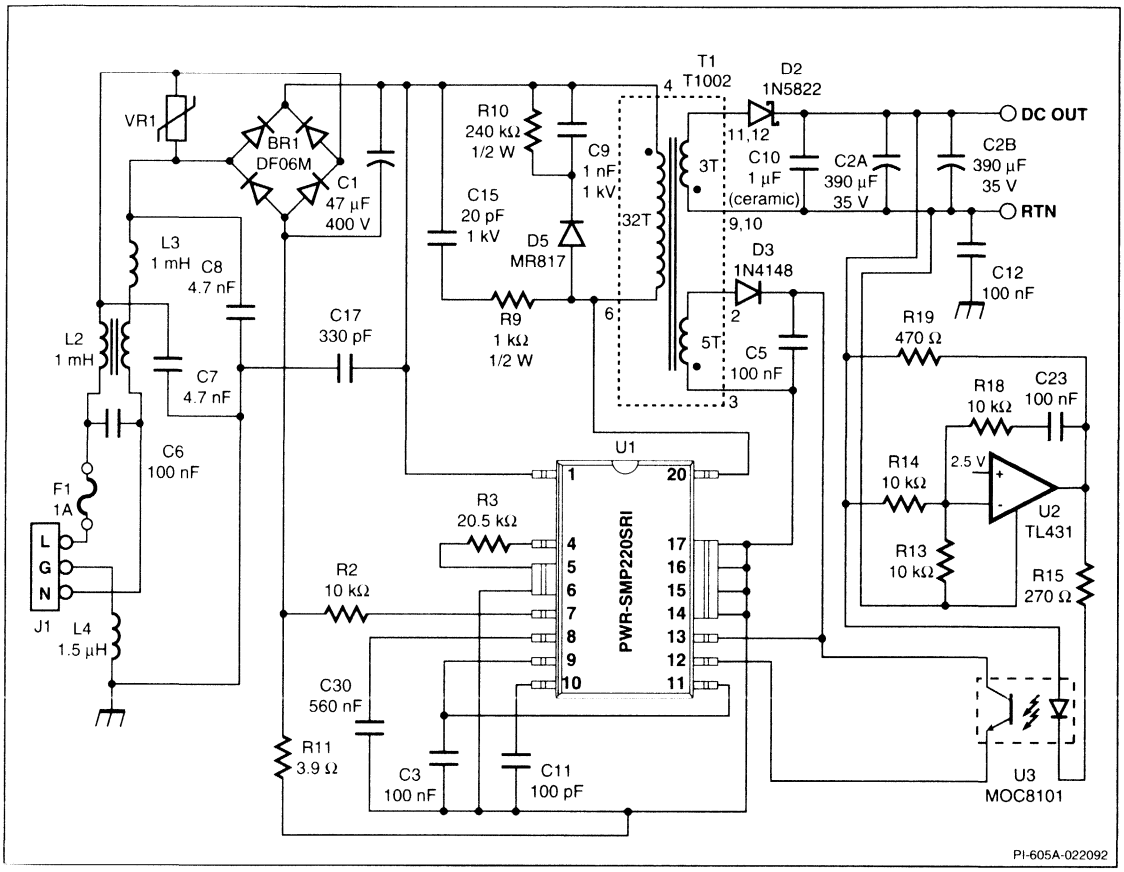

Figure 4. Schematic Diagram of a 5 V, 12 W Universal Input Power Supply Utilizing the PWR-SMP220.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 12 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the PWR-SMP220, which directly controls the duty cycle of the integrated high voltage MOSFET switch.

The effective output voltage can be fine-tuned by adjusting the resistive divider formed by R13 and R14. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of transformer T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the PWR-SMP220. The clamp circuit implemented by R10, C9, and D5 clamps the leading edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The power secondary winding is rectified and filtered by D2, C2A, C2B, and C10 to create the desired output voltage. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the PWR-SMP220, which

General Circuit Operation (cont.)

effectively cuts off the high voltage internal linear regulator. Common mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C12, C17, C7, C8, and L2. Differential mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L3. Voltage spikes on the AC line are clamped by VR1.

Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_S. The oscillator frequency is determined by C11. Transistor switch current is sensed by resistor R11. The initial voltage level at the fault pin is determined by resistor R2. C30 determines the auto-restart time interval.

The secondary-referenced error amplifier control system is implemented with the TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference , error amplifier, and driver. The output voltage is sensed , divided by R13 and R14, and applied to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R18, C23, and the high frequency gain setting resistor R14. Bias current of 2 mA minimum for U2 is provided by resistor R19. The LED current in the optocoupler is limited by resistor R15. Optocoupler U3 drives the error signal into the FEEDBACK pin of the PWR-SMP220. Note that the EA IN pin must be connected to the V_S pin to properly configure the PWR-SMP220 for this type of control.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high voltage linear regulator. Ensure that the maximum specified voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

Implementing Output Overvoltage Protection

If the load is extremely sensitive to overvoltage conditions, an overvoltage shutdown function can be implemented as shown in Figure 5. The output voltage is fed back to the PWR-SMP220 via an op amp and optocoupler. If the voltage at pin 7 is greater than 4 V, the internal latch will shut off the output.

The PWR-SMP220 must be restarted by removing the input voltage and then reapplying it, causing the latch to reset and the circuit to begin a new startup cycle.

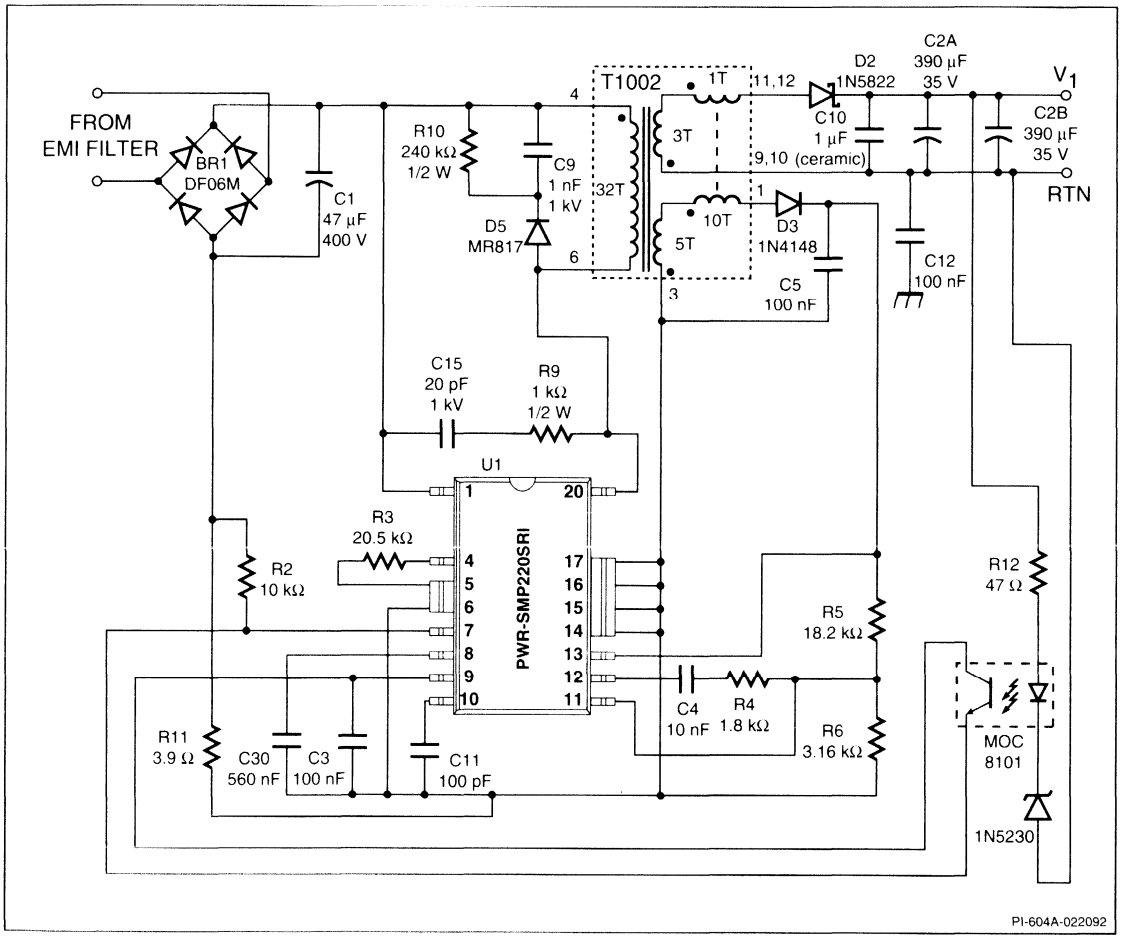

Figure 5. Implementing Feedback Winding Regulation and Output Overvoltage Protection.

ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	700 V
V_{IN} Voltage	500 V
V_{BIAS} Voltage	35 V
Drain Current[2]	1.3 A
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 125°C
Ambient Temperature	-40 to 85°C
Junction Temperature[4]	150°C
Lead Temperature[5]	260°C
Power Dissipation (T_A = 25°C)	3.0 W
(T_A = 70°C)	1.5 W
Thermal Impedance (θ_{JA})	30°C/W
Thermal Impedance (θ_{JC})[6]	6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 15/16.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT} = 20.5 kΩ, C_S = 560 nF T_A = -40 to 85°C (See Note 1)	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	750	850	kHz
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
		f_{OSC} = 200 kHz	0-48	0-50		
Optocoupler Output Current	I_C	EA IN = V_S, Maximum Duty Cycle	400		600	µA
Dynamic Control Current	i_C	0 to Maximum Duty Cycle	50	100	200	µA
CIRCUIT PROTECTION						
FAULT Offset Current				100		µA
FAULT OV Threshold	V_{OV}			4		V
FAULT Current Limit Threshold	V_{ILIMIT}			0		V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
CIRCUIT PROTECTION (cont.)						
Current Limit Delay Time	$t_{d(off)}$	See Figure 6	75	150	250	ns
Thermal Shutdown Temperature			125	140		°C
Thermal Shutdown Hysteresis				15		°C
SHUTDOWN/AUTO-RESTART						
ON Time	t_{ON}	See Figure 7		38		ms
OFF Time	t_{OFF}	See Figure 7		150		ms
Reset Time	t_{RESET}	See Figure 7		12.5		ms
Charge/Discharge Ratio				4:1		
Upper Threshold Voltage	V_{THU}			4.0		V
Lower Threshold Voltage	V_{THL}			1.0		V
ERROR AMPLIFIER						
Reference Voltage	V_{REF}		1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}			50		ppm/°C
Gain-Bandwidth Product				500		kHz
DC Gain	A_{VOL}		60	80		dB
Output Impedance	Z_{OUT}			1.5		kΩ

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Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_S = 560 nF, T_A = -40 to 85°C (See Note 1)		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT (cont.)							
ON-State Resistance	$R_{DS(ON)}$	I_D = 200 mA	T_J = 25°C			7.2	Ω
			T_J = 115°C			13	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_J = 25°C	0.7	1.0		A
			T_J = 115°C	0.5	0.7		
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			150		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V			2000		nJ
Rise Time	t_r	See Figure 6			70	150	ns
Fall Time	t_f	See Figure 6			70	150	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open			3	4.5	mA
		V_{BIAS} > 8.25 V				0.1	
		Thermal Shutdown ON				2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied		8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied			3	4.5	mA
V_S Source Voltage	V_S			5.1		6.0	V
V_S Source Current	I_S					400	µA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP220 is connected to a high voltage power source when the test circuit is activated.

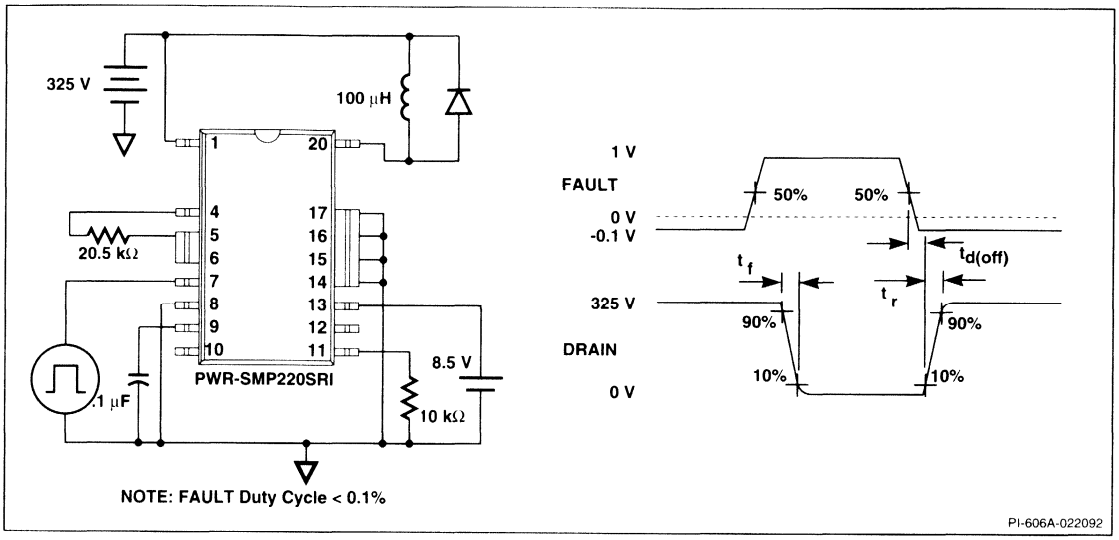


Figure 6. Current Limit Delay/Switching Time Test Circuit.

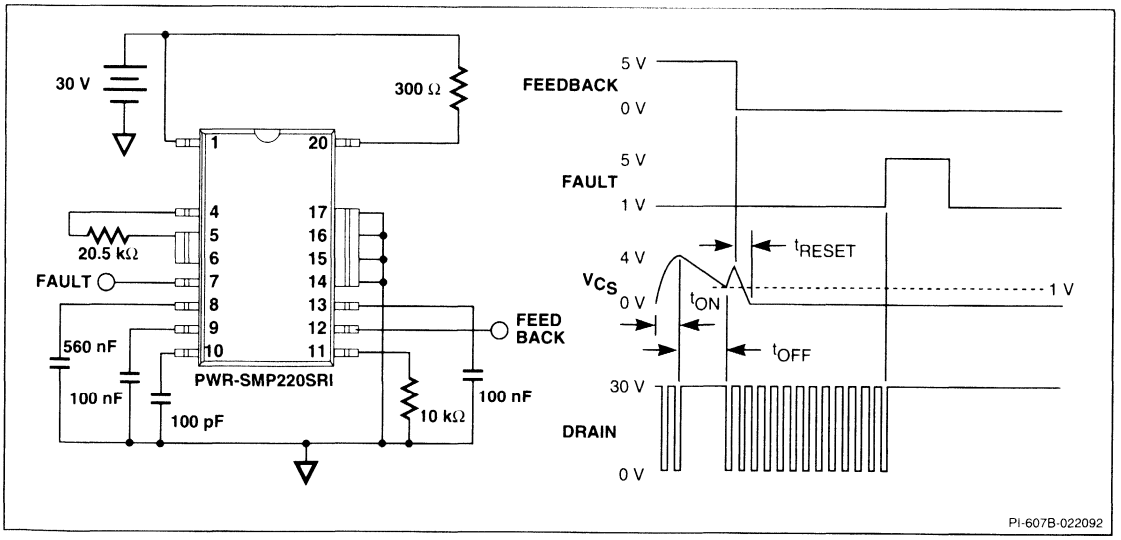
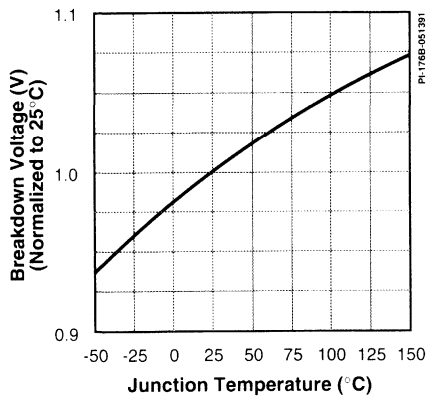
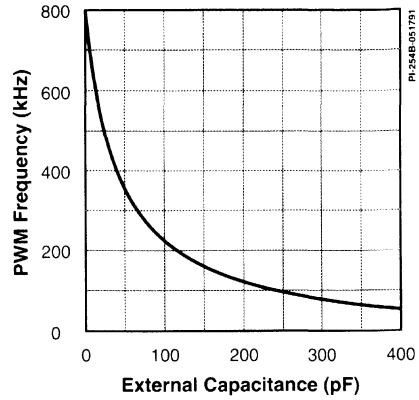


Figure 7. Auto-restart Test Circuit.

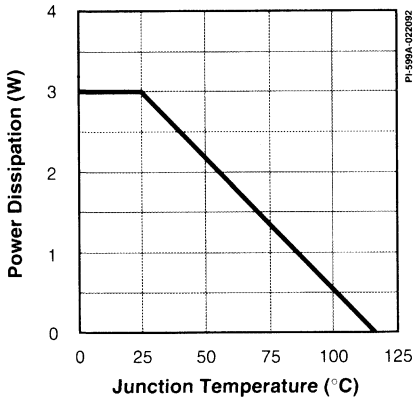
BREAKDOWN vs. TEMPERATURE



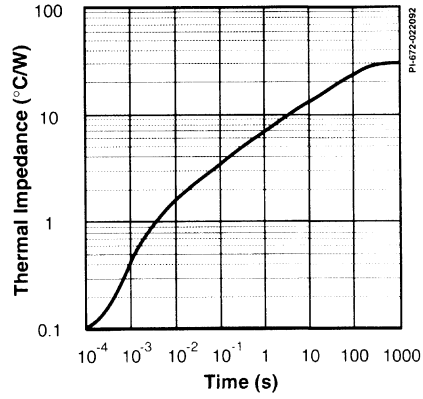
f_{PWM} vs. EXTERNAL CAPACITANCE



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP240

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller

- Output power up to 40 W from rectified 220/240 VAC input, 20 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller

- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-In Self-protection Circuits

- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

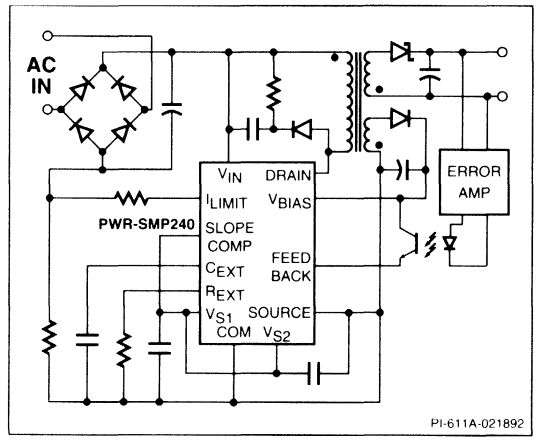


Figure 1. Typical Application

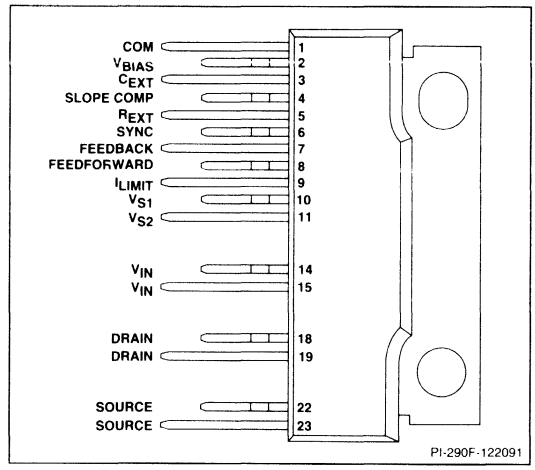


Figure 2. Pin Configuration

Description

The PWR-SMP240, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP240 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP240 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP240WTC	23-pin PWR SIP	0 to 70°C

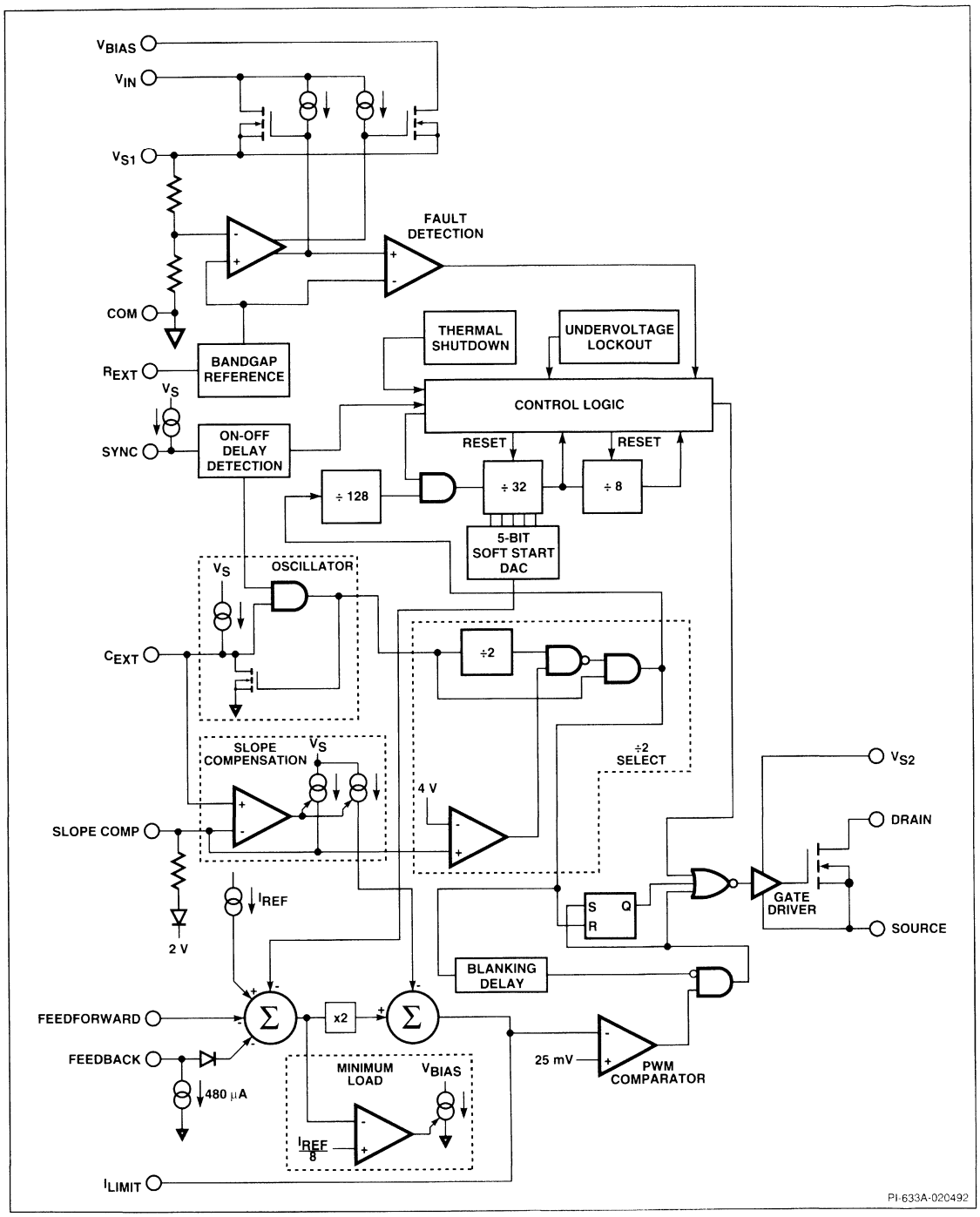


Figure 3. Functional Block Diagram of the PWR-SMP240.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
$\mathbf{V_{BIAS}}$ is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
$\mathbf{C_{EXT}}$ is used to set the oscillator frequency. Adding external capacitance between $\mathbf{C_{EXT}}$ and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connction through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between $\mathbf{R_{EXT}}$ and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
$\mathbf{I_{LIMIT}}$ is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
$\mathbf{V_{S1}}$ is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via $\mathbf{V_{S2}}$. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
$\mathbf{V_{IN}}$ for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

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PWR-SMP240 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP240 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the Ilimit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{SI} is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

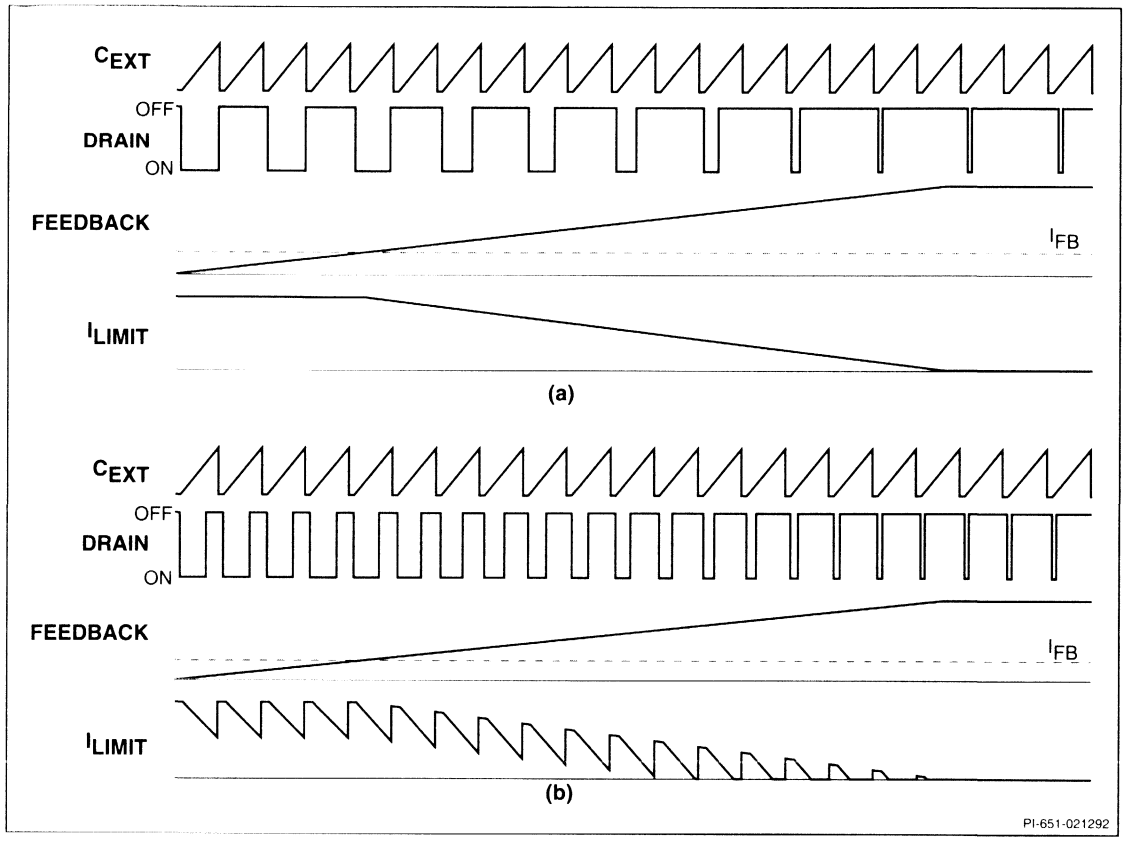


Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

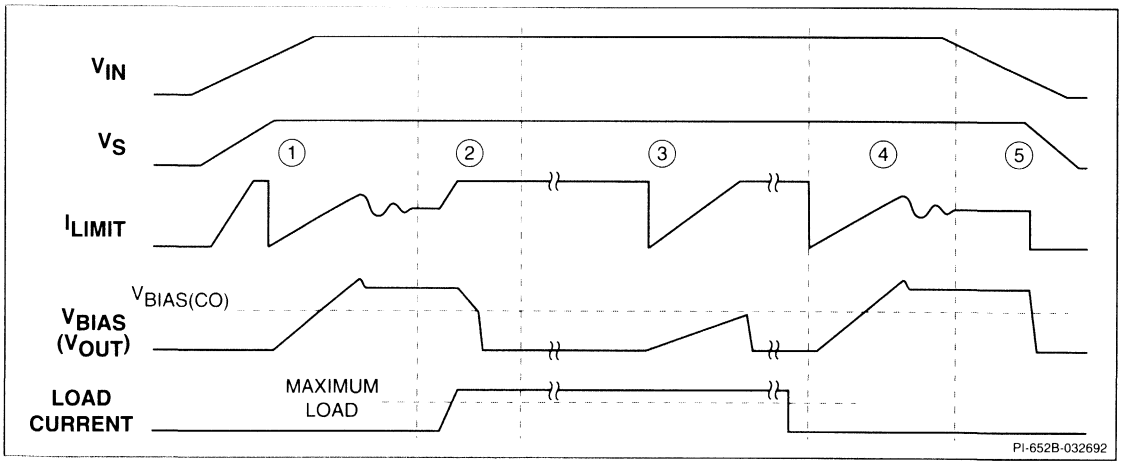


Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

20 W, Universal Off-line Power Supply

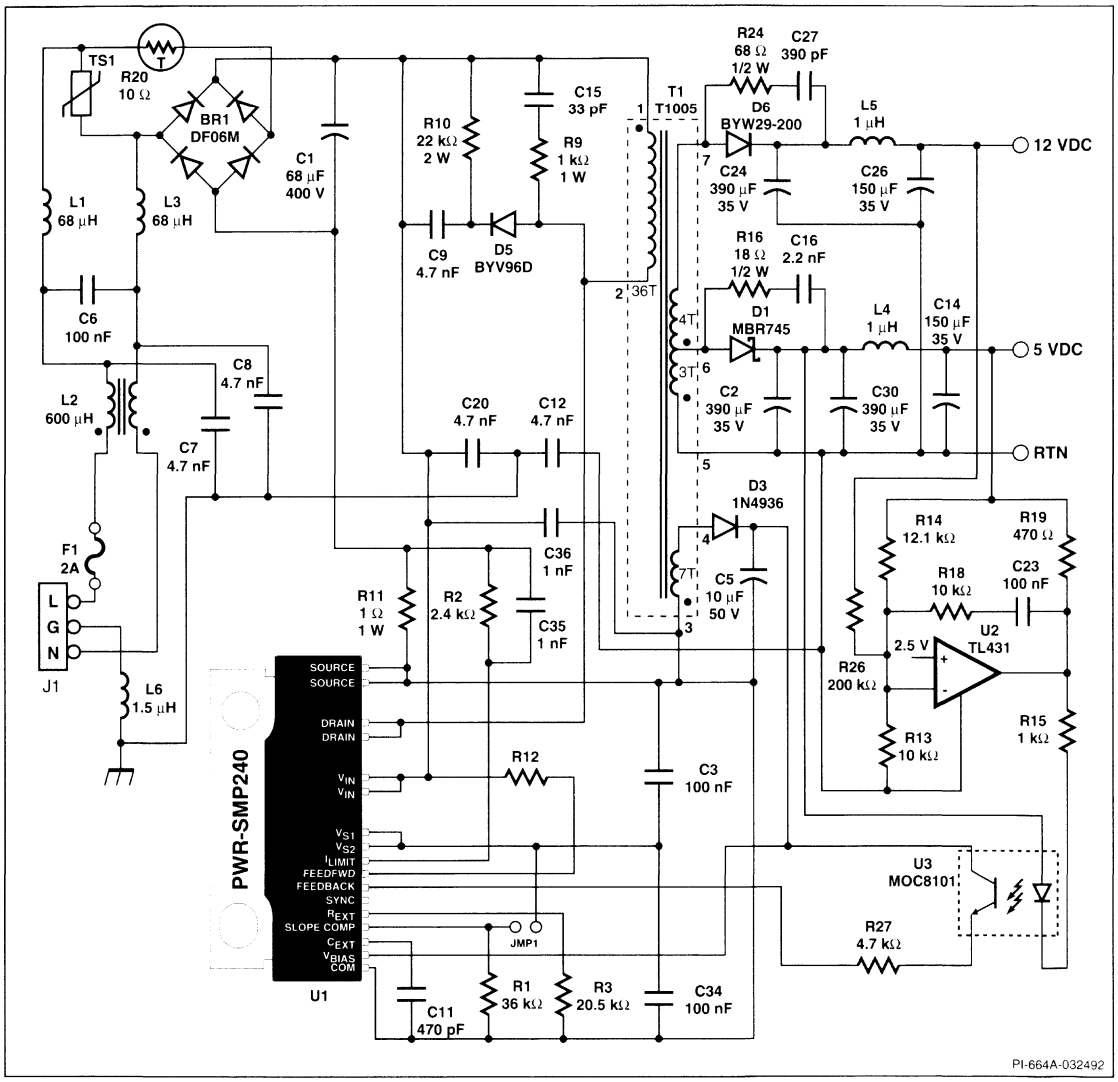


Figure 6. Schematic Diagram of a Single Output 20 W Supply Utilizing the PWR-SMP240.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 20 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current-mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

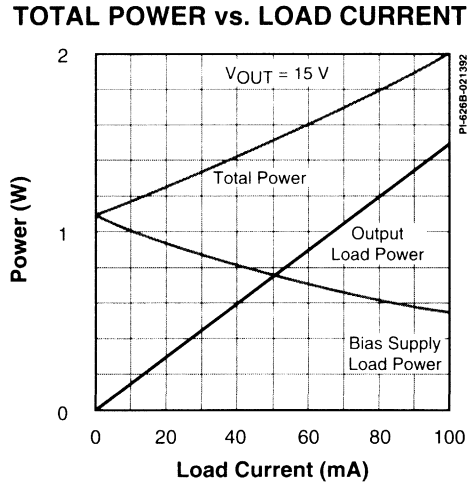


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP240 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{IN} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SI} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

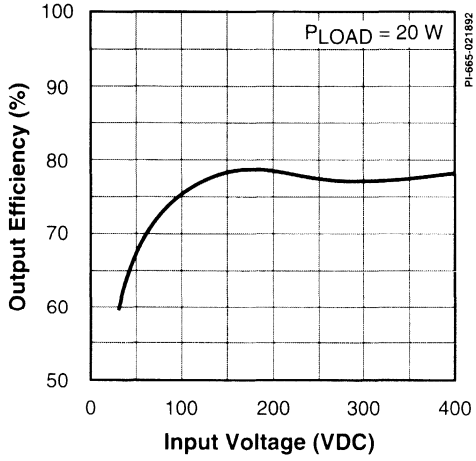
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

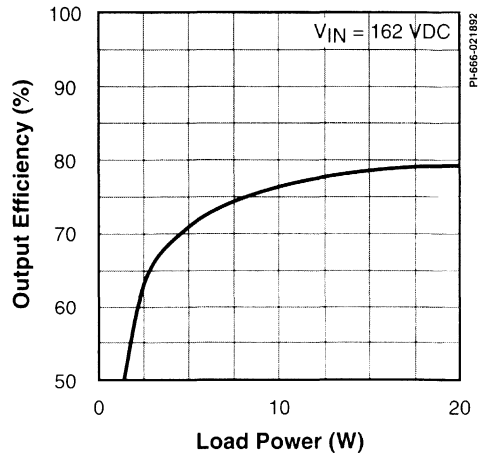
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL8 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP240. Complete supply specifications are included, as will as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 2 A
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} =325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S, FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
PULSE WIDTH MODULATOR (cont.)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity				±0.5		lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C			5	Ω
			T_J = 115°C			8.5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		1.2	1.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			200		pF
Output Stored Energy	E_{OSS}				1500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP240 is connected to a high-voltage power source when the test circuit is activated.

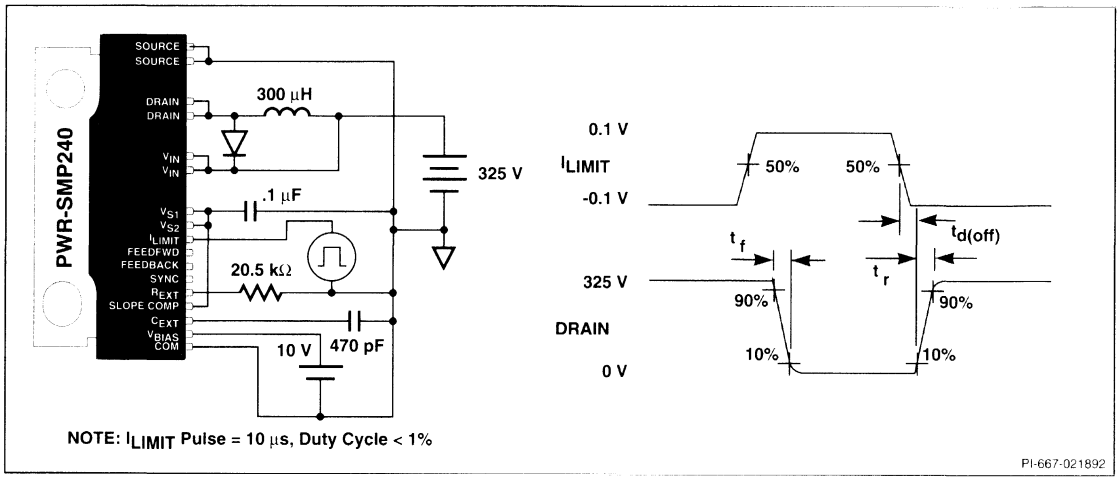
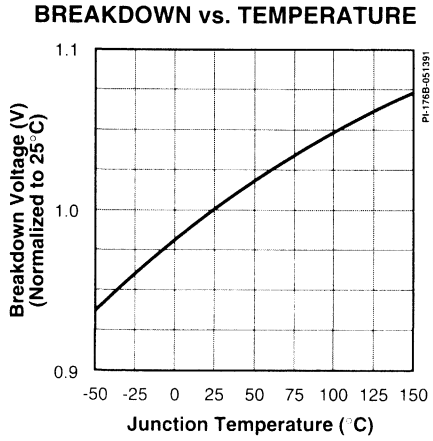
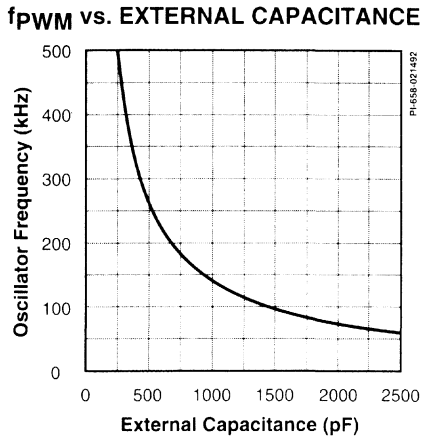
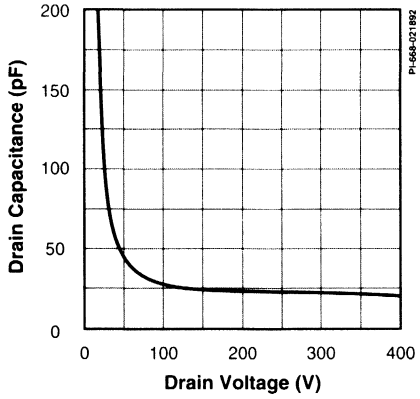


Figure 8. Switching Time Test Circuit.

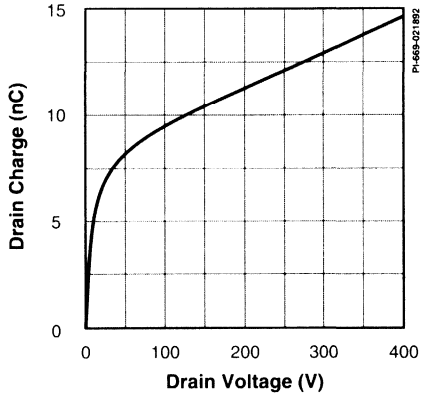




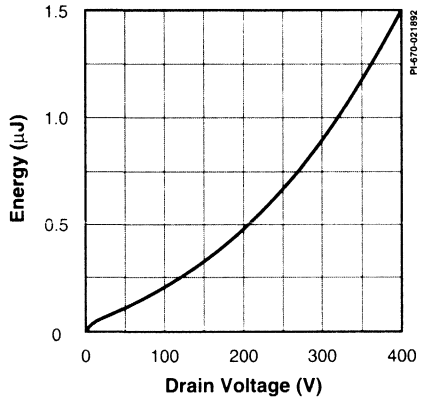
C_{OSS} vs. DRAIN VOLTAGE



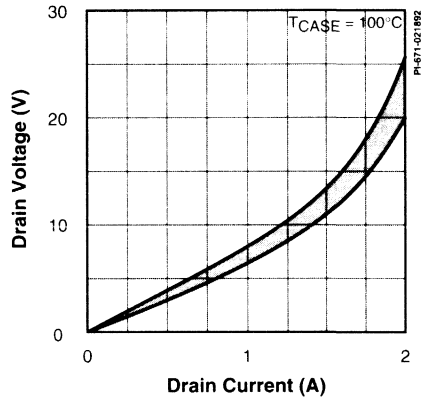
DRAIN CHARGE vs. DRAIN VOLTAGE



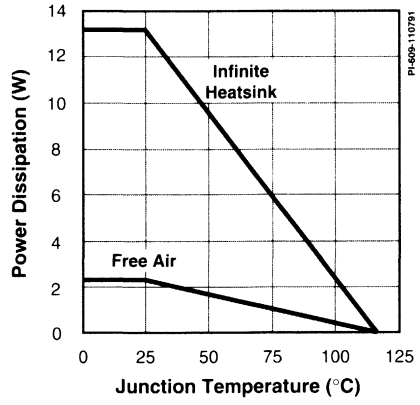
DRAIN CAPACITANCE ENERGY



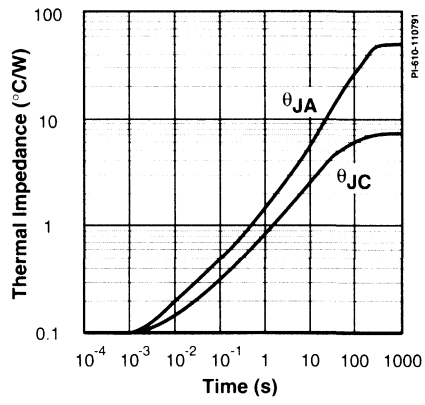
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



1

PWR-SMP260

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 60 W from rectified 220/240 VAC input, 30 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-In Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

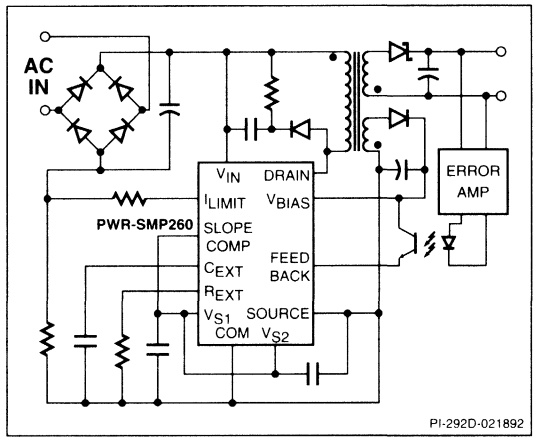


Figure 1. Typical Application

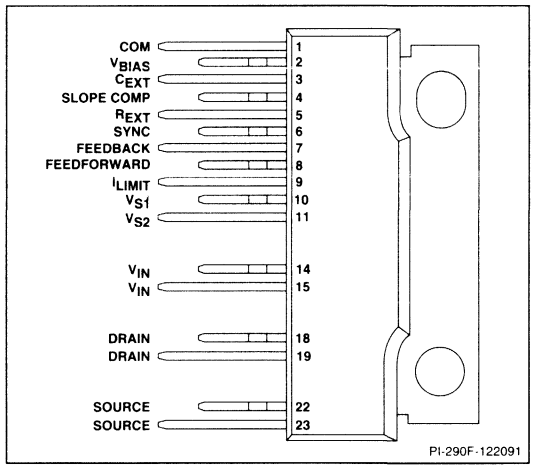


Figure 2. Pin Configuration

Description

The PWR-SMP260, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP260 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP260 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP260WTC	23-pin PWR SIP	0 to 70°C

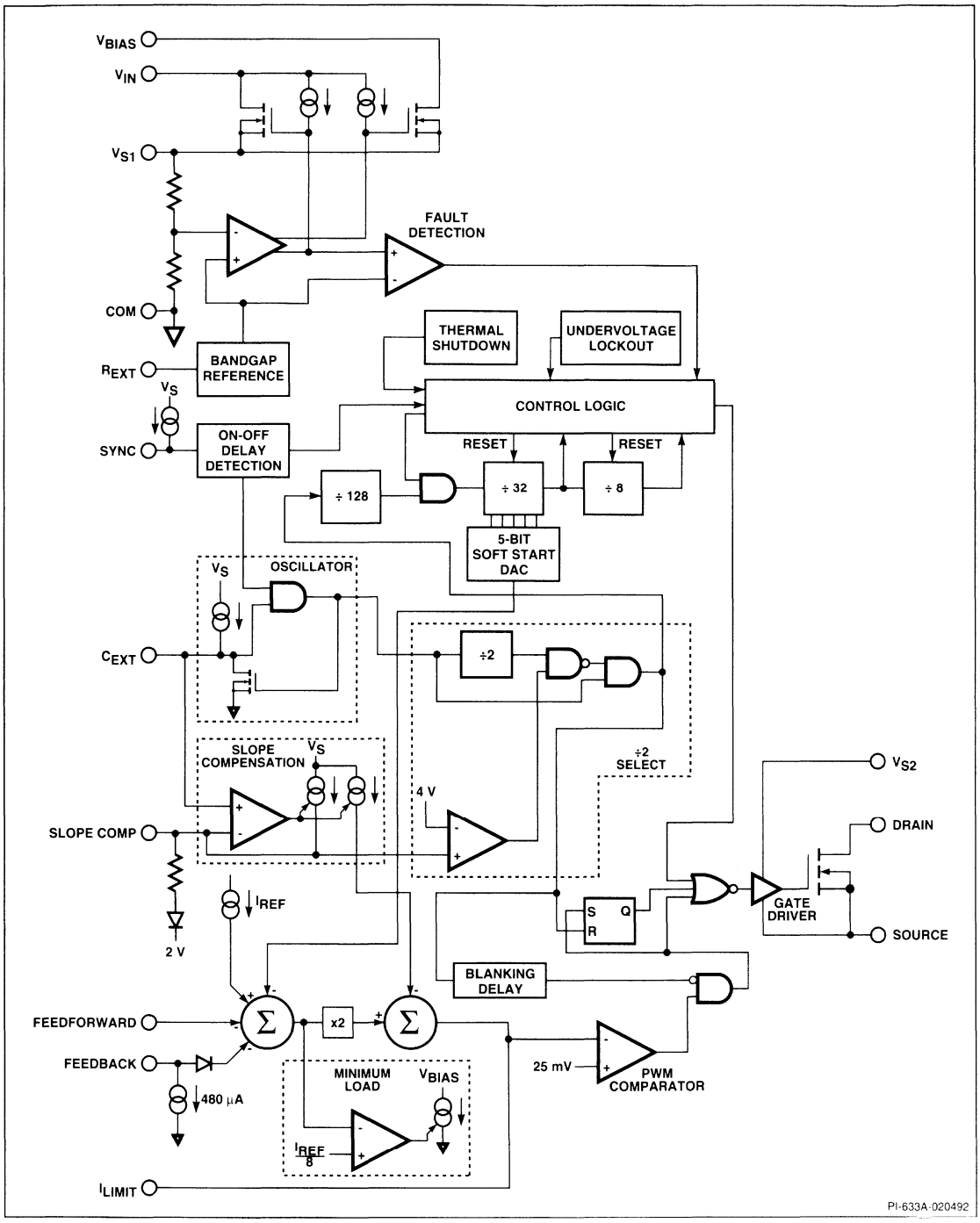


Figure 3. Functional Block Diagram of the PWR-SMP260.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connection through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

1

PWR-SMP260 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP260 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care chould be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the Ilimit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{S1} voltage is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

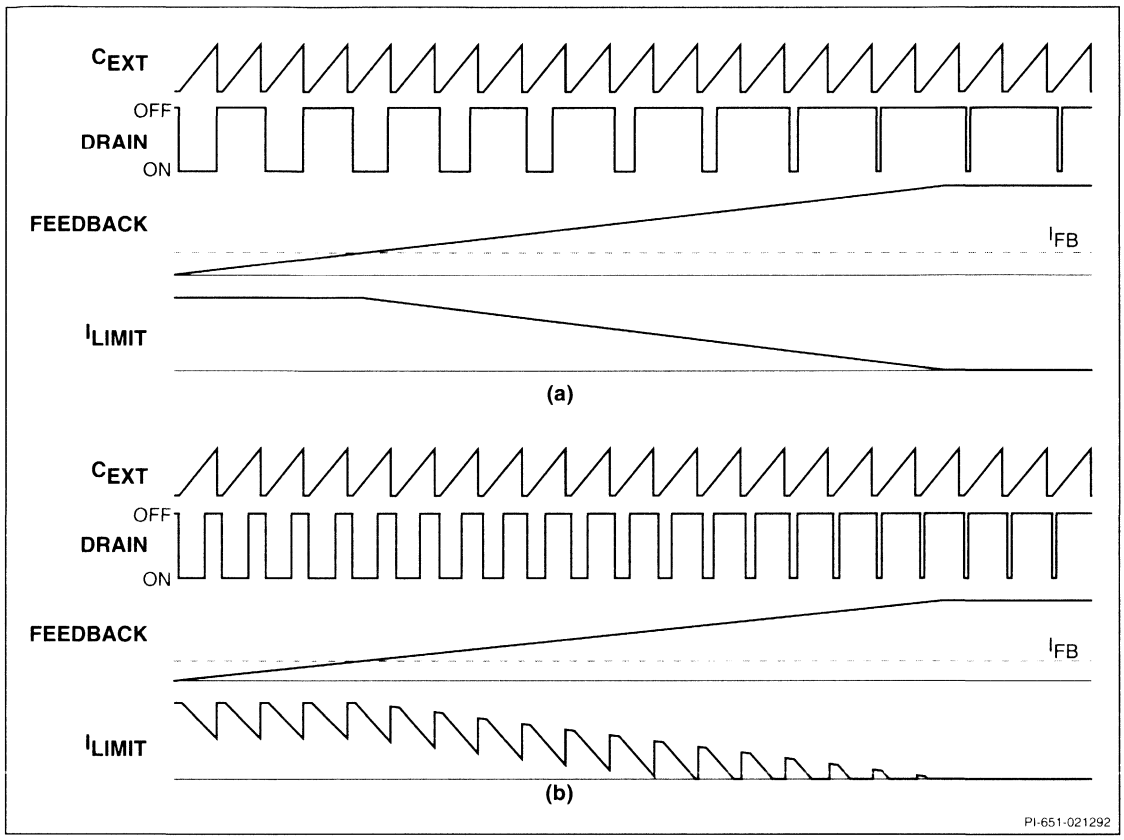


Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

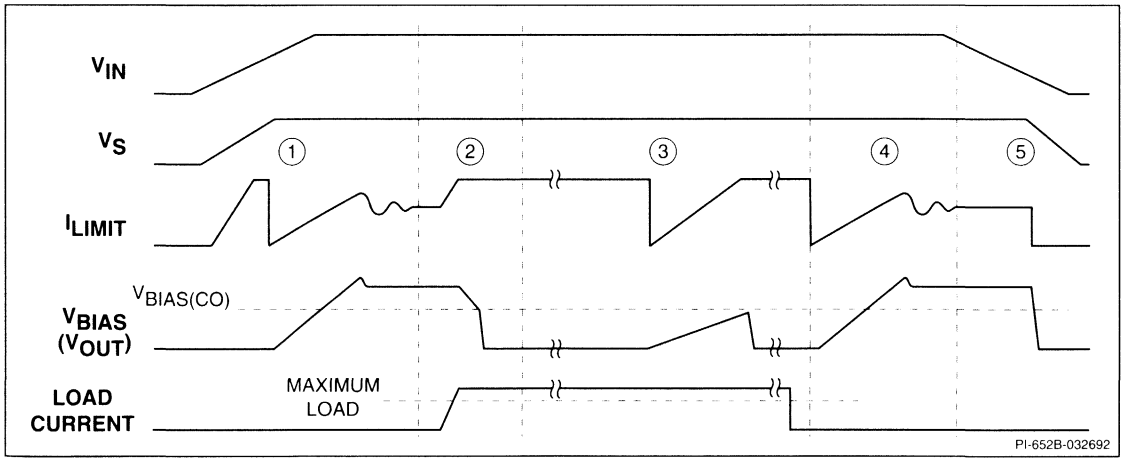


Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

30 W, Universal Off-line Power Supply

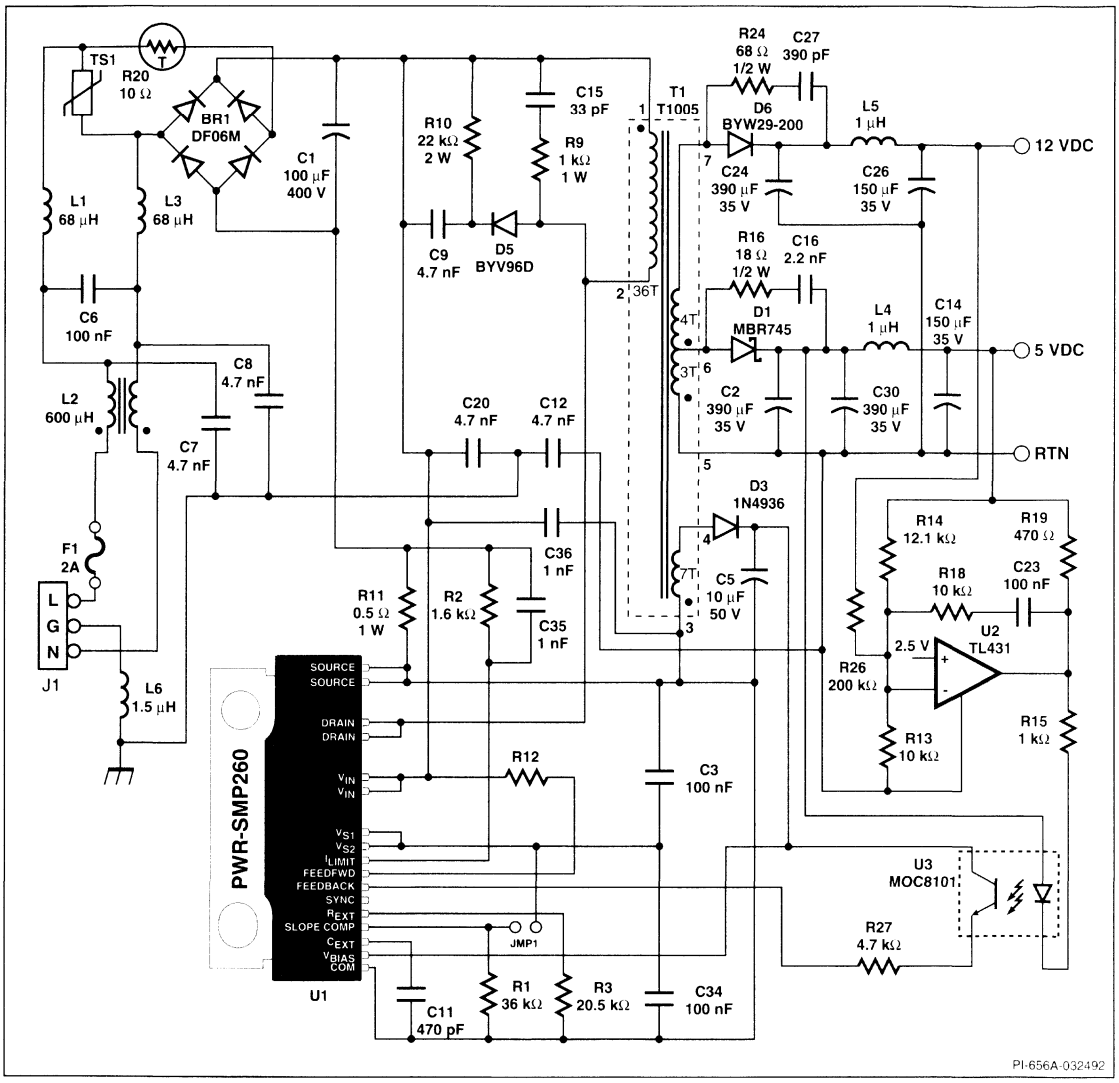


Figure 6. Schematic Diagram of a Single Output 30 W Supply Utilizing the PWR-SMP260.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 30 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SU}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SU}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

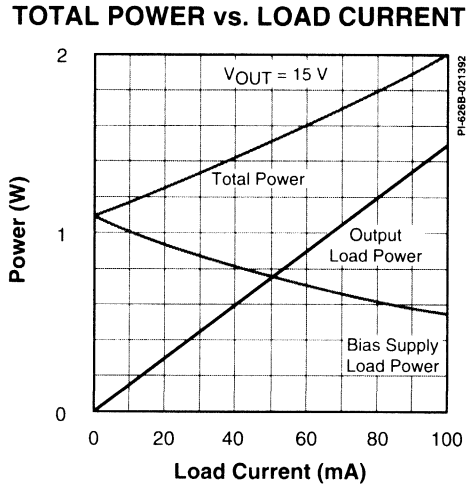


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{IN} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SI} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

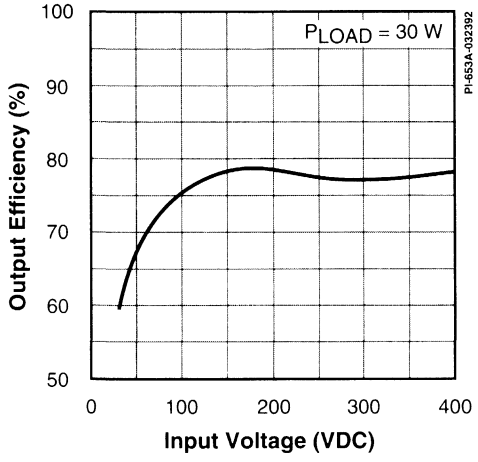
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

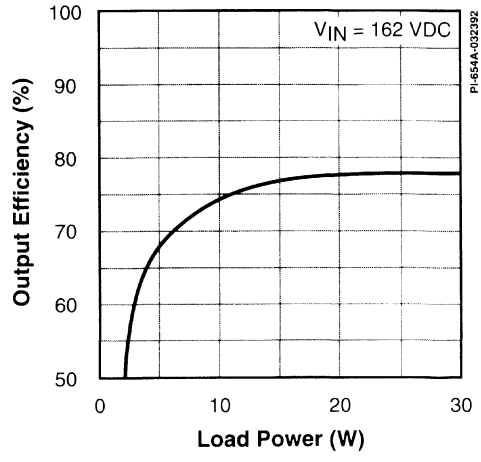
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL7 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP260. Complete supply specifications are included, as will as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 3 A
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} =325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S, FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
PULSE WIDTH MODULATOR (cont.)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity				±0.5		lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	TYP	MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C			3	Ω
			T_J = 115°C			5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		2	2.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			280		pF
Output Stored Energy	E_{OSS}				2500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP260 is connected to a high-voltage power source when the test circuit is activated.

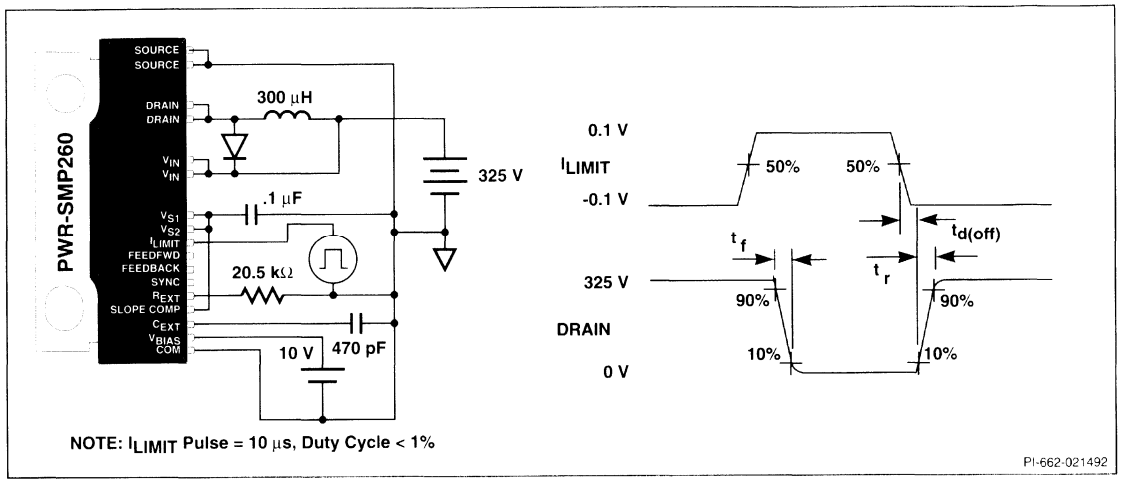
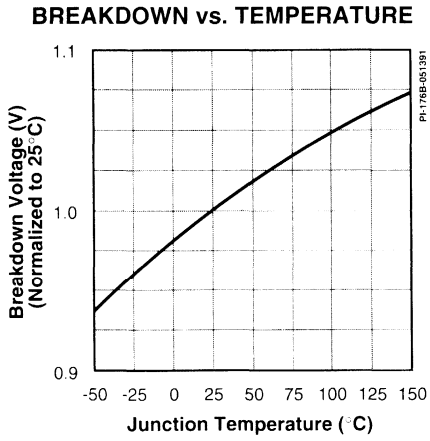
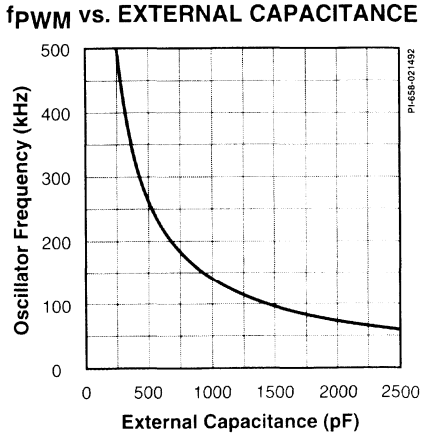
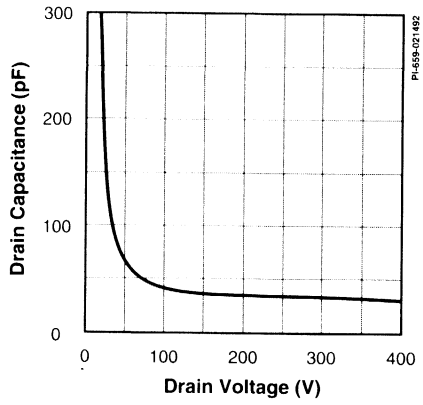


Figure 8. Switching Time Test Circuit.

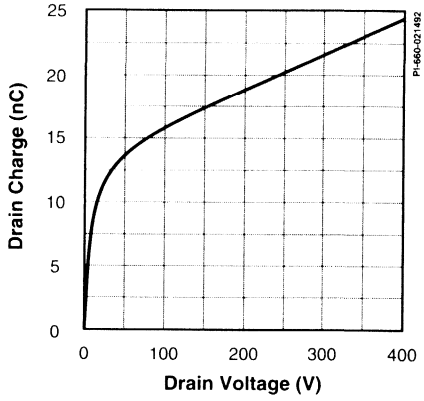




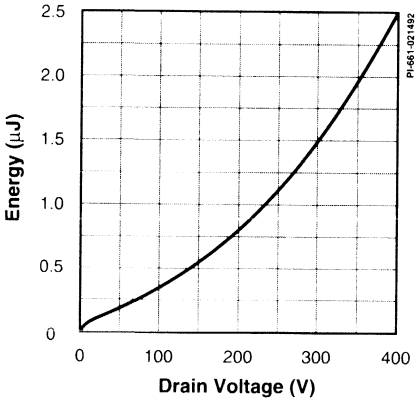
C_{OSS} vs. DRAIN VOLTAGE



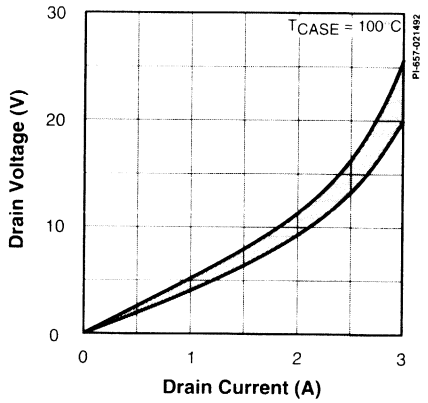
DRAIN CHARGE vs. DRAIN VOLTAGE



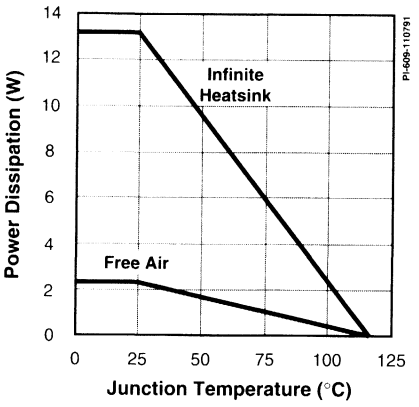
DRAIN CAPACITANCE ENERGY



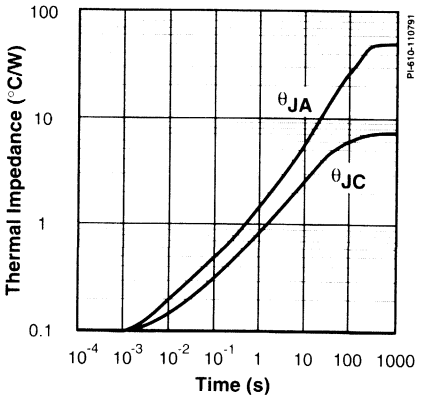
TRANSFER CHARCTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



1

PWR-SMP400

PWM Power Supply IC

20-100 VDC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power > 5 W from 48 VDC input
- Integrated solution minimizes overall size
- External transformer provides isolation and selectable output voltages

High-voltage, Low-capacitance MOSFET Output
- Designed for telecommunications and distributed power applications
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Inherent current limiting protects from short circuits
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

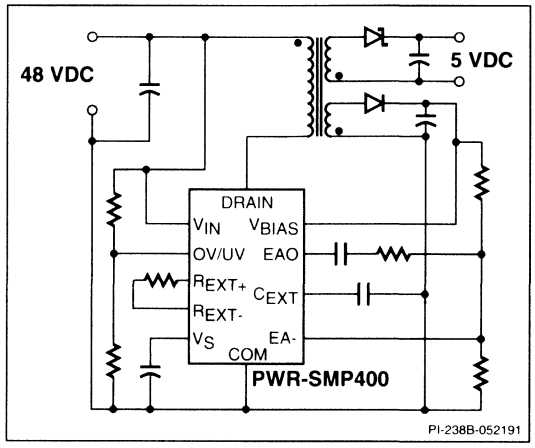


Figure 1. Typical Application

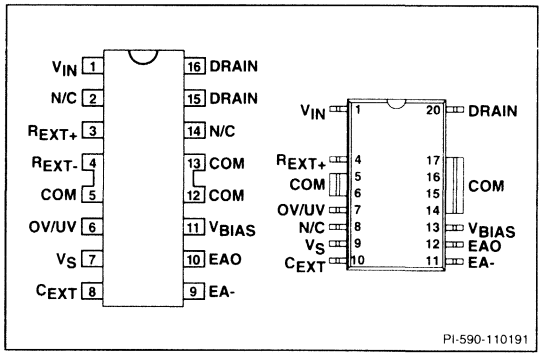


Figure 2. Pin Configurations.

Description

The PWR-SMP400, intended for telecommunications and distributed power applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated converter. High frequency operation reduces total power supply size.

The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. The combination of lower capacitance and lower gate threshold voltage results in a tenfold reduction in gate drive power. Lower capacitances also facilitate higher frequency operation.

The controller section of the PWR-SMP400 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference, error amplifier, gate driver, undervoltage lockout, and over-temperature protection, and current limiting. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies.

The PWR-SMP400 is available in a 16-pin plastic batwing DIP or 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP400BNC	16-pin PWR PDIP	0 to 70°C
PWR-SMP400BNI	16-pin PWR PDIP	-40 to 85°C
PWR-SMP400SRI	20-pin PWR SOIC	-40 to 85°C

Pin Functional Description

(Pin Number in Parenthesis is for SOIC Version)

Pin 1(1):
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3(4):
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4(5, 6):
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13(14, 15, 16, 17):
COM connections. Ground or reference point for the circuit.

Pin 6(7):
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7(9):
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8(10):
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9(11):
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10(12):
EAO is the error amplifier output for connection to the external compensation network.

Pin 11(13):
V_{BIAS} is the feedback voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15, 16(20):
Open **DRAIN** of the output MOSFET. Both pins must be externally connected.

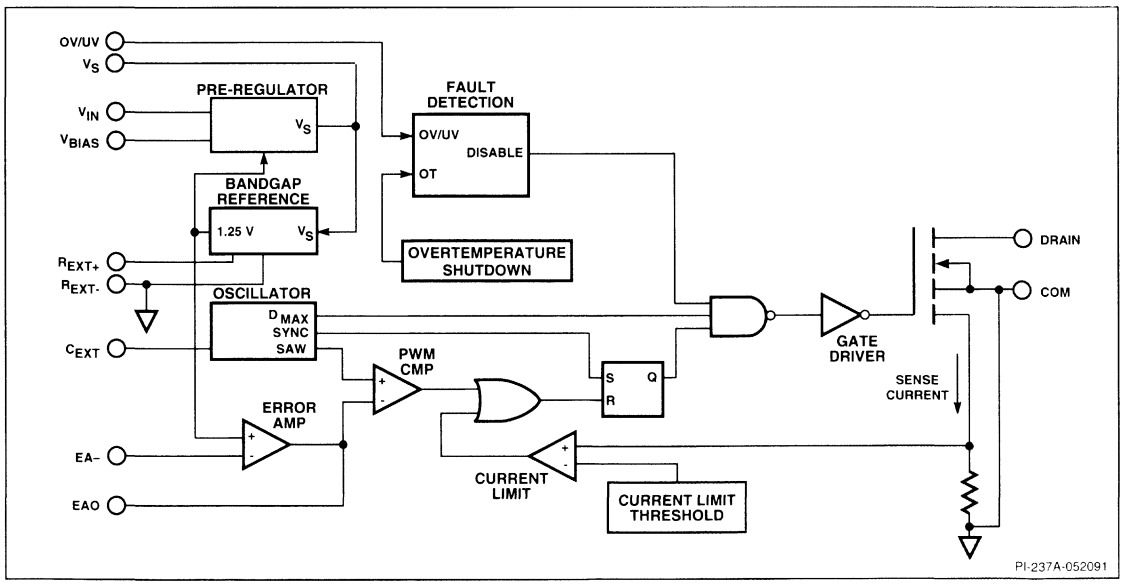


Figure 3. Functional Block Diagram of the PWR-SMP400.

PWR-SMP400 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET.

The pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. The oscillator frequency can be lowered by adding additional capacitance at the C_{EXT} pin.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

The error amplifier output pin EAO is buffered so that external loads will not affect its output. The buffer has an offset voltage of around 2 V, and an output impedance of about 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle. The transfer function is linear from zero to maximum duty cycle, providing a very wide dynamic range.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Current Limit Protection
The current limit sense consists of a current mirror on the power device and a sense resistor. The current mirror produces a current proportional to the drain current of the power switch. A sense voltage is generated by passing the mirror current through a sense resistor. This voltage is then compared to a reference voltage using an internal comparator.

5 W, 48 V DC-DC Converter with Feedback Winding Regulation

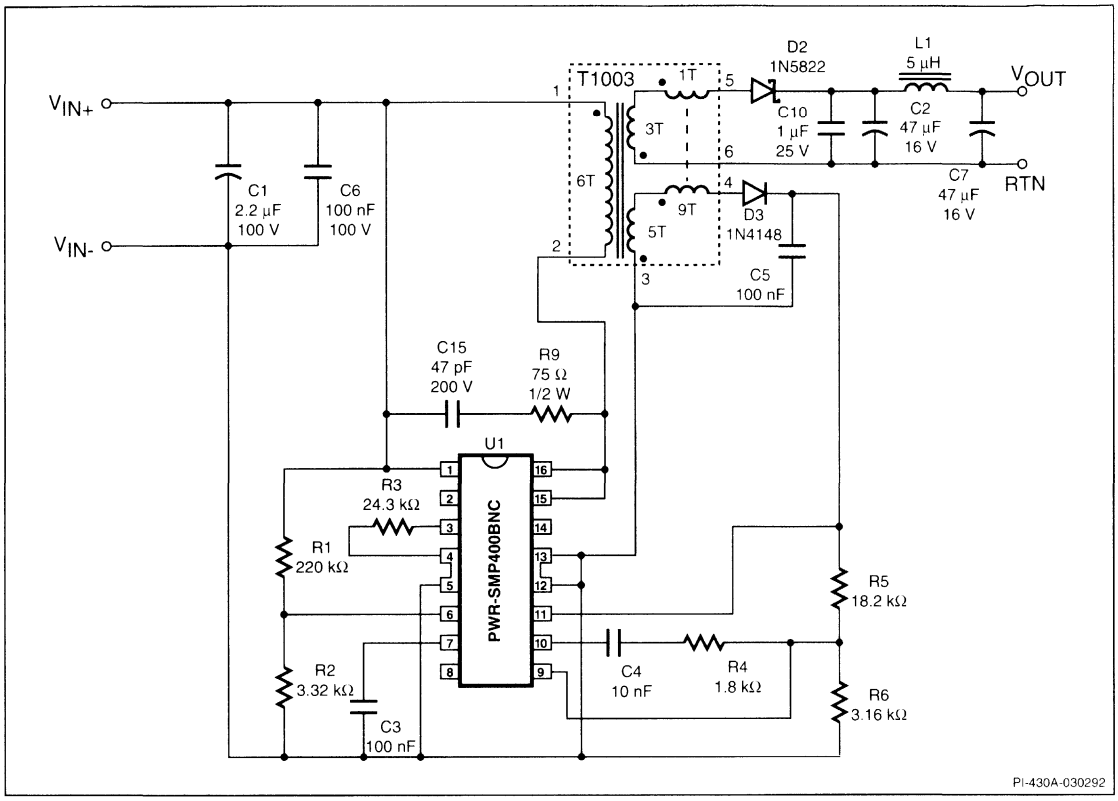


Figure 4. Schematic Diagram of a 5 W DC-DC Converter Utilizing the PWR-SMP400. For Improved Regulation, use the Optical Feedback Circuit Shown in AN-8.

General Circuit Operation

The flyback power supply circuit shown in Figure 4, when operated with the T1003 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 30 to 80 VDC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding. The PWR-SMP400 has been designed for a feedback voltage (pin 11) of 8.5 volts. The effective transformer volts per turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. Three elements affect the regulation of the output voltage: maintaining a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

C1 and C6 form the EMI filter. The voltage divider formed by R1 and R2 set the input voltage that activates the input undervoltage and overvoltage shutdown function. C15 and R9 damp the leakage inductance ringing voltage. C2, C7, C10 and L1 form the output filter. This damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage (VBIAS) to 8.5 volts. R4, R5, C2, C4, C7, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP400. C3 and C5 are bypass capacitors.

General Circuit Operation (cont.)

To achieve full output power and reliable operation of the PWR-SMP400, both DRAIN connections on the batwing DIP package (pin 15 and 16) must be connected together at the printed circuit board. Pin 15 and 16 are not connected within the package.

This circuit uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and stability of ±5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on optical feedback.

The circuit shown in Figure 4 is the schematic diagram of the PWR-EVAL4 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP400. Complete supply specifications are included, as well as instructions on how to modify the board for other output voltages and oscillator frequencies.

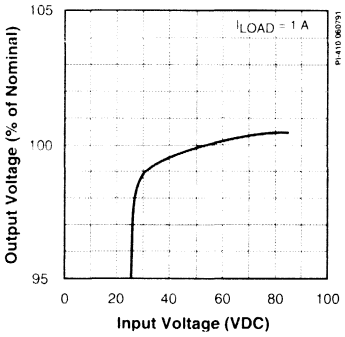
The line and load regulation graphs shown below were measured on a PWR-EVAL4 board operated from a DC source. The switching frequency of the power supply was measured at 750 kHz.

The maximum output power curve shows the power output capability for the standard transformer T1003. See DA-3 for further information on ordering transformers for use with the PWR-SMP400.

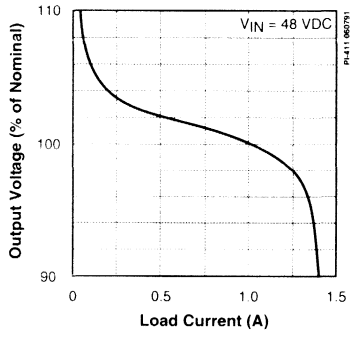
The output power versus frequency curve was generated by characterization of the PWR-SMP400 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-offs between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

Typical Performance Characteristics (Figure 4 Power Supply)

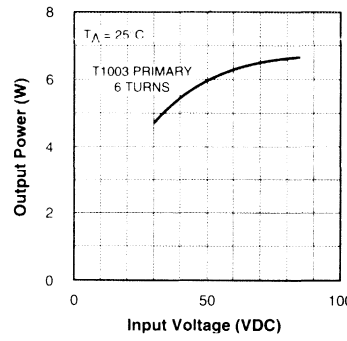
LINE REGULATION



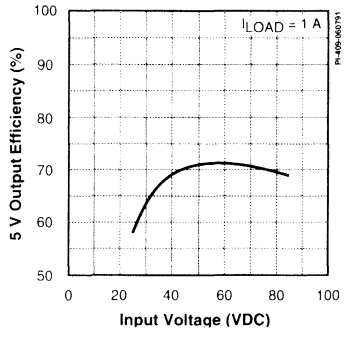
LOAD REGULATION



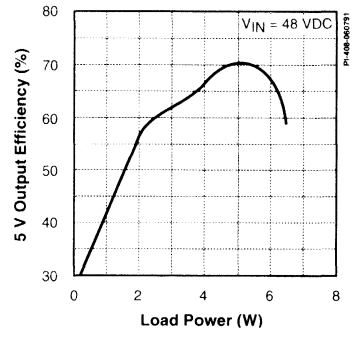
MAXIMUM OUTPUT POWER



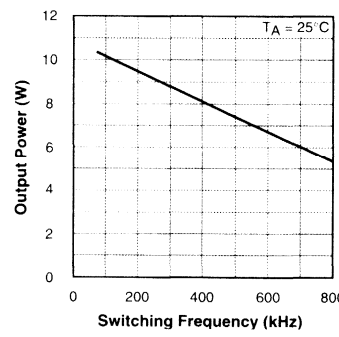
EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



OUTPUT POWER vs. FREQUENCY



ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage ..... 200 V
V_{IN} Voltage ..... 200 V
V_{BIAS} Voltage ..... 11 V
Drain Current[2] ..... 2.5 A
Input Voltage[3] ..... - 0.3 V to V_S + 0.3 V
Storage Temperature ..... -65 to 125°C
Ambient Temperature (C Suffix) ..... 0 to 70°C
(I Suffix) ..... -40 to 85°C
Junction Temperature ..... 150°C
Lead Temperature[4] ..... 260°C
Power Dissipation
BN Suffix (T_A = 25°C) ..... 2.1 W
(T_A = 70°C) ..... 1.05 W
Power Dissipation
SR Suffix (T_A = 25°C) ..... 3.0 W
(T_A = 70°C) ..... 1.5 W
Thermal Impedance (θ_{JA}) (BN Suffix) ..... 43°C/W
(SR Suffix) ..... 30°C/W
Thermal Impedance (θ_{JC})[5] (BN Suffix) ..... 6°C/W
(SR Suffix) ..... 6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = Full Operating Range (see Note 1)		Test Limits MIN	TYP	MAX	Units
OSCILLATOR							
Output Frequency	f_{OSC}	C_{EXT} = Open	C Suffix	650	750	825	kHz
			I Suffix	650	750	850	
PULSE WIDTH MODULATOR							
Duty Cycle	DC	C_{EXT} = Open		0-35	0-40		%
		f_{OSC} = 200 kHz		0-45	0-50		
CIRCUIT PROTECTION							
Current Limit Threshold				0.9	1.1	1.25	A
Input UV Trip-off				0.29	0.34	0.39	V
Input UV Hysteresis				35	50	70	mV
Input OV Trip-off		See Note 2		1.17	1.25	1.33	V
Input OV Hysteresis				40	60	80	mV
OV/UV Turn-off Delay Time		See Figure 5			250	500	ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BB} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = Full Operating Range (see Note 1)		Test Limits MIN	TYP	MAX	Units
CIRCUIT PROTECTION (cont.)							
Thermal Shutdown Temperature				115	135		°C
Thermal Shutdown Hysteresis					45		°C
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 500 mA	T_J = 25°C		3	4.1	Ω
			T_J = 115°C		5.3	6.4	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		0.9	1.1		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 160 V, T_A = 115°C			10	25	µA
Breakdown Voltage	BV_{DSS}	I_D = 100 µA, T_A = 25°C		200			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			75		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 48 V			85		nJ
Rise Time	t_R	See Figure 5			10	20	ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 24.3 kΩ, T_A = Full Operating Range (see Note 1)		Test Limits MIN	TYP	MAX	Units
OUTPUT (cont.)							
Fall Time	t_F	See Figure 5			20	50	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		200	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			6.5		8.25	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open	C Suffix		4	5.0	mA
			I Suffix		4	5.6	
		V_{BIAS} > 8.25 V				0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback	C Suffix		4	5.0	mA
			I Suffix		4	5.6	
V_S Source Voltage	V_S			5.1		6.0	V
V_S Source Current	I_S					400	µA

NOTES:

1. Those specifications having only one limit number apply over the entire temperature range for both C Suffix (0 to 70°C), and I Suffix (-40 to 85°C) versions. Those specifications with a split limit showing each temperature range separately are as marked.

2. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP400 is connected to a high voltage power source when the test circuit is activated.

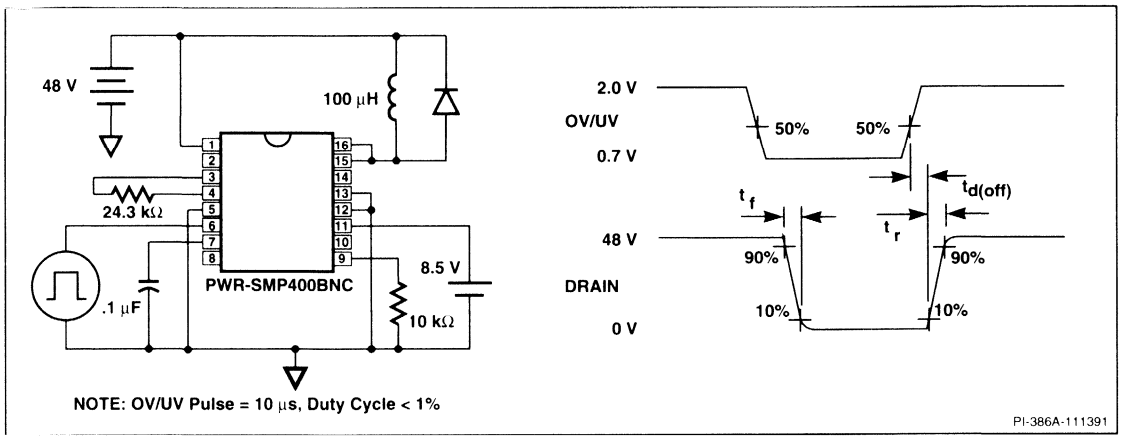
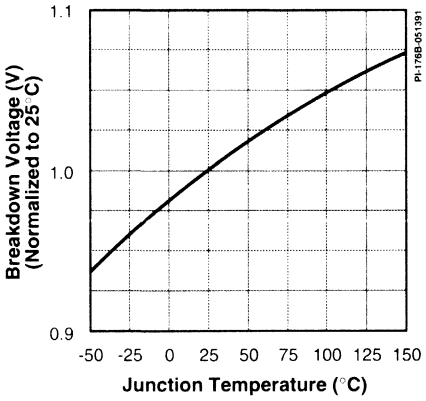
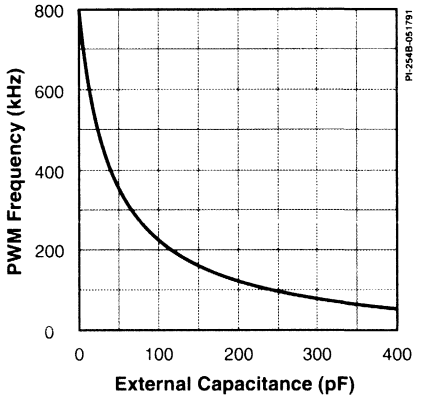


Figure 5. Switching Time Test Circuit.

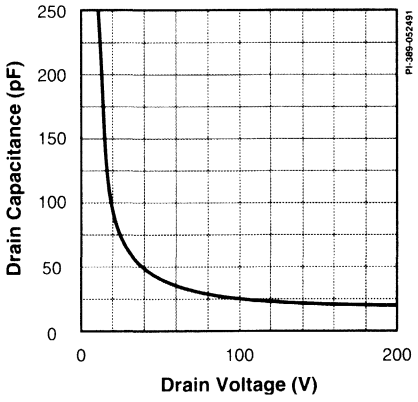
BREAKDOWN vs. TEMPERATURE



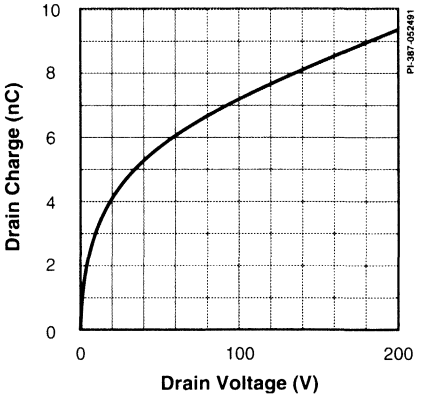
f_{PWM} vs. EXTERNAL CAPACITANCE



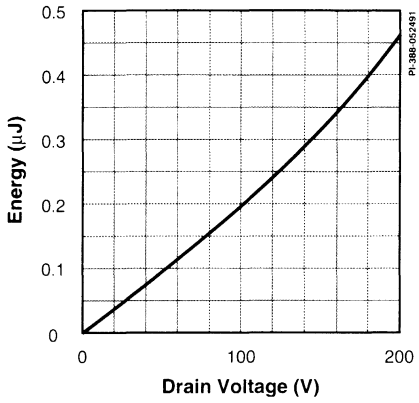
C_{OSS} vs. DRAIN VOLTAGE



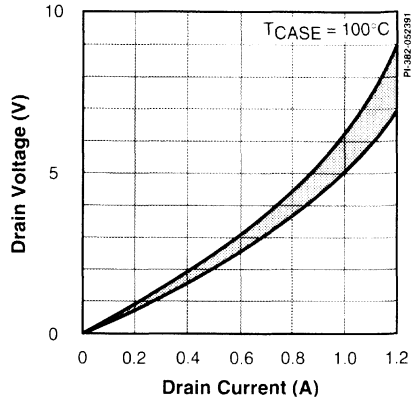
DRAIN CHARGE vs. DRAIN VOLTAGE



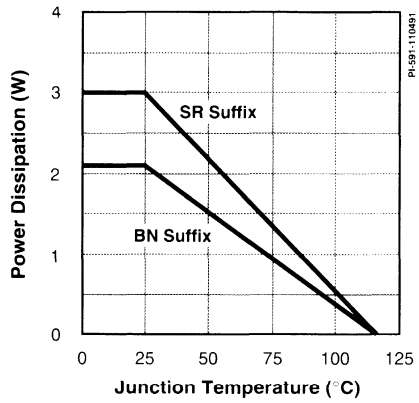
DRAIN CAPACITANCE ENERGY



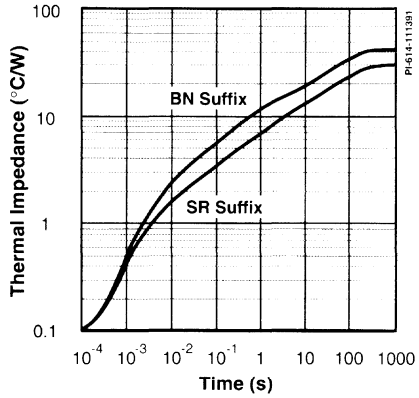
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-SMP402

1-Watt Buck Regulator IC

20-72 VDC Input
Non-isolated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power > 1 W from 48 VDC input
- Adjustable output voltage
- Integrated solution minimizes overall size

High-voltage, Low-capacitance MOSFET Output
- Designed for ISDN T1 telecommunications applications
- Low capacitance allows for high frequency operation

High-voltage Buck Regulator
- Internal pre-regulator self-powers the IC on start-up
- Designed for low power consumption
- Minimum external parts required

Built-In Self-protection Circuits
- Undervoltage lockout
- Thermal shutdown
- Input polarity/level sense

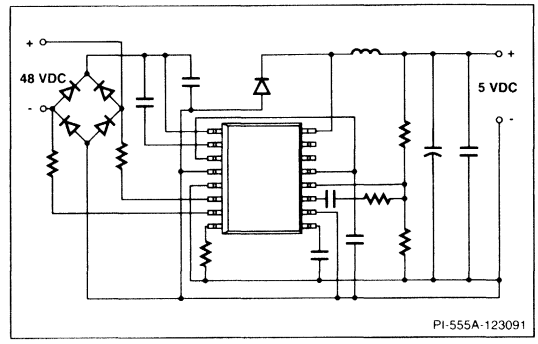


Figure 1. Typical Application.

Description

The PWR-SMP402, intended for non-isolated ISDN telecommunications power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost power supply which meets stringent ISDN specifications. High frequency operation reduces total power supply size.

The P-channel power MOSFET switch features include high voltage, low $R_{DS(ON)}$, and low capacitance. Lower capacitance results in a reduction in gate drive power, and also facilitates higher frequency operation.

The controller section of the PWR-SMP402 contains all the blocks required to drive and control the power stage: start-up pre-regulator circuit, oscillator, bandgap reference, error amplifier, gate driver and level shift. Protection features include undervoltage lockout, thermal shutdown, and input polarity and level sensing.

The PWR-SMP402 is available in a 16-pin plastic SOIC package.

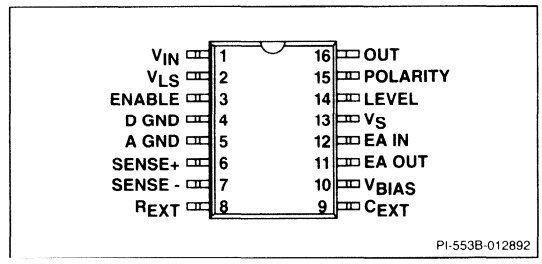


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP402TNC	16-pin SOIC	0 to 70°C

Pin Functional Description

Pin 1:
V_{IN} is the high-voltage input to the switching regulator. This is the Source connection of the P-Channel power MOSFET pass transistor.

Pin 2:
V_{LS} is an internal supply for the level shift circuit that drives the P-Channel MOSFET. A capacitor should be placed between V_{LS} and V_{IN} for bypassing. V_{LS} is normally 10 V below V_{IN}.

Pin 3:
The power supply can be shut down by pulling **ENABLE** low.

Pin 4:
D GND is the common return point for the logic portions of the circuit.

Pin 5:
A GND is the common return point. R_{EXT} and C_{EXT} are directly connected to this point.

Pin 6:
The **SENSE+** input monitors the polarity and level of the input voltage for ISDN emergency standby sensing.

Pin 7:
The **SENSE-** input monitors the polarity and level of the input voltage for ISDN emergency standby sensing.

Pin 8:
A 20.5 kΩ resistor connected between R_{EXT} and A GND sets the internal bias currents including oscillator charge and discharge currents.

Pin 9:
The oscillator frequency can be programmed by selecting the value of the capacitor connected between C_{EXT} and A GND.

Pin 10:
V_{BIAS} can be connected to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off when the output is in regulation.

Pin 11:
EA OUT is the error amplifier output pin for connection to the external compensation network.

Pin 12:
EA IN is the error amplifier negative input for connection to the feedback and compensation networks.

Pin 13:
V_S is the internal supply voltage. This pin is brought out for external bypassing.

Pin 14:
The **LEVEL** output indicates when the input voltage is in its normal operating range.

Pin 15:
The **POLARITY** output is used to notify a microprocessor of an emergency standby condition for ISDN applications.

Pin 16:
OUT is the Drain connection of the P-Channel pass transistor.

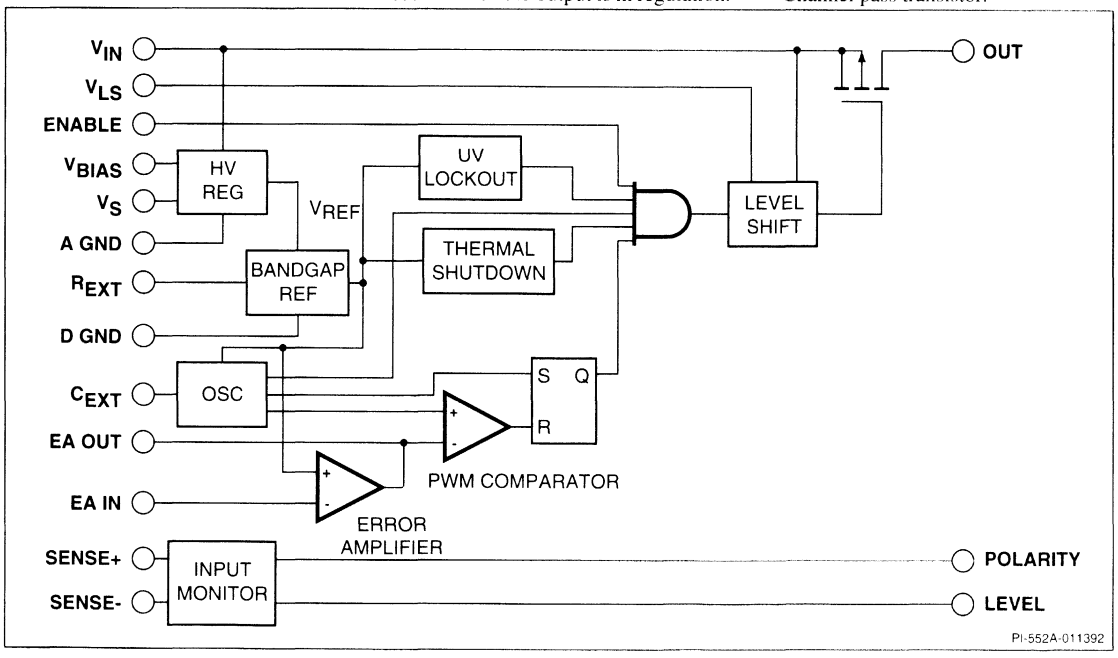


Figure 3. Functional Block Diagram.

Functional Description

High Voltage Regulator
The high-voltage regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5 volts by controlling the gate of the MOSFET.

In 5 V output applications, the control circuitry may also be operated by connecting the V_{BIAS} pin to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off automatically when the converter output is in regulation. Only the supply current for the level shift stage (≈50 µA) and the AC switching currents for the P-Channel output device are drawn from the V_{IN} supply under this condition. If unused, V_{BIAS} must be hardwired to A GND to disable the automatic switchover during powerup.

V_{LS} is the level-shift supply for driving the gate of the internal P-channel MOSFET. The voltage at V_{LS} is approximately 10 V below V_{IN}. V_S is the supply voltage for the controller and driver circuitry. External bypass capacitors connected to V_{LS} and V_S are required for filtering and reducing noise.

UV Lockout
During powerup, the Undervoltage Lockout circuit keeps the P-channel output transistor in the off state until the internal V_S supply is in regulation and the voltage sensed by the input monitor circuit is within the normal operation range (>20 V).

Band Gap Reference
V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier and over temperature circuit.

Oscillator
The oscillator frequency can be adjusted by changing the external C_{EXT} capacitor. This capacitor is charged and discharged by switched constant current sources.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

Thermal Shutdown
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Input Polarity and Level Sense
The input monitor circuitry checks the input voltage polarity. The inputs to the circuit are SENSE+ and SENSE-, low impedance input nodes biased at approximately 1.5 V and externally connected by dropping resistors to the high-voltage input.

POLARITY is a logic-level output that indicates the input voltage polarity. When the input voltage is normal, POLARITY is high, and when the input voltage is reversed, POLARITY is low. This output is only valid after the output voltage is in regulation.

The LEVEL output indicates the input voltage level as defined by the two sensing resistors R_{S+} and R_S. It is valid only after the output voltage is in regulation. Since the internal undervoltage lockout is set at 20 V, it is recommended that the LEVEL input be set at no less than 24 V for proper operation.

Enable
The power supply can be shut down by pulling the ENABLE pin low. It is internally pulled up to V_S with a 100 µA (nominal) current source. However, it is recommended that this pin be tied to V_S if it is unused.

P-Channel Output Transistor
The output MOSFET is a 90 V pass transistor capable of supplying >200 mA. To minimize switching noise and EMI, it is important to keep the path from OUT through the output diode, the input storage capacitor, and into V_{IN} as short as possible.

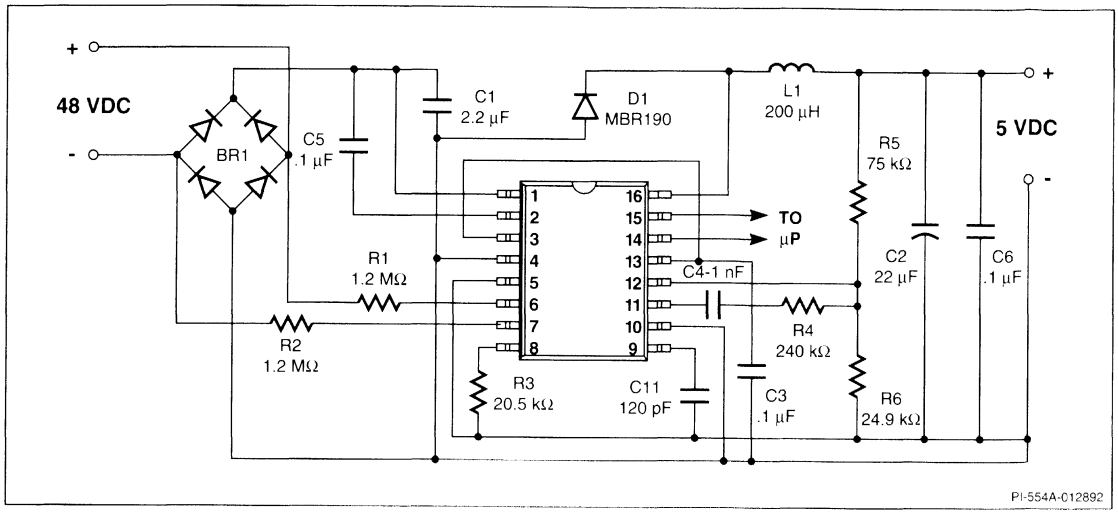


Figure 4. Non-isolated ISDN Regulator Circuit.

General Circuit Operation

The buck regulator power supply circuit shown in Figure 4 will produce a 5 volt, 1 watt power supply that will operate over a 20 to 72 VDC input voltage range. The output voltage is selected by the resistor divider ratio formed by R5 and R6. The maximum output voltage is limited to 50% of the minimum DC input voltage by the maximum duty cycle and the voltage drop across the switch when it is on.

$$V_O = 1.25 \times \frac{R_5 + R_6}{R_6}$$

The P-channel switch inside the integrated circuit, D1, L1, and C2 form the buck regulator power processing path. The P-channel switch and D1 chop the DC input voltage with a duty cycle that changes the average voltage to be equal to the output voltage and L1 and C2 form the low pass filter that extracts the average value and rejects the AC components of the switching waveform.

R4, R5, and C4 are the frequency compensation components for the output error amplifier and affect the stability of the control loop. The values of these components are related to the low pass filter elements L1 and C2.

C11 sets the oscillator frequency. The frequency is inversely proportional to the capacitance value and is nominally 200 kHz when using a 120 pF capacitor. R3 sets the internal current sources within the integrated circuit. The value of R3 is fixed.

C3 and C5 are bypass capacitors that supply transient currents within the integrated circuit. C5 bypasses the P-channel gate drive circuit . C1 is the input filter capacitor. C1 averages the pulsing current that flows through the P-channel switch to reduce the EMI feedback to the DC voltage source. C1 also stores energy to sustain the output voltage for short interruptions in the DC input voltage.

R1 and R2 are used to sense the polarity of the input voltage for ISDN applications. A reversed battery voltage indicates emergency standby battery operation. The POLARITY signal allows the control logic in the integrated circuit to notify the load when this occurs. The input voltage at which LEVEL notifies the load that an undervoltage condition occurs can be selected by the values of R1 and R2.

The circuit also has an enable input that allows the output voltage to be turned off with a logic signal. This signal is normally generated by the logic circuitry in the load circuit, and turns off non-essential loads and/or functions when an emergency battery condition exists.

ABSOLUTE MAXIMUM RATINGS[1]

V_{IN} Voltage	90 V
Drain-Source Voltage (V_{IN} to OUT)	90 V
V_{BIAS} Voltage	5.5 V
SENSE Current	±200 µA
OUT Current	250 mA
Logic Input Voltage	-0.3 V to V_S + 0.3 V
Storage Temperature	-65 to 165°C
Ambient Temperature	0 to 70°C
Junction Temperature	150°C
Lead Temperature[2]	260°C
Power Dissipation	1.0 W
Thermal Impedance (θ_{JA})	100°C/W

1. Unless noted, all voltages referenced to A GND, T_A=25°C
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = 30 to 300 pF	50		500	kHz
Initial Accuracy	Δf_{OSC}		170	200	230	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC		0-50	0-60		%
ERROR AMPLIFIER						
Threshold Voltage	V_{REF}		1.25		1.35	V
Gain-Bandwidth Product				0.5		MHz
DC Gain	A_{VOL}		60	80		dB
Output Impedance	Z_{OUT}			1		kΩ
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				15		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V, R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF, R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
LOGIC							
Input Current High	I_{IH}				10	50	µA
Input Current Low	I_{IL}				100	500	µA
Input Voltage High	V_{IH}					3.0	V
Input Voltage Low	V_{IL}			1.0			V
Output Voltage High	V_{OH}	I_{OH} = -0.5 mA		3.5			V
Output Voltage Low	V_{OL}	I_{OL} = 0.5 mA				0.4	V
SENSE INPUTS							
POLARITY Threshold Voltage		See Figure 5			0		V
LEVEL Threshold Current		See Figure 5			23		µA
LEVEL Current Hysteresis		See Figure 5			3		µA
LEVEL Bias Voltage		See Figure 5			1.7		V
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_{OUT} = -100 mA	T_J = 25°C			12	Ω
			T_J = 115°C			20	
ON-State Current	$I_{D(ON)}$	See Note 1		200			mA
OFF-State Current	I_{DSS}	OUT = 72 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{OUT} = -100 µA, T_A = 25°C		90			V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
SUPPLY						
HV Regulator Voltage	V_{IN}		20		72	V
Off-line Supply Current	I_{IN}	V_{BIAS} = A GND			2.5	mA
		V_{BIAS} = 5 V			1.5	
V_{BIAS} Supply Voltage	V_{BIAS}		4.75		5.25	V
V_{BIAS} Supply Current	I_{BIAS}			1		mA

NOTES:

1. At low output currents (< 20 mA), the part may operate in blocking oscillation mode, resulting in large output ripple.

INPUT VOLTAGE CONDITION	POLARITY	LEVEL
Negative voltage, level too low	0	0
Negative voltage, correct level	0	1
Positive voltage, level too low	1	0
Positive voltage, correct level	1	1

Figure 5. LEVEL/POLARITY Input-Output Truth Table.

PWR-SMP520

PWM Controller IC

110/220 VAC Input
MOSFET Cascode Drive Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Pre-regulator and CMOS Controller
- Implements isolated power supply
- Supplies up to 10 W from rectified 110 VAC and 20 W from rectified 220 VAC using an external MOSFET
- Pre-regulator derives power from the line during start-up
- External transformer provides isolation and selectable output voltages

Low-capacitance MOSFET Driver
- Drives external MOSFET in cascode configuration
- Expanded drive capability available

High-speed Voltage-mode PWM Controller
- High PWM frequency reduces component size
- Minimum external parts required

Built-In Self-protection Circuits
- Fast integrated current limit protects external MOSFET
- Input overvoltage shutdown/undervoltage lockout
- Thermal shutdown

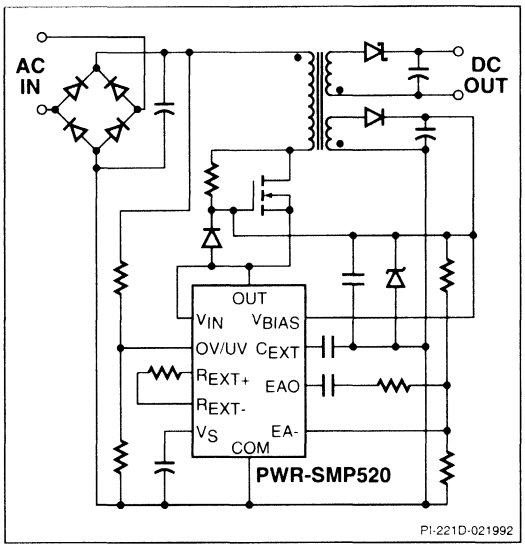


Figure 1. Typical Application

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Description

The PWR-SMP520 is a PWM controller which combines a high-voltage pre-regulator, a switchmode controller, and a MOSFET driver in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

MOSFET driver features include low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage. Lower capacitances facilitate higher frequency operation when driving an external MOSFET in a cascode configuration.

The controller section of the PWR-SMP520 contains all the blocks required to drive and control the power stage: start-up pre-regulator circuit, oscillator, bandgap reference, error amplifier, gate driver, undervoltage lockout, thermal shutdown, and current limiting. C_{EXT} allows selection of PWM frequency.

The PWR-SMP520 is available in a 16-pin plastic DIP package.

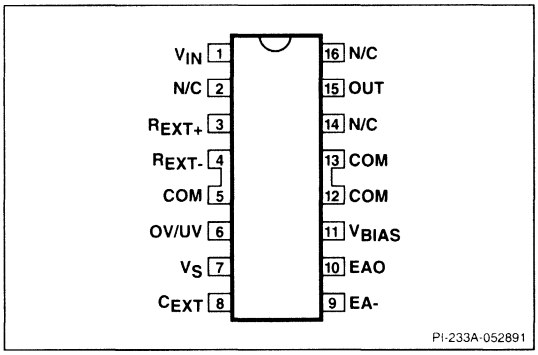


Figure 2. Pin Configuration

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP520BNC	16-pin PWR PDIP	0 to 70°C

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the controller during start-up.

Pin 2:
N/C for creepage distance.

Pin 3:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4:
R_{EXT-} is the return for the reference current. Do not connect to ground plane.

Pin 5, 12, 13:
COM connections. Ground or reference point for the circuit.

Pin 6:
OV/UV is used with an external resistor divider to shut down the power supply when the input voltage is not within the desired range.

Pin 7:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9:
EA– is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10:
EAO is the error amplifier output for connection to the external compensation network.

Pin 11:
V_{BIAS} is the feedback voltage used to self power the controller once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15:
OUT connects the controller to an external MOSFET.

Pin 16:
N/C for creepage distance.

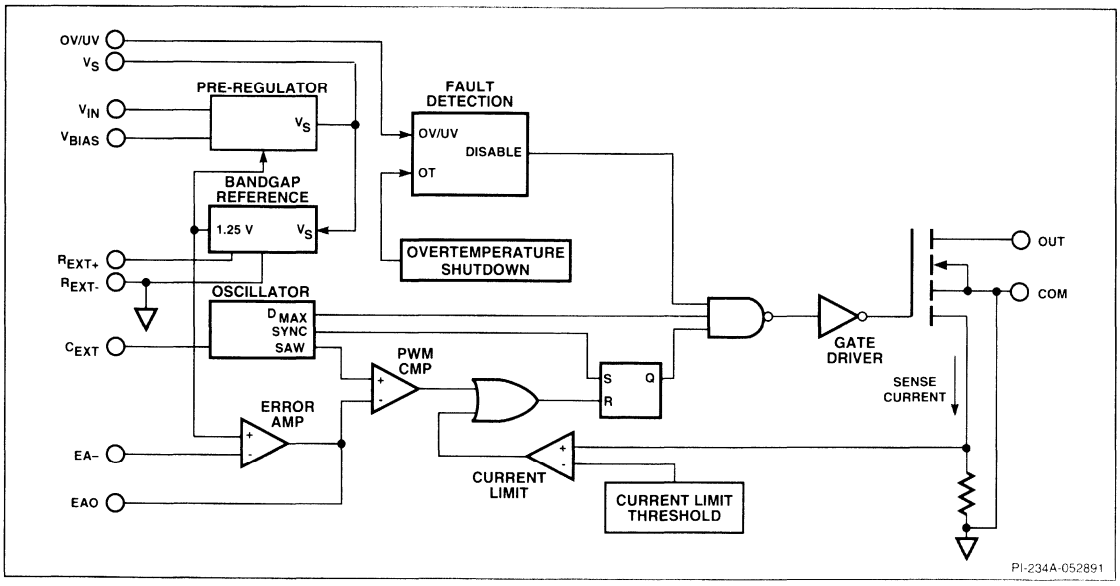


Figure 3. Functional Block Diagram of the PWR-SMP520.

PWR-SMP520 Functional Description

Pre-regulator and On-board Voltages
The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. During start-up, the pre-regulator regulates V_{BIAS} to approximately 7.5 volts. Once the output of the power supply is in regulation, the error amplifier regulates V_{BIAS} to approximately 8.5 volts by controlling the duty cycle applied to the source of the external MOSFET. The pre-regulator is turned off by forcing its output voltage from 7.5 volts to 8.5 volts. V_{BIAS} is used by another linear regulator to generate the onboard supply voltage V_S.

The pre-regulator is intended to be connected to the midpoint of the cascode drive circuit. The source of the high-voltage switching transistor and the pre-regulator input will be switching from ground to 25 volts at the power supply operating frequency. When the power supply output voltage V_{BIAS} is low, the bias current for the controller circuit flows through the pre-regulator and the high-voltage MOSFET. This can cause significant amounts of power to be dissipated in the MOSFET. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and internal bias current is supplied by the feedback circuit.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

Band Gap Reference
V_{REF} is the 1.25 volt reference voltage generated by the temperature compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, oscillator, over temperature circuit, and current limit circuit.

Oscillator
The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. An external capacitor can be added to lower the switching frequency.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the driver.

The error amplifier output pin is buffered from the actual amplifier output and has approximately a 2 volt offset and output impedance of 1.5 kΩ.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the cascode driver. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

The protection circuitry inhibits the driver signal when the input voltage is outside the limits of operation.

OV/UV Lockout Protection
Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 135°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Current Limit Protection
The current limit circuit consists of a current mirror on the output driver and a current sense resistor. The current mirror produces a current proportional to the drain current of the output driver. A sense voltage is generated by passing the mirror current through the sense resistor. This voltage is then compared to a reference voltage with a comparator.

Cascode Output Driver
The output of the PWR-SMP520 is an open-drain MOSFET which carries the full primary current, but only a portion of the primary voltage. The OUT pin is connected to the source of an external 800 V MOSFET in a cascode connection as shown in Figure 4.

The benefits of cascode operation are:

- High speed operation
- Overcurrent protection
- No intermediate gate drive supply required

Relatively small, low capacitance MOSFETs such as the BUZ78A or BUK444-800A work best with the PWR-SMP520.

25 W, Universal Input Power Supply with Feedback Winding Regulation

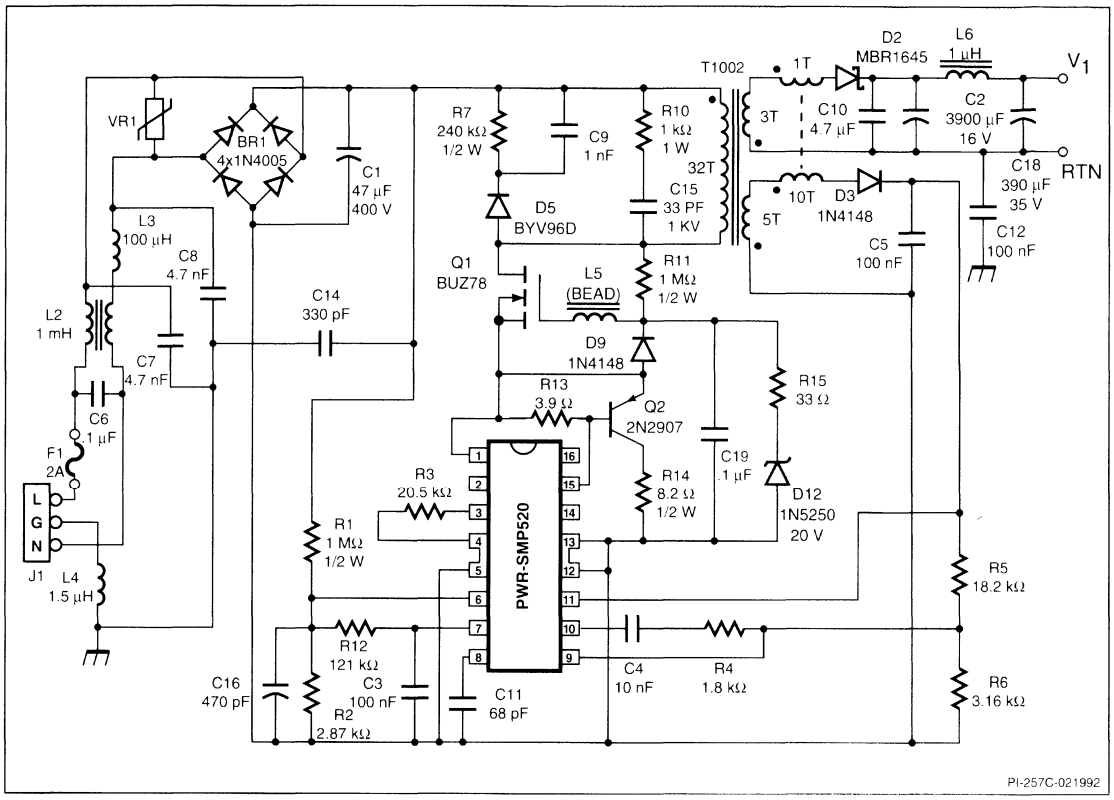


Figure 4. 25 W Universal Flyback Power Supply Using the PWR-SMP520, a bipolar shunt, and a BUZ78.

General Circuit Operation

The frequency of operation is set by C11. If no capacitance is connected to pin 8 of the PWR-SMP520, the PWM frequency will be approximately 800 kHz. Refer to the curve in the typical characteristics section.

The off time duty cycle will always be at least 50%. This fixes the amount of time the flyback transformer has to deliver the energy into the load. The long interval reduces the peak value of the secondary current and improves load regulation.

The output voltage of the feedback circuit applied to V_{BIAS} must be high enough to cut off the pre-regulator. The PWR-SMP520 has been designed to operate with a typical feedback voltage of 8.5 V.

The PWR-SMP520 switches the source of the external MOSFET to provide switch control. This technique has been used very successfully with bipolar transistors to take advantage of the high-voltage standoff capability of bipolars along with the high-speed capability of a lower voltage MOSFET. In RF circuit design, this is also well known for building very high frequency amplifiers and oscillators in the common-base or common-gate configurations.

At start-up, the external MOSFET is biased to turn on via the primary side of the transformer. Once gate voltage is available, the MOSFET provides current from its source to the pre-regulator within the PWR-SMP520, charging the bypass capacitor. When sufficient voltage is available, the PWR-SMP520 begins an orderly start-up and the OUT terminal begins to switch. Since V_{IN} is also being switched, the bypass capacitor is essential to provide internal bias during the drive pulse width. The power in the MOSFET will be minimized when the bias voltage is available from the V_{BIAS} winding. Once V_{BIAS} is available, bias from V_{IN} is cut off.

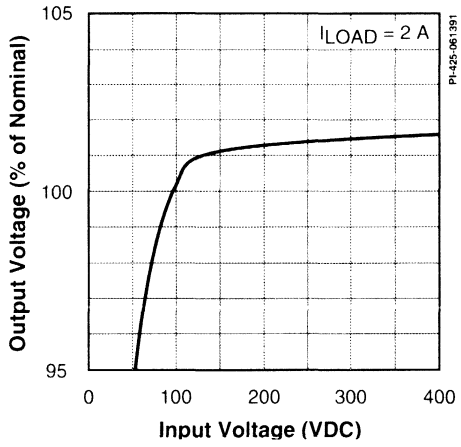
General Circuit Operation (cont.)

Additional cascode drive current is available with the addition of 3 components R13, R14 and Q2. This circuit provides a drive current in parallel with the internal cascode drive transistor. The drive current is shared by the ratio of resistance R14 to the internal series resistance of the cascode drive transistor. Current limit and output power capability is also scaled by this ratio of resistances. R13 is a small value resistor to insure fast turn off of Q2.

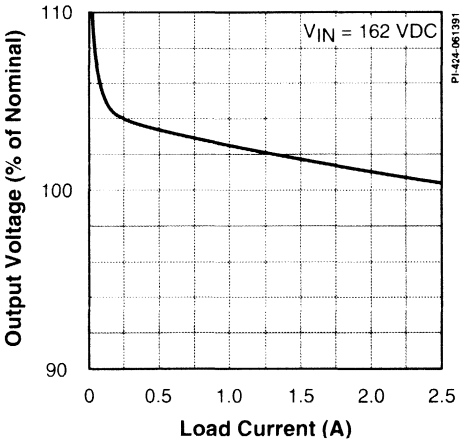
The external MOSFET should be as small a geometry as possible to insure that the gate-source capacitance is minimized. If the effective capacitance is too large, two symptoms can occur. The apparent delay at turn off with low output power can become significant, and the gate charge current spike at turn on can prematurely activate the current limit circuitry.

Typical Performance Characteristics (Figure 4 Power Supply)

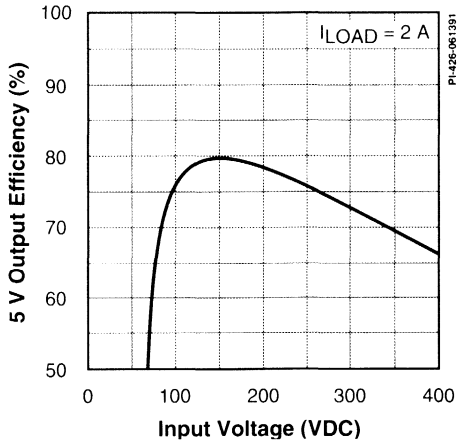
LINE REGULATION



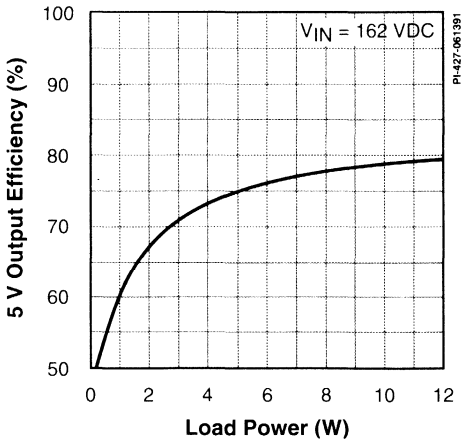
LOAD REGULATION



EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



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ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	120 V
V_{IN} Voltage	120 V
V_{BIAS} Voltage	11 V
Drain Current[2]	800 mA
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 125°C
Ambient Temperature	0 to 70°C
Junction Temperature[2]	150°C
Lead Temperature[4]	260°C
Power Dissipation (T_A = 25°C)	2.1 W
(T_A = 70°C)	1.05 W
Thermal Impedance (θ_{JA})	43°C/W
Thermal Impedance (θ_{JC})[5]	6°C/W

1. Unless noted, all voltages referenced to COM.
2. Normally limited by internal circuitry.
3. Does not apply to V_{IN} or DRAIN.
4. 1/16" from case for 5 seconds.
5. Measured at pin 12/13.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 50 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open	650	800	950	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC	C_{EXT} = Open	0-35	0-39		%
		f_{OSC} = 200 kHz	0-48	0-50		
CIRCUIT PROTECTION						
Current Limit Threshold			350	400	450	mA
Input UV Trip-off			0.29	0.34	0.39	V
Input UV Hysteresis			35	50	70	mV
Input OV Trip-off		See Note 1	1.17	1.25	1.33	V
Input OV Hysteresis			40	60	80	mV
OV/UV Turn-off Delay Time	$t_{d(off)}$	See Figure 5		250	500	ns
Thermal Shutdown Temperature			115	135		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 50 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
ERROR AMPLIFIER							
Threshold Voltage				1.21	1.25	1.29	V
Threshold Voltage Temperature Drift					50		ppm/°C
Gain-Bandwidth Product				0.9	1.0		MHz
DC Gain	A_{VOL}			60	80		dB
Output Impedance	Z_{OUT}				1.5		kΩ
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		14	16	Ω
			T_j = 115°C		21	25	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		350			mA
OFF-State Current	I_{DSS}	V_{DRAIN} = 96 V, T_A = 115°C			10	25	µA
Breakdown Voltage	BV_{DSS}	I_D = 100 µA, T_A = 25°C		120			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			22		pF
Rise Time	t_R	See Figure 5			33	100	ns
Fall Time	t_F	See Figure 5			8	15	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		120	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			6.5		8.25	V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 50 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
SUPPLY (cont.)						
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open		4	5.0	mA
		V_{BIAS} > 8.25 V			0.1	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally generated via feedback	8.25		9.0	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally generated via feedback		4	5.0	mA
V_S Source Voltage	V_S		5.1		6.0	V
V_S Source Current	I_S				400	µA

NOTES:

1. Applying >3.5 V to the OV/UV pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP520 is connected to a high voltage power source when the test circuit is activated.

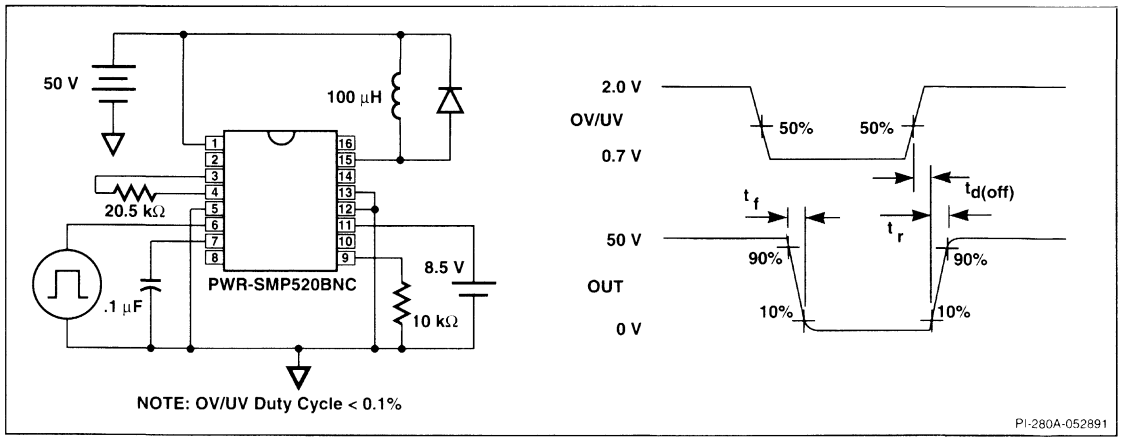
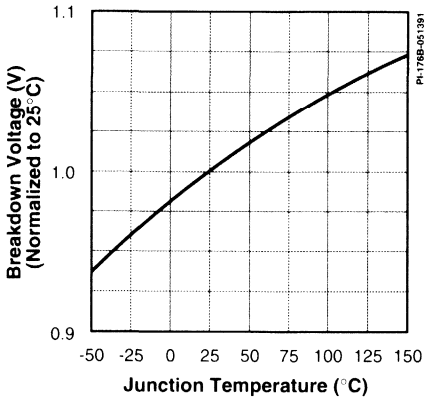
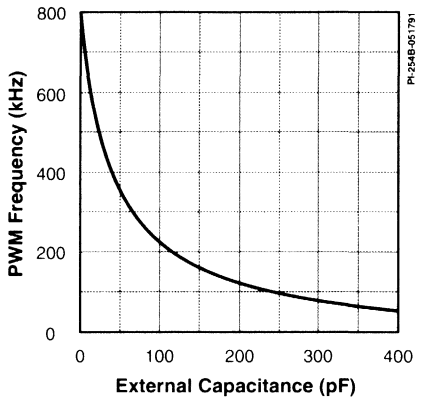


Figure 5. Switching Time Test Circuit.

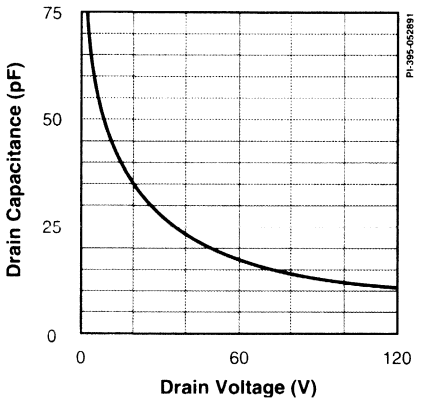
BREAKDOWN vs. TEMPERATURE



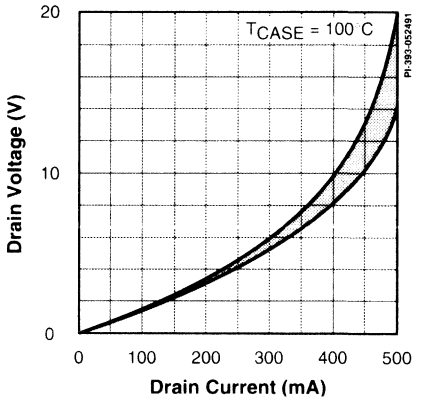
f_{PWM} vs. EXTERNAL CAPACITANCE



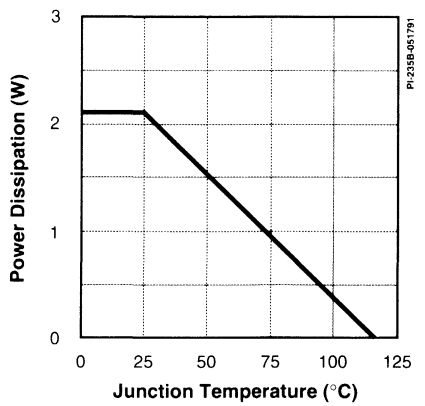
C_{OSS} vs. DRAIN VOLTAGE



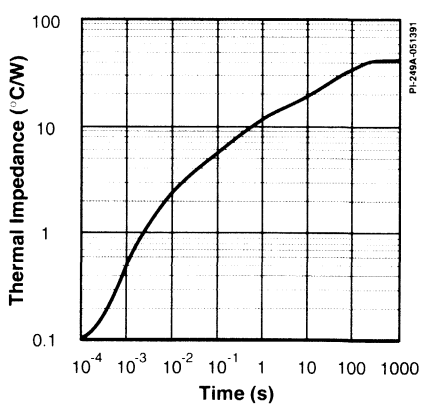
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



1

Interface Products 2

INDEX

PWR-INT200

Low-side Driver IC

Low-side Drive and High-side Control with Simultaneous Conduction Lockout

POWER INTEGRATIONS, INC.

Product Highlights

5 V CMOS Compatible Control Inputs
- Combines logic inputs for low and high-side drives
- Schmidt-triggered inputs for noise immunity

Built-in High-voltage Level Shifters
- Integrated level shifters simplify high-side interface
- Can withstand up to 800 V for direct interface to the PWR-INT201 high-side driver
- Pulsed high-voltage level shifters reduce power consumption

Gate Drive Output for an External MOSFET
- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Features
- Simultaneous conduction lockout protection
- UV lockout

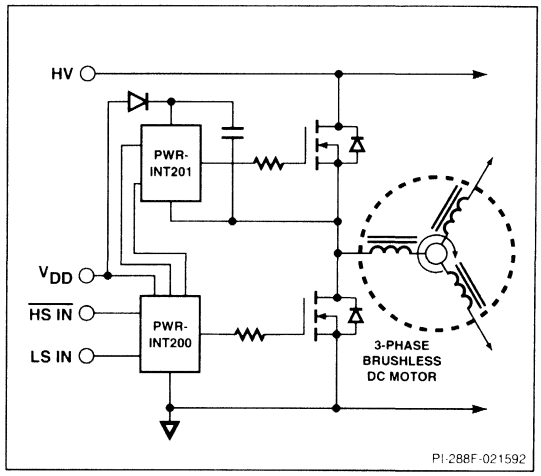


Figure 1. Typical Application

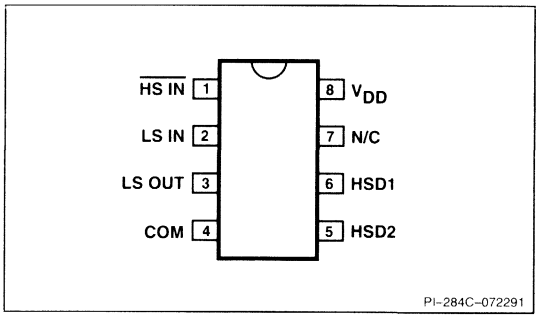


Figure 2. Pin Configuration.

Description

The PWR-INT200 Low-side driver IC provides gate drive for an external low-side MOSFET switch and high-side level shifting. When used in conjunction with the PWR-INT201 high-side driver, the PWR-INT200 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads. The PWR-INT200 is designed to be used with rectified 110 V or 220 V supplies. Both high-side and low-side switches can be controlled independently from ground-referenced 5 V logic inputs on the low side driver.

Built-in protection logic prevents both switches from turning on at the same time and shorting the high voltage supply. Pulsed level shifting saves power and provides enhanced noise immunity. The circuit is powered from a nominal 15 V supply to provide adequate gate drive for external N-channel MOSFETs.

Applications include motor drives, electronic ballasts, and uninterruptible power supplies. The PWR-INT200 can also be used to implement full- bridge and multi-phase configurations.

The PWR-INT200 is available in 8-pin plastic DIP and SOIC packages.

ORDERING INFORMATION

PART NUMBER	PACKAGE	ISOLATION VOLTAGE
PWR-INT200PFI1	8-pin PDIP	600 V
PWR-INT200TFI1	8-pin SOIC	600 V
PWR-INT200PFI2	8-pin PDIP	800 V
PWR-INT200TFI2	8-pin SOIC	800 V

Pin Functional Description

Pin 1:
Active-low logic-level input **HS IN** controls the pulse circuit which signals the PWR-INT201 high-side driver.

Pin 2:
Active-high logic level input **LS IN** controls the low side driver output.

Pin 3:
LS OUT is the driver output which controls the low-side MOSFET.

Pin 4:
COM connection; analog reference point for the circuit.

Pin 5:
Level shift output **HSD 2** signals the high-side driver to turn off. One short, precise pulse is sent on each positive transition of HS IN.

Pin 6:
Level shift output **HSD 1** signals the high-side driver to turn on. Two short, precise pulses are sent on each negative transition of HS IN.

Pin 7:
N/C for creepage distance.

Pin 8:
V_{DD} supplies power to the logic, high-side interface, and low-side driver.

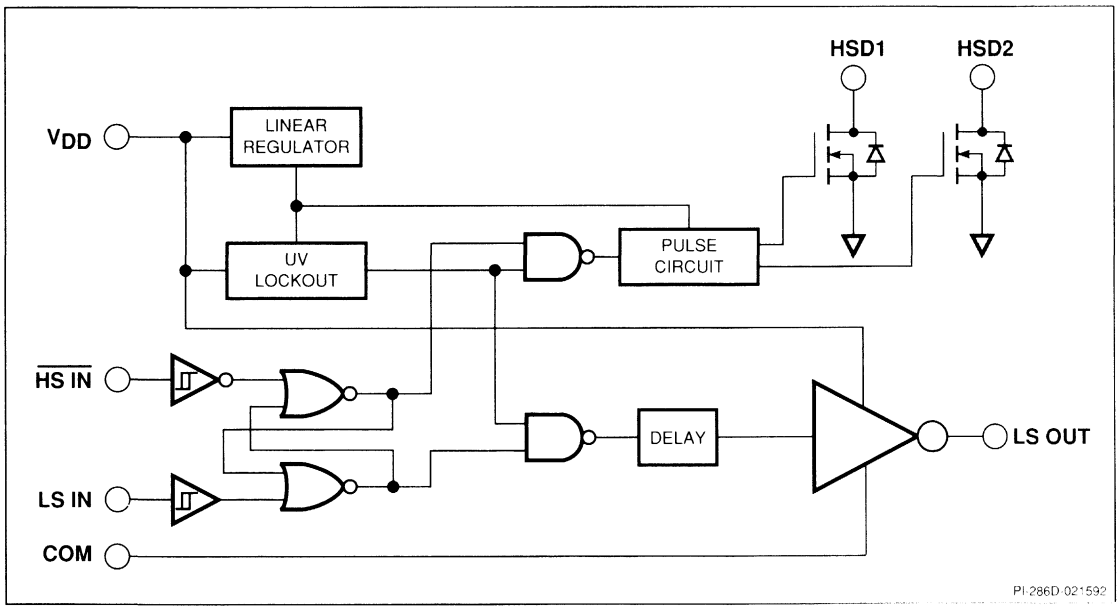


Figure 3. Functional Block Diagram of the PWR-INT200

PWR-INT200 Functional Description

5 V Regulator
The 5 V linear regulator circuit provides the supply voltage for the control logic and high-voltage level shift circuit. This allows the logic section to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

Undervoltage Lockout
The undervoltage lockout circuit disables the LS OUT pin and both HSD pins whenever the V_{DD} power supply falls below 9.25 V, and maintains this condition until the V_{DD} power supply rises above 9.5 V. This guarantees that both MOSFETs will remain off during power-up or fault conditions.

HSD1/HSD2
The HSD1 and HSD2 outputs are connected to integrated high-voltage N-channel MOSFET transistors which perform the level-shifting function for communication to the high-side driver. Controlled current capability allows the drain voltage to float with the high-side driver. Two individual channels produce a true differential communication channel for accurately controlling the high-side driver in the presence of fast moving high-voltage waveforms.

Pulse Circuit
The pulse circuit provides the two high-voltage level shifters with precise timing signals. Two pulses are sent over HSD1 to signal the high-side driver to turn on. One pulse is sent over HSD2 to signal the high-side driver to turn off. The combination of differential communication with the precise timing provides maximum immunity to noise.

Conduction Latch
An RS latch prevents the low-side driver and high-side driver from being on at the same time, regardless of the input signals.

Delay Circuit
The delay circuit matches the low-side propagation delay with the combination of the pulse circuit, high voltage level shift, and high-side driver propagation delays. This ensures that the low-side driver and high-side driver will never be on at the same time during switching transitions in either direction.

Driver
The CMOS drive circuit provides drive power to the gate of the MOSFET used on the low side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving an external transistor gate at up to 15 V.

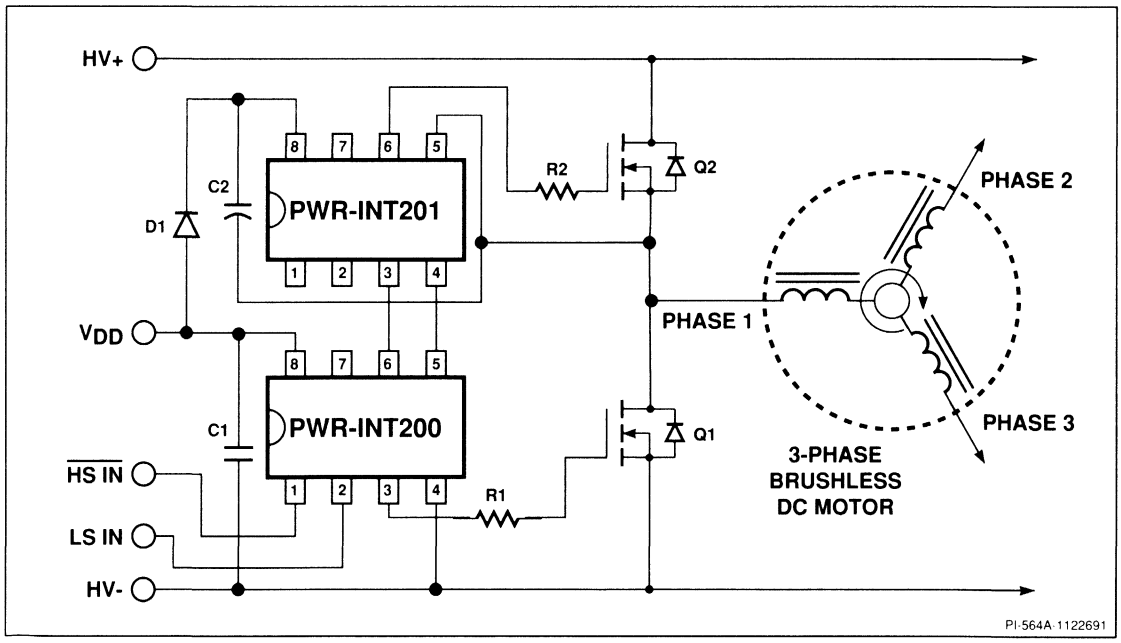


Figure 4. Using the PWR-INT200 and PWR-INT201 in a 3-phase Configuration.

General Circuit Operation

One phase of a three-phase brushless DC motor drive circuit is shown in Figure 4 to illustrate an application of the PWR-INT200/201. The LS IN signal directly controls MOSFET Q1. The HS IN signal causes the PWR-INT200 to command the PWR-INT201 to turn MOSFET Q2 on or off as required. The PWR-INT200 will ignore input signals that would command both Q1 and Q2 to conduct simultaneously, protecting against shorting the HV+ bus to HV-.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+.

The length of time that the high-side can remain on is limited by the size of the bootstrap capacitor. Applications with extremely long high-side on times require special techniques discussed in AN-10.

Maximum frequency of operation is limited by power dissipation due to high-voltage switching, gate charge, and bias power. Figure 5 indicates the maximum switching frequency as a function of input voltage and gate charge. For higher ambient temperatures, the switching frequency should be derated linearly.

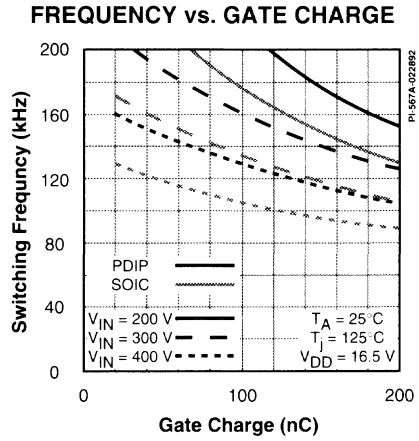


Figure 5. Gate Charge versus Switching Frequency.

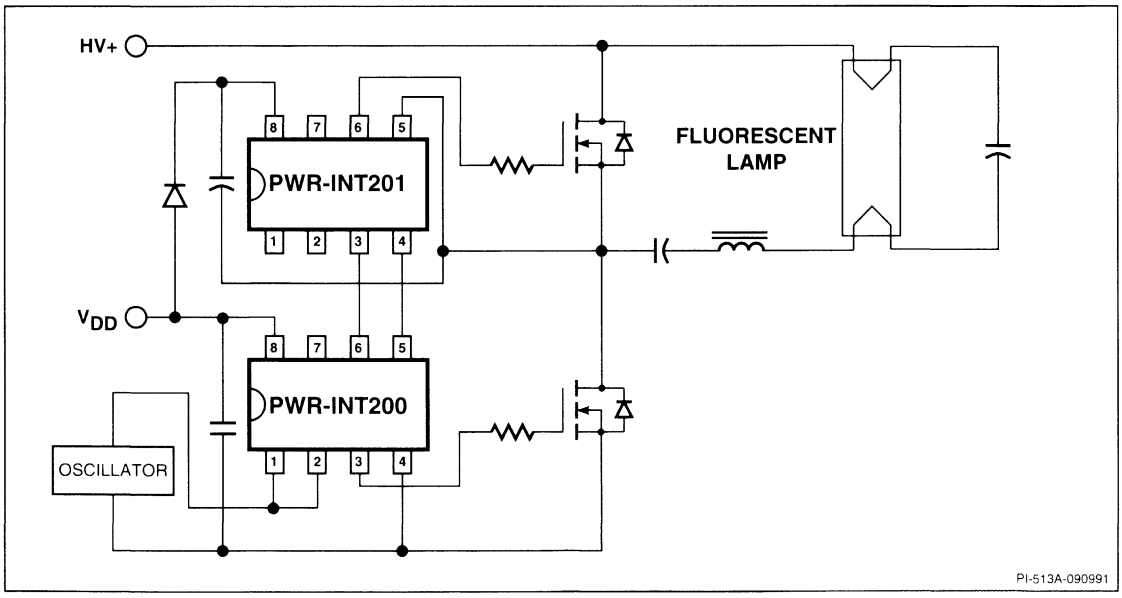


Figure 6. Using the PWR-INT200 and PWR-INT201 to Drive a Fluorescent Lamp.

ABSOLUTE MAXIMUM RATINGS[1]

HSD1/HSD2 Voltage (1 Suffix) ..... 600 V
(2 Suffix) ..... 800 V
HSD1/HSD2 Slew Rate ..... 10 V/ns
V_{DD} Voltage ..... 16.5 V
Logic Input Voltage ..... -0.3V to 5.5 V
LS OUT Voltage ..... -0.3 V to V_{DD} + 0.3 V
Storage Temperature ..... –65 to 165°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature ..... 150°C
Lead Temperature[2] ..... 260°C

Power Dissipation
PF Suffix (T_A = 25°C) ..... 1.45 W
(T_A = 70°C) ..... 940 mW
TF Suffix (T_A = 25°C) ..... 1.05 W
(T_A = 70°C) ..... 660 mW
Thermal Impedance (θ_{JA})
PF Suffix ..... 85°C/W
TF Suffix ..... 120°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 15 V, COM = 0V, T_A = -40 to 85°C	Test Limits MIN	TYP	MAX	Units
LOGIC						
Input Current, High or Low	I_{IH}, I_{IL}			0.1	5	µA
Input Voltage High	V_{IH}		4.0	3.0		V
Input Voltage Low	V_{IL}			2.3	1.0	V
Input Voltage Hysteresis	V_{HY}		0.3	0.7		V
HSD OUTPUTS						
Breakdown Voltage	BV_{DSS}	1 Suffix	600	700		V
		2 Suffix	800	900		
Off-State Output Current	$I_{HSD(OFF)}$	V_{HSD1}, V_{HSD2} = 500 V		0.1	15	µA
On-State Output Current	$I_{HSD(ON)}$	V_{HSD1}, V_{HSD2} = 10 V	5	25		mA
On-State Pulse Width	$t_{HSD(ON)}$				156	ns
Output Capacitance	C_{OSS}	V_{HSD1}, V_{HSD2} = 25 V		10		pF

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 15 V, COM = 0V, T_A = -40 to 85°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
LS OUT							
Output Voltage High	V_{OH}	I_o= -20 mA		V_{DD}-1.0	V_{DD}-0.5		V
Output Voltage Low	V_{OL}	I_o= 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_o= 0V	150			mA
			V_o= V_{DD}	300			
Turn-on Delay Time	$t_{d(on)}$	See Figure 7			0.6	1	µs
Rise Time	t_r	See Figure 7			80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 7			0.5	1	µs
Fall Time	t_f	See Figure 7			50	100	ns
SYSTEM RESPONSE							
Deadtime (Low Off to High On)	Dt_{P+}	See Figure 8		0	450		ns
Deadtime (High Off to Low On)	Dt_{P-}	See Figure 8		0	300		ns
UNDERVOLTAGE LOCKOUT							
Input UV Trip-off Voltage	$V_{DD(UV)}$			8.5	9.25	10	V
Input UV Hysteresis				175	350		mV
SUPPLY							
Supply Current	I_{DD}				1.5	3.0	mA
Supply Voltage	V_{DD}			10		16	V

NOTES:

1. Applying a short circuit to the LS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.

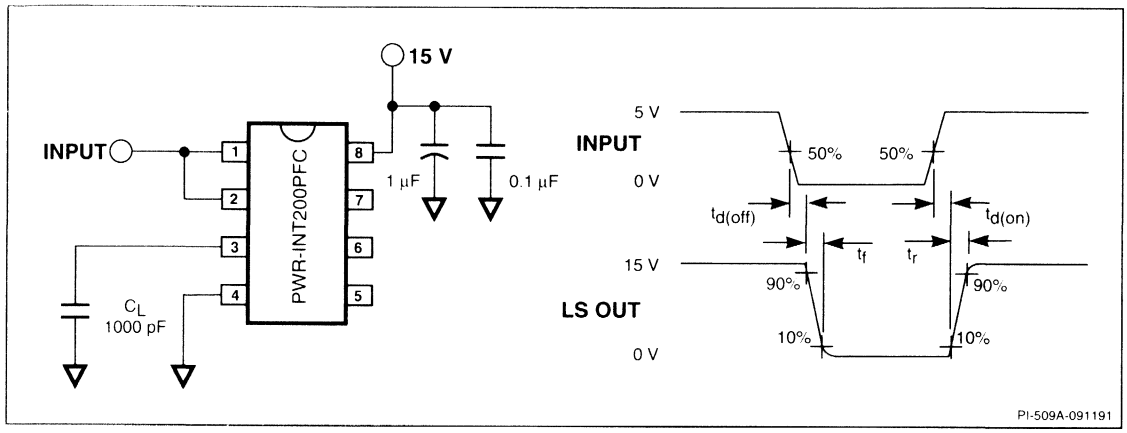


Figure 7. Switching Time Test Circuit.

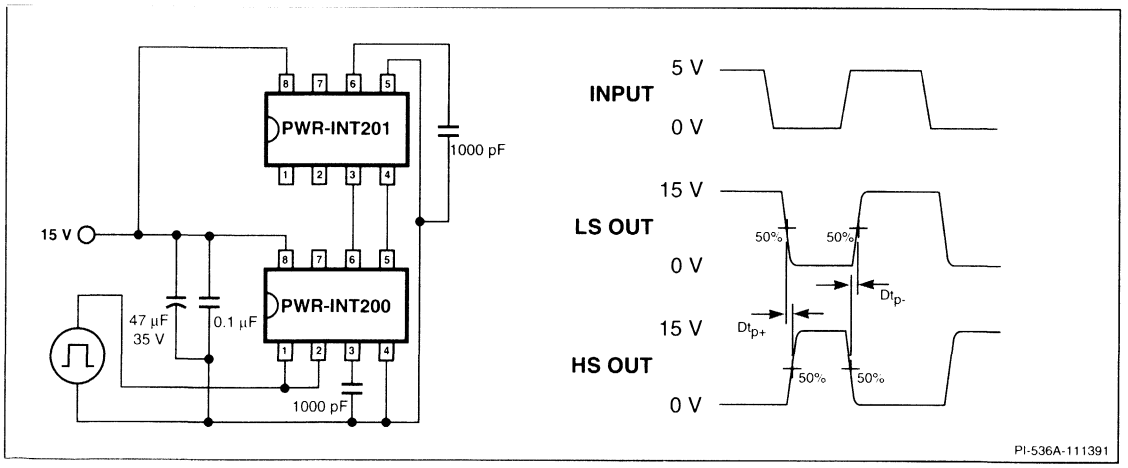
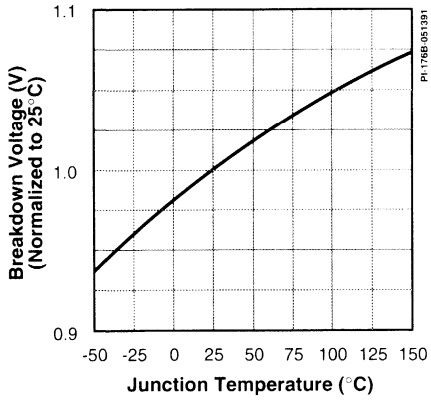
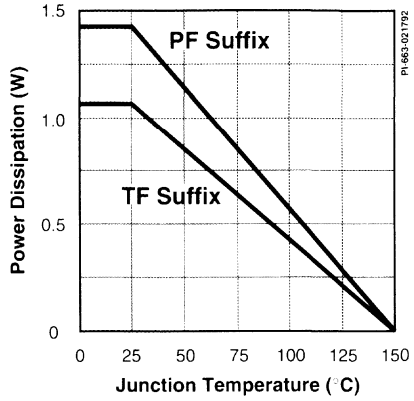


Figure 8. Dead Time Test Circuit.

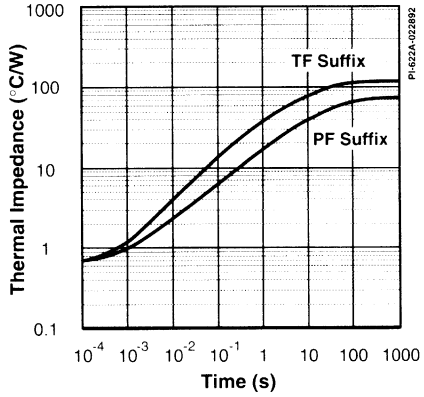
BREAKDOWN vs. TEMPERATURE



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-INT201

High-side Driver IC

Floating Inputs
Floating High-side Drive

Product Highlights

Floating Control Inputs
- Connects directly to PWR-INT200 or PWR-INT202 HSD outputs
- No external level translators or transformers required

Gate Drive Output for an External MOSFET
- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- Floating source for driving high-side N-channel MOSFET
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Circuits
- Logic inputs include noise rejection circuitry
- Undervoltage lockout

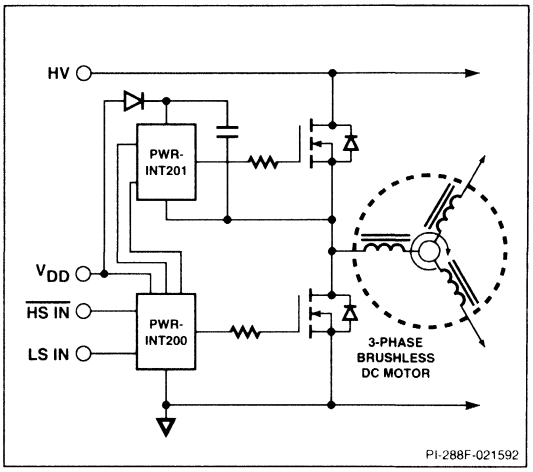


Figure 1. Typical Application.

Description

The PWR-INT201 high-side driver IC provides gate drive for an external high-side MOSFET switch. When used in conjunction with the PWR-INT200 or PWR-INT202 low-side drivers, the PWR-INT201 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads.

Built-in noise rejection circuitry shared between the PWR-INT201 and the PWR-INT200 or PWR-INT202 provides reliable operation in the harshest industrial environments. The PWR-INT201 is powered from a ground-referenced low-voltage supply. A floating supply is derived from this rail by using a simple bootstrap technique to provide adequate gate drive for the external N-channel MOSFET.

Applications include motor drives, electronic ballasts, and uninterruptible power supplies. ThePWR-INT201 can also be used to implement full- bridge and multi-phase configurations.

The PWR-INT201 is available in 8-pin plastic DIP and SOIC packages.

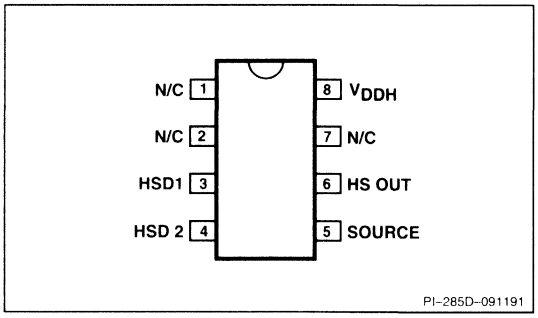


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-INT201PFI	8-pin PDIP	-40 to 85°C
PWR-INT201TFI	8-pin SOIC	-40 to 85°C

Pin Functional Description

Pin 1:
No connection.

Pin 2:
No connection.

Pin 3:
Level shift input **HSD 1** works in conjunction with HSD 2 to provide interface from the low side control logic and to give noise immunity.

Pin 4:
Level shift input **HSD 2** works in conjunction with HSD 1 to provide interface from the low side control logic and to give noise immunity.

Pin 5:
SOURCE connection. Analog reference point for the circuit, normally connected to the source of the high side MOSFET.

Pin 6:
HS OUT is the output of the MOSFET driver for the high side.

Pin 7:
No connection.

Pin 8:
V_{DDH} supplies power to the control logic and output driver.

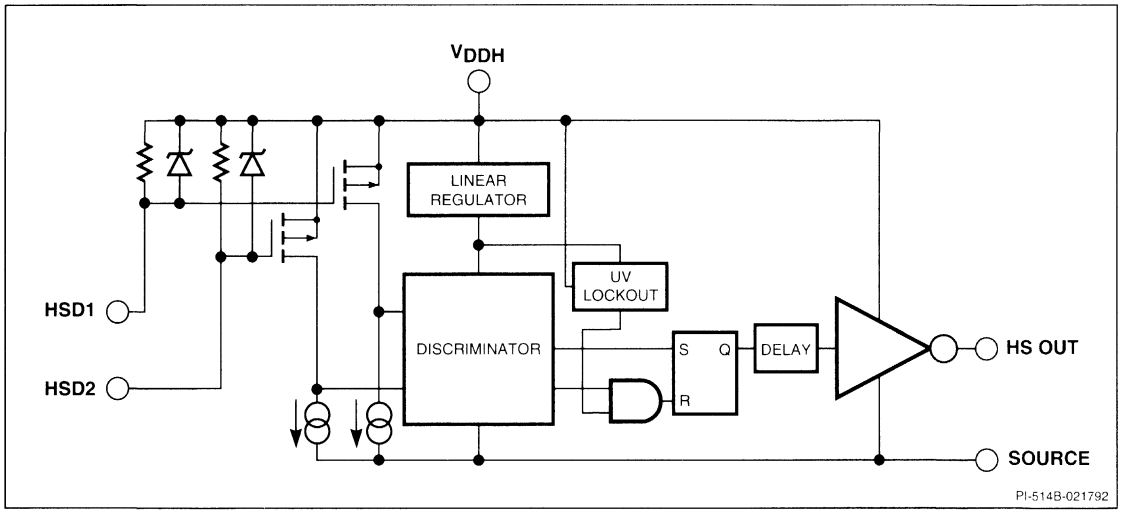


Figure 3. Functional Block Diagram of the PWR-INT201.

PWR-INT201 Functional Description

5 V Regulator
The 5 V linear regulator circuit provides the supply voltage for the noise rejection circuitry and control logic. This allows the logic section and the driver circuitry to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

Undervoltage Lockout
The undervoltage lockout circuit disables the HS OUT pin whenever the V_{DDH} power supply falls below 9.25 V, and maintains this condition until the V_{DDH} power supply rises above 9.5 V. This guarantees that the high side MOSFET will be off during power-up or fault conditions.

Noise Immunization Circuit
This circuit provides noise immunity by combining a sampling circuit with a flip-flop to turn on and off the driver only when required to and not when there is noise on the HSD inputs.

Driver
The CMOS driver circuit provides drive power to the gate of the MOSFET used on the high side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving external transistors at up to 15 V. The SOURCE pin is connected to the source of the external MOSFET to establish a reference for the gate voltage.

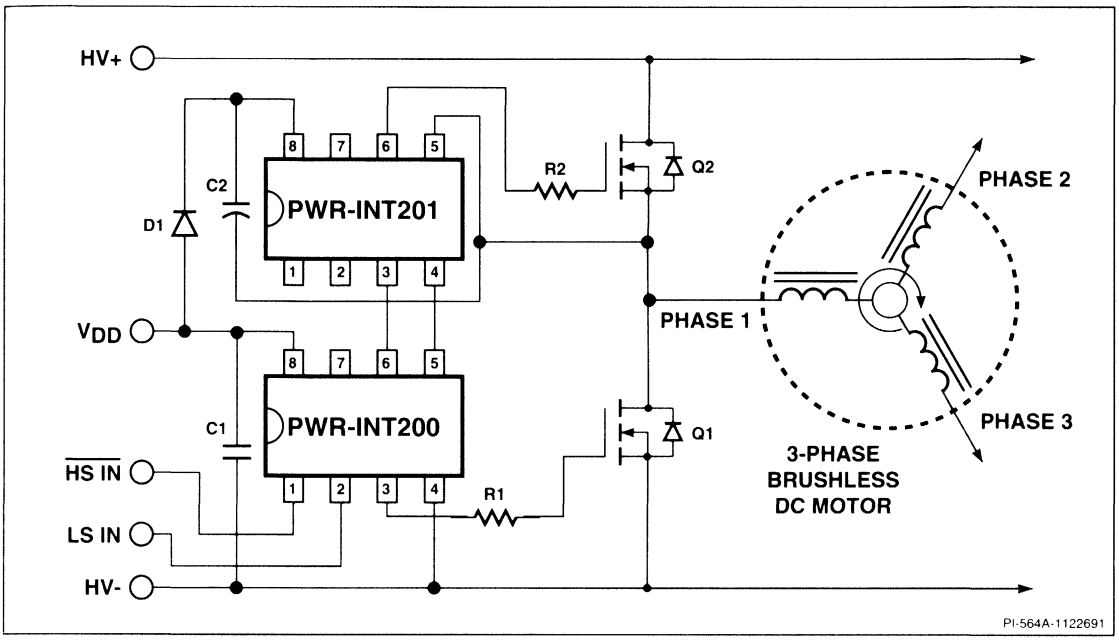


Figure 4. Using the PWR-INT200 and PWR-INT201 in a 3-phase Configuration.

General Circuit Operation

One phase of a three-phase brushless DC motor drive circuit is shown in Figure 4 to illustrate an application of the PWR-INT200/201. The LS IN signal directly controls MOSFET Q1. The HS IN signal causes the PWR-INT200 to command the PWR-INT201 to turn MOSFET Q2 on or off as required. The PWR-INT200 will ignore input signals that would command both Q1 and Q2 to conduct simultaneously, protecting against shorting the HV+ bus to HV-.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+.

The PWR-INT201 is latched on and off by the edges of the appropriate low-side logic signal ($\overline{\text{HS IN}}$ for the PWR-INT200, and HS IN for the PWR-INT202). The high-side driver will latch off and stay off if the bootstrap capacitor discharges below the undervoltage lockout threshold. Undervoltage lockout-induced turn off can occur during conditions such as power ramp up, motor start, or low speed operation.

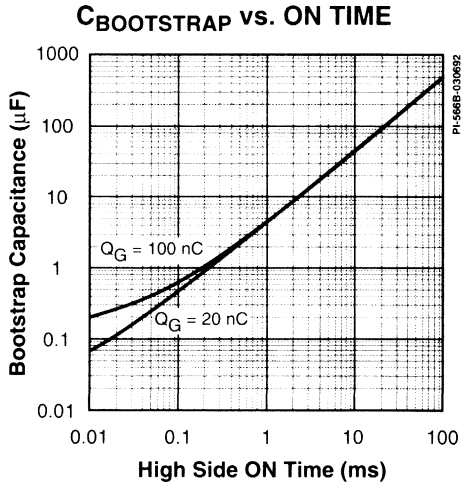


Figure 5. High-side On Time versus Bootstrap Capacitor.

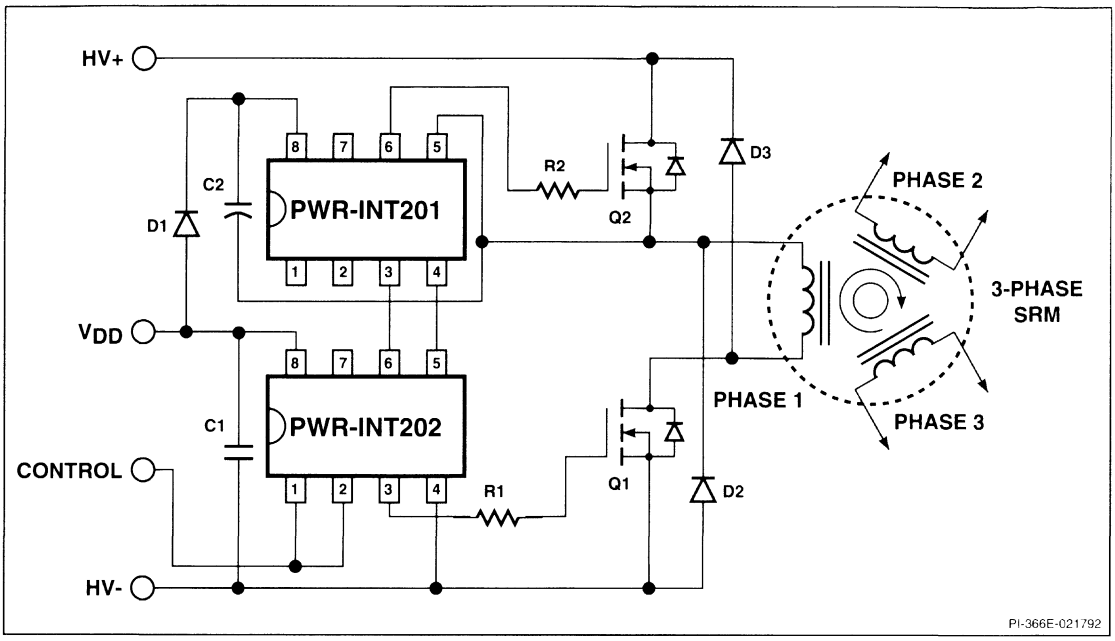


Figure 6. Using the PWR-INT202 and PWR-INT201 to Drive a Switched Reluctance Motor.

General Circuit Operation (cont.)

The bootstrap capacitor must be large enough to provide bias current over the entire on time interval of the high-side driver without significant voltage sag or decay. The MOSFET gate charge must also be supplied at the desired switching frequency. Figure 5 shows the maximum high-side on time versus gate charge of the external MOSFET. Applications with extremely long high-side on times require special techniques discussed in AN-10.

A three-phase switched reluctance motor example using the PWR-INT202/201 is given in Figure 6. The LS IN signal directly controls MOSFET Q1. Unlike the PWR-INT200, the PWR-INT202 allows both the low and high-side drivers to be on at the same time, as this is required in applications where the load is placed between the low and high-side output MOSFETs.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DDH} Voltage ..... 16.5 V
Logic Input Voltage ..... -0.3 V to 5.5 V
HS OUT Voltage ..... -0.3 V to V_{DDH} + 0.3 V
Storage Temperature ..... -65 to 165°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature. ..... 150°C
Lead Temperature[2]. ..... 260°C

Power Dissipation
PF Suffix (T_A = 25°C) ..... 1.25 W
PF Suffix (T_A = 70°C) ..... 800 mW
TF Suffix (T_A = 25°C) ..... 1.05 W
TF Suffix (T_A = 70°C) ..... 660 mW
Thermal Impedance (θ_{JA})
PF Suffix ..... 100°C/W
TF Suffix ..... 120°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DDH} = 15 V, SOURCE = 0V, T_A = -40 to 85°C		Test Limits MIN	TYP	MAX	Units
HSD INPUTS							
Input Current Threshold	I_{HSD1}, I_{HSD2}				2.5	5	mA
HS OUT							
Output Voltage, High	V_{OH}	I_o = -20 mA		V_{DDH}-1.0	V_{DDH}-0.5		V
Output Voltage, Low	V_{OL}	I_o = 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_O = 0 V	150			mA
			V_O = V_{DDH}	300			
Turn-on Delay Time	$t_{d(on)}$	See Figure 7			1.0	1.5	µs
Rise Time	t_r	See Figure 7			80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 7			420	600	ns
Fall Time	t_f	See Figure 7			50	100	ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DDH} = 15 V, SOURCE = 0V, T_A = -40 to 85°C	Test Limits MIN	TYP	MAX	Units
SYSTEM RESPONSE						
Deadtime (Low Off to High On)	Dt_{P+}	See Figure 8	0	450		ns
Deadtime (Low On to High Off)	Dt_{P-}	See Figure 8	0	300		ns
Matching (Low On to High On)	Mt_{P+}	See Figure 9		0.3	1	µs
Matching (Low Off to High Off)	Mt_{P-}	See Figure 9		0.3	1	µs
UNDERVOLTAGE LOCKOUT						
Input UV Threshold Voltage	$V_{DDH(UV)}$		8.5	9.25	10	V
Input UV Hysteresis			175	350		mV
SUPPLY						
Supply Current	I_{DDH}			1.5	3.0	mA
Supply Voltage	V_{DDH}		10		16	V

NOTES:

1. Applying a short circuit to the HS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.

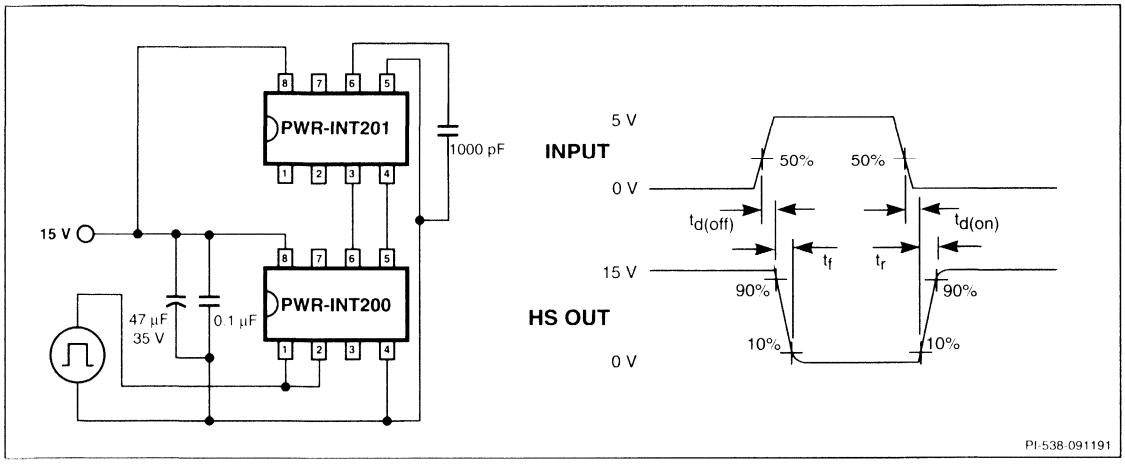


Figure 7. Switching Time Test Circuit.

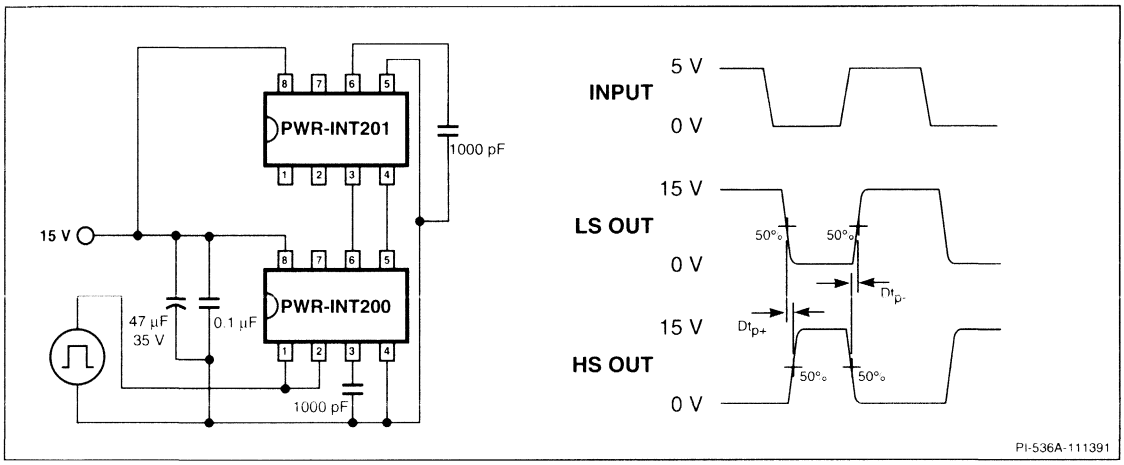


Figure 8. Dead Time Test Circuit.

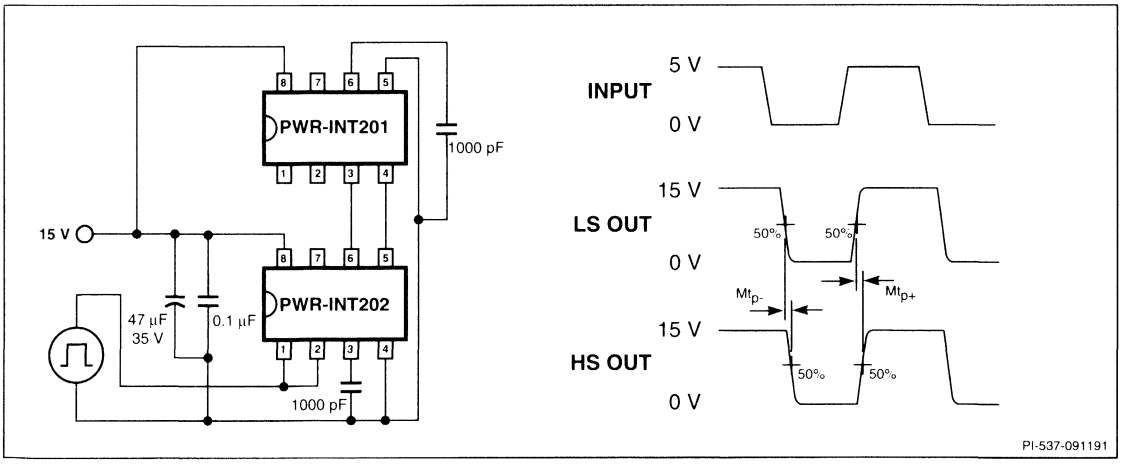
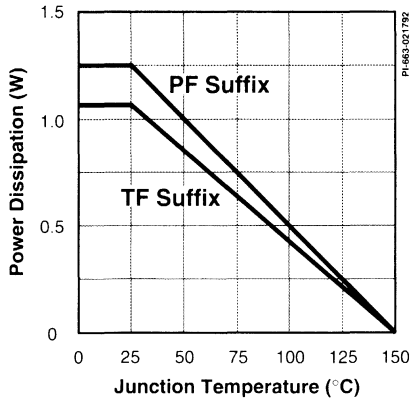


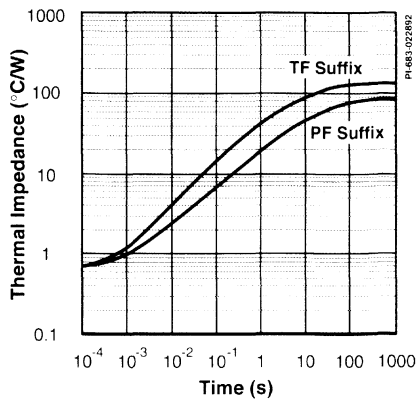
Figure 9. Matching Test Circuit.

2

PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-INT202

Low-side Driver IC

Low-side Drive and High-side Control for Simultaneous Conduction

POWER INTEGRATIONS, INC.

Product Highlights

5 V CMOS Compatible Control Inputs
- Combines logic inputs for low and high-side drives
- Schmidt-triggered inputs for noise immunity

Built-in High-voltage Level Shifters
- Integrated level shifters simplify high-side interface
- Can withstand up to 800 V for direct interface to the PWR-INT201 high-side driver
- Pulsed high-voltage level shifters reduce power consumption

Gate Drive Output for an External MOSFET
- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Features
- UV lockout

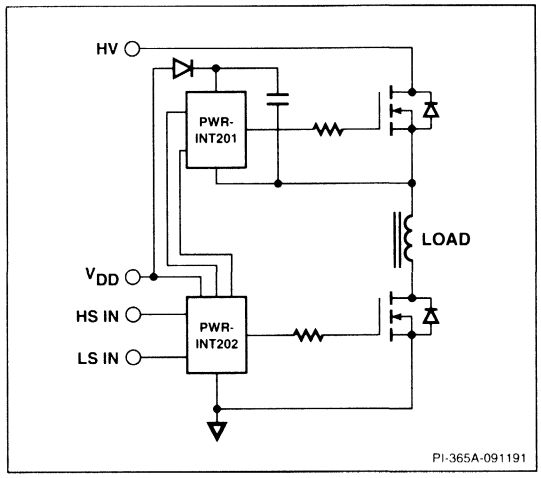


Figure 1. Typical Application

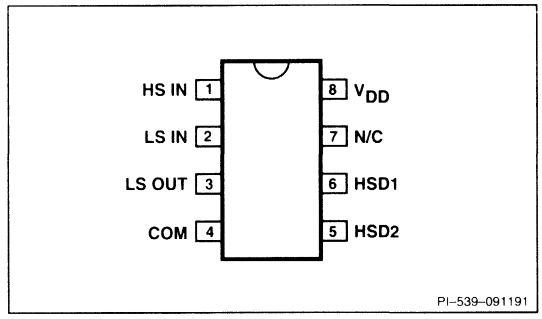


Figure 2. Pin Configuration.

Description

The PWR-INT202 Low-side driver IC provides gate drive for an external low-side MOSFET switch and high-side level shifting. When used in conjunction with the PWR-INT201 high-side driver, the PWR-INT202 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads. The PWR-INT202 is designed to be used with rectified 110 V or 220 V supplies. Both high side and low side switches can be controlled independently from ground-referenced 5 V logic inputs on the low side driver.

Pulsed level shifting saves power and provides enhanced noise immunity. The circuit is powered from a nominal 15 V supply to provide adequate gate drive for external N-channel MOSFETs.

Applications include switched reluctance motor drives. The PWR-INT202 can also be used to implement multi-phase configurations.

The PWR-INT202 is available in 8-pin plastic DIP and SOIC packages.

ORDERING INFORMATION

PART NUMBER	PACKAGE	ISOLATION VOLTAGE
PWR-INT202PFI1	8-pin PDIP	600 V
PWR-INT202TFI1	8-pin SOIC	600 V
PWR-INT202PFI2	8-pin PDIP	800 V
PWR-INT202TFI2	8-pin SOIC	800 V

Pin Functional Description

Pin 1:
Active-high logic-level input **HS IN** controls the pulse circuit which signals the PWR-INT201 high-side driver.

Pin 2:
Active-high logic level input **LS IN** controls the low side driver output.

Pin 3:
LS OUT is the driver output which controls the low-side MOSFET.

Pin 4:
COM connection: analog reference point for the circuit.

Pin 5:
Level shift output **HSD 2** signals the high-side driver to turn off. One short, precise pulse is sent on each positive transition of HS IN.

Pin 6:
Level shift output **HSD 1** signals the high-side driver to turn on. Two short, precise pulses are sent on each negative transition of HS IN.

Pin 7:
N/C for creepage distance.

Pin 8:
V_{DD} supplies power to the logic, high-side interface, and low-side driver.

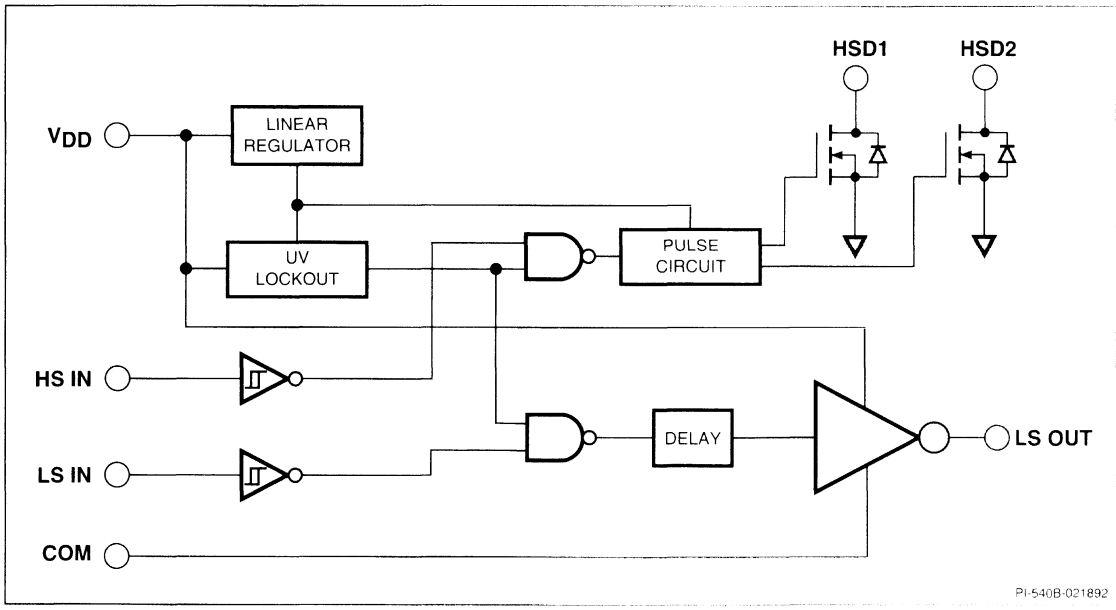


Figure 3. Functional Block Diagram of the PWR-INT202

PWR-INT202 Functional Description

5 V Regulator
The 5 V linear regulator circuit provides the supply voltage for the control logic and high-voltage level shift circuit. This allows the logic section to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

Undervoltage Lockout
The undervoltage lockout circuit disables the LS OUT pin and both HSD pins whenever the V_{DD} power supply falls below 9.25 V, and maintains this condition until the V_{DD} power supply rises above 9.5 V. This guarantees that both MOSFETs will remain off during power-up or fault conditions.

HSD1/HSD2
The HSD1 and HSD2 outputs are connected to integrated high-voltage N-channel MOSFET transistors which perform the level-shifting function for communication to the high-side driver. Controlled current capability allows the drain voltage to float with the high-side driver. Two individual channels produce a true differential communication channel for accurately controlling the high-side driver in the presence of fast moving high-voltage waveforms.

Pulse Circuit
The pulse circuit provides the two high-voltage level shifters with precise timing signals. Two pulses are sent over HSD1 to signal the high-side driver to turn on. One pulse is sent over HSD2 to signal the high-side driver to turn off. The combination of differential communication with the precise timing provides maximum immunity to noise.

Driver
The CMOS drive circuit provides drive power to the gate of the MOSFET used on the low side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving an external transistor gate at up to 15 V.

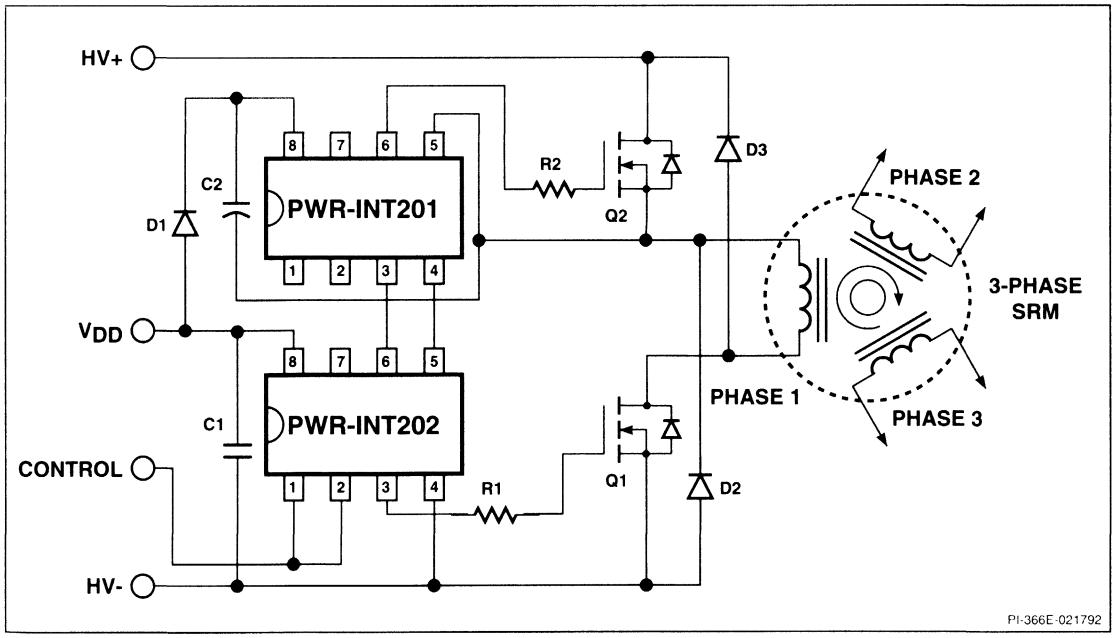


Figure 4. Using the PWR-INT202 and PWR-INT201 to Drive a Switched Reluctance Motor.

General Circuit Operation

The three-phase switched reluctance motor drive circuit shown in Figure 4 illustrates a typical application for the PWR-INT202/201. The LS IN signal directly controls MOSFET Q1. The HS IN signal causes the PWR-INT202 to command the PWR-INT201 to turn MOSFET Q2 on or off as required.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+.

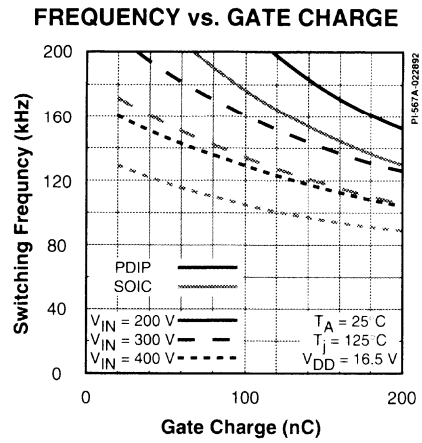


Figure 5. Gate Charge versus Switching Frequency.

The length of time that the high-side can remain on is limited by the size of the bootstrap capacitor. Applications with extremely long high-side on times require special techniques discussed in AN-10.

Maximum frequency of operation is limited by power dissipation due to high-voltage switching, gate charge, and bias power. Figure 5 indicates the maximum switching frequency as a function of input voltage and gate charge. For higher ambient temperatures, the switching frequency should be derated linearly.

ABSOLUTE MAXIMUM RATINGS[1]

HSD1/HSD2 Voltage (1 Suffix) ..... 600 V
(2 Suffix) ..... 800 V
HSD1/HSD2 Slew Rate ..... 10 V/ns
V_{DD} Voltage ..... 16.5 V
Logic Input Voltage ..... -0.3V to 5.5 V
LS OUT Voltage ..... -0.3 V to V_{DD} + 0.3 V
Storage Temperature ..... -65 to 165°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature ..... 150°C
Lead Temperature[2] ..... 260°C

Power Dissipation
PF Suffix (T_A = 25°C) ..... 1.45 W
(T_A = 70°C) ..... 940 mW
TF Suffix (T_A = 25°C) ..... 1.05 W
(T_A = 70°C) ..... 660 mW
Thermal Impedance (θ_{JA})
PF Suffix ..... 100°C/W
TF Suffix ..... 120°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 15 V, COM = 0V, T_A = -40 to 85°C	Test Limits MIN	TYP	MAX	Units
LOGIC						
Input Current, High or Low	I_{IH}, I_{IL}			0.1	5	µA
Input Voltage High	V_{IH}		4.0	3.0		V
Input Voltage Low	V_{IL}			2.3	1.0	V
Input Voltage Hysteresis	V_{HY}		0.3	0.7		V
HSD OUTPUTS						
Breakdown Voltage	BV_{DSS}	1 Suffix	600	700		V
		2 Suffix	800	900		
Off-State Output Current	$I_{HSD(OFF)}$	V_{HSD1}, V_{HSD2} = 500 V		0.1	15	µA
On-State Output Current	$I_{HSD(ON)}$	V_{HSD1}, V_{HSD2} = 10 V	5	25		mA
On-State Pulse Width	$t_{HSD(ON)}$				156	ns
Output Capacitance	C_{OSS}	V_{HSD1}, V_{HSD2} = 25 V		10		pF

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 15 V, COM = 0V, T_A = -40 to 85°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
LS OUT							
Output Voltage High	V_{OH}	I_o= -20 mA		V_{DD}-1.0	V_{DD}-0.5		V
Output Voltage Low	V_{OL}	I_o= 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_o= 0V	150			mA
			V_o= V_{DD}	300			
Turn-on Delay Time	$t_{d(on)}$	See Figure 6			0.6	1	µs
Rise Time	t_r	See Figure 6			80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 6			0.5	1	µs
Fall Time	t_f	See Figure 6			50	100	ns
SYSTEM RESPONSE							
Matching (Low On to High On)	Mt_{P+}	See Figure 7			0.3	1	µs
Matching (Low Off to High Off)	Mt_{P-}	See Figure 7			0.3	1	µs
UNDERVOLTAGE LOCKOUT							
Input UV Trip-off Voltage	$V_{DD(UV)}$			8.5	9.25	10	V
Input UV Hysteresis				175	350		mV
SUPPLY							
Supply Current	I_{DD}				1.5	3.0	mA
Supply Voltage	V_{DD}			10		16	V

NOTES:

1. Applying a short circuit to the LS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.

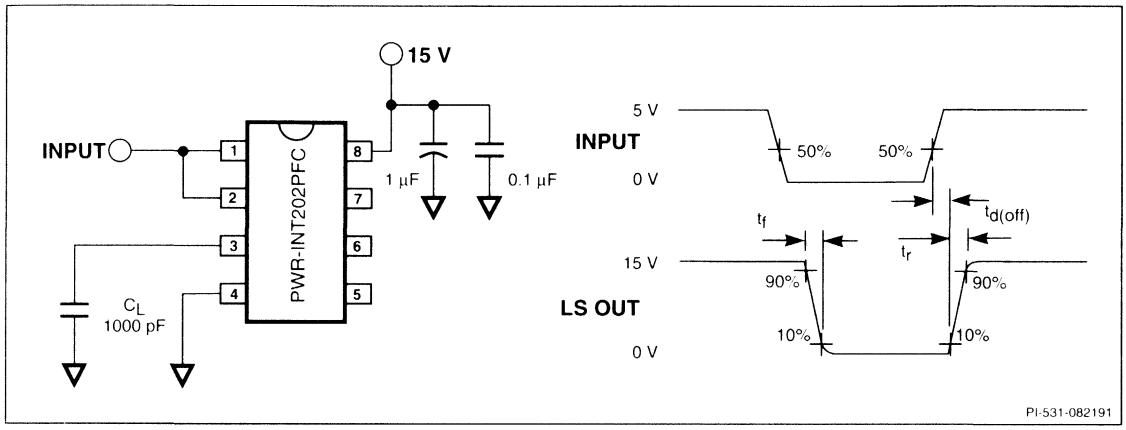


Figure 6. Switching Time Test Circuit.

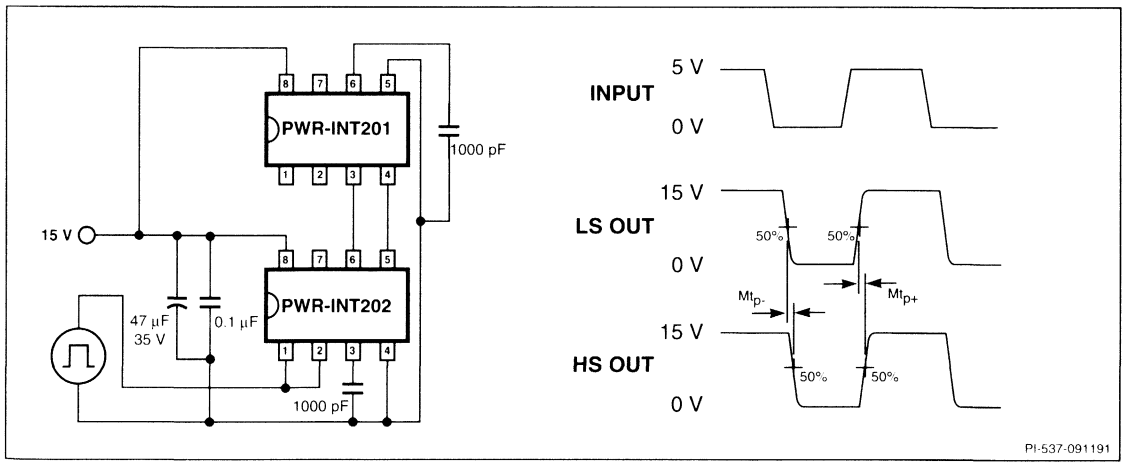
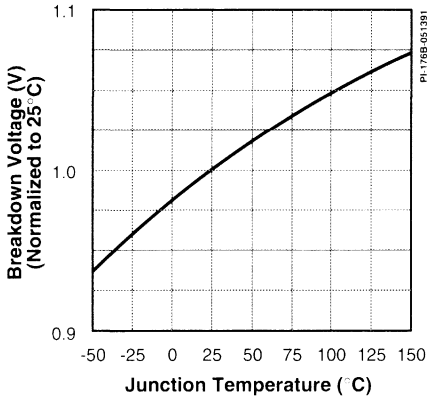
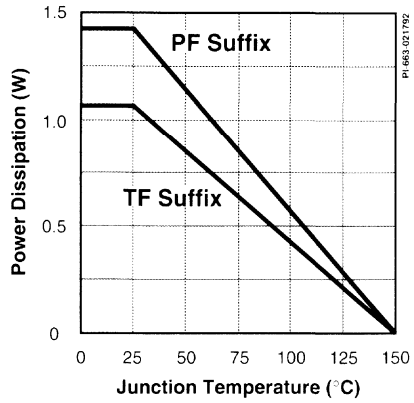


Figure 7. Matching Test Circuit.

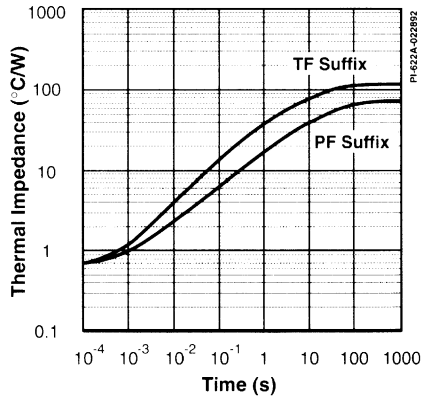
BREAKDOWN vs. TEMPERATURE



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



PWR-INT600

Serial-to-Parallel Converter

5V CMOS Serial Input
64 High-Voltage Outputs

POWER INTEGRATIONS, INC.

Product Highlights

High-performance Logic Circuits

- High-speed shift register handles data rates up to 6 MHz
- Bi-directional shift register allows left- or right-hand shift
- Buffered input latch holds one line of data while next line is being loaded
- 5 V CMOS-compatible inputs

64 High-voltage Open-drain Outputs

- 375 V minimum standoff voltage
- Low leakage
- Direct 5 V gate drive eliminates the need for an intermediate level translator

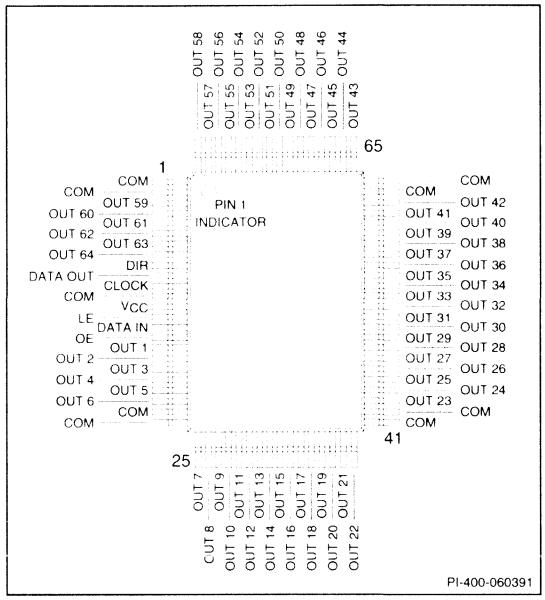


Figure 1. Pin Configuration

Description

The PWR-INT600 is a low-voltage serial to high-voltage parallel converter with 64 open-drain outputs capable of driving capacitive loads such as electrostatic printers and plotters, and flat-panel displays.

The low-voltage logic section of the PWR-INT600 contains a 64-bit bi-directional shift register, 64 latches, and Output Enable (OE) control logic. Data is shifted into the shift register on the falling edge of each CLOCK pulse. The DIR pin controls direction of the data through the shift register, allowing for either left-to-right or right-to-left shift. Transfer of data from the shift register to the latch is controlled by the LE pin.

Each output of the PWR-INT600 is an open-drain MOSFET capable of withstanding 375 V in the OFF-state. The slew rate of the turn-on and turn-off have been limited by internal circuitry to minimize system noise.

The PWR-INT600 is available is an 80-pin gullwing quad flat-pack (QFP) package.

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**TEMP RANGE**
PWR-INT600EYC	80-pin Gullwing QFP	0 to 70°C

2

Pin Functional Description

Pin 1, 2:
COM connections. Ground or reference point for the open-drain outputs.

Pin 3-8:
Open-drain of the outputs for channels 59 through 64.

Pin 9:
The direction of data flow through the shift register is determined by the **DIR** pin (see Figure 3).

Pin 10:
DATA OUT is the output of the shift register. DATA OUT of one device can be connected to DATA IN of another device to form a "daisy chain" serial data path.

Pin 11:
The movement of data through the shift register is controlled by the **CLOCK** pin (see Figure 3).

Pin 12:
COM connection. Digital input reference.

Pin 13:
V_{CC} is the low-voltage supply for the logic and driver sections.

Pin 14:
LE controls the movement of data from the shift register to the latch (see Figure 3).

Pin 15:
DATA IN is the input of the shift register. DATA OUT of one device can be connected to DATA IN of another device to form a "daisy chain" serial data path.

Pin 16:
OE controls when the data in the latch can be passed to the outputs (see Figure 3).

Pin 17-22:
Open-drain of the outputs for channels 1 through 6.

Pin 23, 24:
COM connections. Ground or reference point for the open-drain outputs.

Pin 25-40:
Open-drain of the outputs for channels 7 through 22.

Pin 41, 42:
COM connections. Ground or reference point for the open-drain outputs.

Pin 43-62:
Open-drain of the outputs for channels 23 through 42.

Pin 63, 64:
COM connections. Ground or reference point for the open-drain outputs.

Pin 65-80:
Open-drain of the outputs for channels 43 through 58.

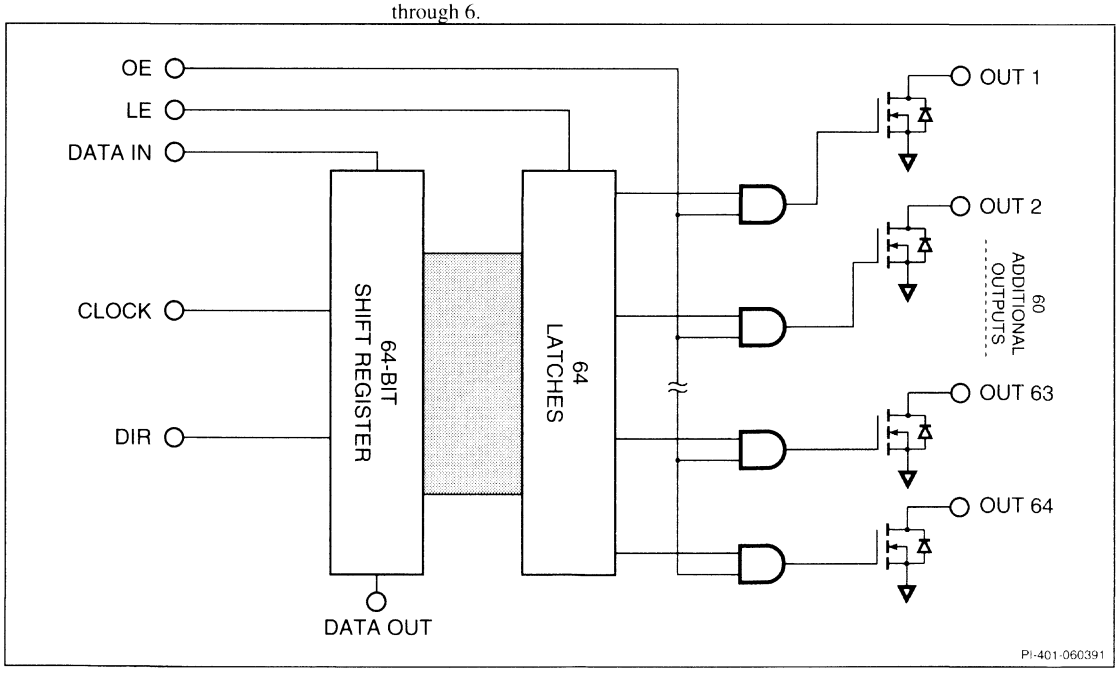


Figure 2. Functional Block Diagram of the PWR-INT600.

FUNCTION	CLOCK	DIR	SHIFT REGISTER	DATA OUT	LE	LATCHES	OE	OUTPUTS
LOAD	↓	H	$OUT_N \rightarrow OUT_{N+1}$	OUT 64	X	DETERMINED	X	DETERMINED
		L	$OUT_N \rightarrow OUT_{N-1}$	OUT1	X	BY	X	
	NO ↓	X	NC	NC	X	LE	X	BY
LATCH	X	X	DETERMINED BY CLOCK		L	HOLD DATA	X	OE
	X	X			H	LOAD DATA	X	
OUTPUT ENABLE	X	X			X	DETERMINED BY LE	L	ALL HIGH
	X	X			X		H	HIGH or LOW*

NOTES:

X - Don't Care
H - Logic 1
L - Logic 0

↓ - Falling Edge
NC - No Change
* - Depends on contents of Latch

Logic 0 in Shift Register/Latch leaves output floating
Logic 1 in Shift Register/Latch pulls the output to COM

Figure 3. Truth Table for the PWR-INT600.

PWR-INT600 Functional Description

Typical Applications
The high channel count and high-speed data transfer rate of the PWR-INT600 make it ideal for driving large arrays of high-voltage capacitive elements, such as those found in flat-panel displays, printers, and electrostatic plotters.

Digital Input Section
The digital logic section of the PWR-INT600 is made up of a serial-input 64-bit shift register, a 64-bit latch, and 64 output drivers.

Shift Register - Data is shifted through the register via the DATA IN pin on each falling edge of the CLOCK input. The DIR pin controls the direction of data flow through the shift register, allowing for either right-or left-hand shift versions from one part. The DATA OUT pin of one device can be connected to DATA IN on the next device to provide a continuous data pipeline for larger arrays.

Latch - The latch is vital to high-speed applications, allowing the output of one line of data to the load while simultaneously shifting in the next line. When LE is low, the latch holds the data from the last time the latch was enabled. New data is loaded from the contents of the shift register when LE is brought high. Note that the latch is transparent, i.e., until LE is brought low again, any changes in the contents of the shift register will flow through to the latch. Also, the logic gates within the shift register and latch have been designed to hold all lows (logic 0) when power is first applied. This will insure that outputs do not come up in an unknown state on power-up.

Output Enable - Usually, the application requires that all the outputs change state at the same time. All 64 output drivers are controlled by the OE pin. When OE is low, all of the outputs are off, which pulls the outputs to the high-voltage rail. When OE is high, the outputs will be on or off, depending on the data that is in the latch at the time.

High-voltage Outputs
The 64 output devices are open-drain MOSFETs designed to drive small capacitive loads (tens of pF) at very high speed. The unique process technology used to make these high-voltage devices provides a fully-enhanced output with only 5 V applied to the gate of the MOSFET. This eliminates the need for an intermediate level-translation supply voltage of 15 V, as is often used with competitive devices.

Each output has a speed control circuit that limits the rise and fall times to approximately 10 µs. This is done to minimize noise coupling and "crosstalk" between channels.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} Voltage	6 V
OUT Voltage	-0.3 V to 400 V
Input Voltage	- 0.3 V to V_S + 0.3 V
COM Current[2]	500 mA
Storage Temperature	–65 to 125°C
Ambient Temperature	0 to 70°C
Junction Temperature	150°C
Lead Temperature[3]	260°C
Power Dissipation (T_A = 25°C)	1.5 W
(T_A = 70°C)	1 W
Thermal Impedance (θ_{JA})	83°C/W

1. Unless noted, all voltages referenced to COM.
2. All COM pins connected together.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{CC} = 5 V, COM = 0 V, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
LOGIC						
Input Current, High or Low	I_{IH}, I_{IL}	V_{IN} = V_{CC} or COM			10	µA
Input Voltage High	V_{IH}		3.0			V
Input Voltage Low	V_{IL}				2.0	V
DATA OUT						
Output Voltage High	V_{OH}	I_{OUT} = -100 µA	4	4.5		V
Output Voltage Low	V_{OL}	I_{OUT} = 100 µA		0.5	1	V
HV OUTPUT						
ON-State Output Voltage	$V_{OUT(ON)}$	I_{OUT} = 1 mA		1	10	V
OFF-State Output Current	$I_{OUT(OFF)}$	V_{OUT} = 375 V, T_A = 25°C		10	100	nA
Clamp Voltage	$V_{OUT(C)}$	I_{OUT} = -1 mA			-3	V
Output Capacitance	C_{OSS}	V_{OUT} = 100 V		3		pF

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{CC} = 5 V, COM = 0 V, T_A = 0 to 70°C	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
DYNAMIC						
Clock Frequency	f_{CLOCK}				6	MHz
Clock Pulse Width High or Low	t_W	See Figure 4	83			ns
Data Setup Time Before ↓ Clock	t_{SU}	See Figure 4	35			ns
Data Hold Time After ↓ Clock	t_H	See Figure 4	15			ns
Latch Enable Pulse Width	t_{WLE}	See Figure 4	83			ns
Latch Enable Delay Time	t_{DLE}	See Figure 4	50			ns
Latch Enable Setup Time	t_{SLE}	See Figure 4	25			ns
Clock Delay Time DATA OUT H→L	t_{DHL}	See Figure 4			135	ns
Clock Delay Time DATA OUT L→H	t_{DLH}	See Figure 4			135	ns
Output Delay Time from LE	$t_{DOUT(LE)}$	See Figure 4		2.2	5	µs
Output Delay Time from OE	$t_{DOUT(OE)}$	See Figure 4		150	500	ns
Output Fall Time	t_f	R_L = 10 MΩ, V_{PP} = 375 V, C_L = 10 pF, See Figure 4		10	25	µs
SUPPLY						
Supply Voltage	V_{CC}		4.5		5.5	V
Supply Current	I_{CC}	f_{CLOCK} = 6 MHz, f_{DATA} = 3 MHz		3	5	mA
		f_{CLOCK} = 0, Shift Register Clear (All 0)		70	300	µA

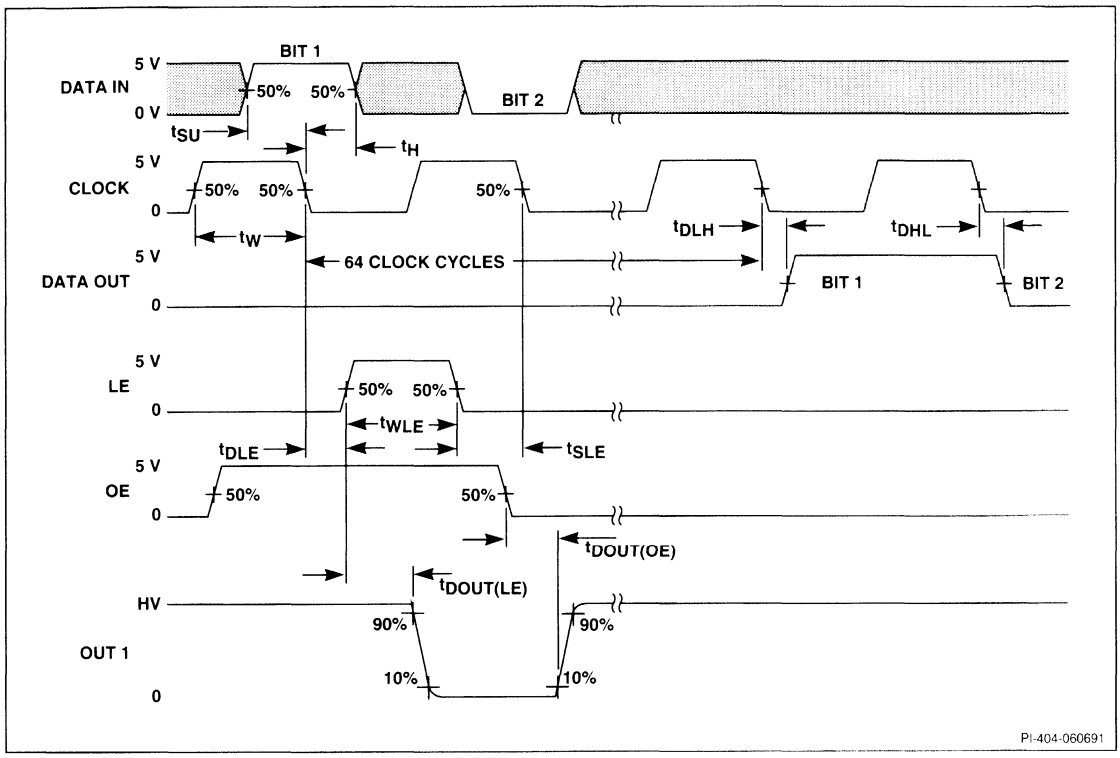
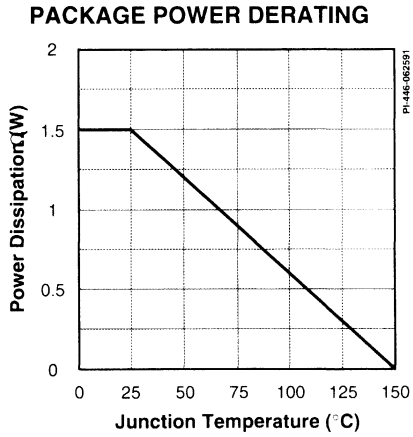


Figure 4. Timing Diagram.



Evaluation Boards 3

INDEX

PWR-EVAL1

PWR-SMP3 Evaluation Board

110 VAC Input
Isolated 5 V, 5 W Output

POWER INTEGRATIONS, INC.

Product Highlights

Isolated 5 V Output from 110 VAC Input
- Up to 5 watts of output power can be supplied
- Isolation is provided by transformer designed to UL specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits
- Input overvoltage shutdown
- Input undervoltage lockout
- Integrated current limit
- Thermal Shutdown

Designed to Meet Regulatory Standards
- UL Recognized component - File #E131417
- Designed to meet FCC Class A

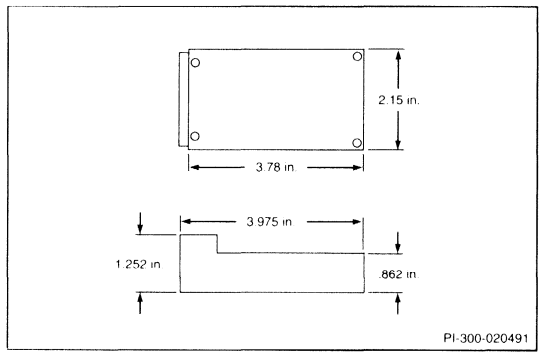


Figure 1. Evaluation Board Overall Physical Dimensions.

Description

The PWR-EVAL1 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP3BNC power supply IC.

The PWR-SMP3, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a switchmode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP3 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP3 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL1 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

PARAMETER	LIMITS
Input Voltage Range	85 to 130 VAC
Input Frequency Range	47 to 440 Hz
Output Voltage Range	4.5 to 5.5 VDC
Load Current Range	.06 to 1 A
Temperature Range	0 to 70°C
Efficiency	> 70%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	OPERATING VOLTAGE
PWR-EVAL1	110 VAC INPUT 5 VDC OUTPUT @ 5 W

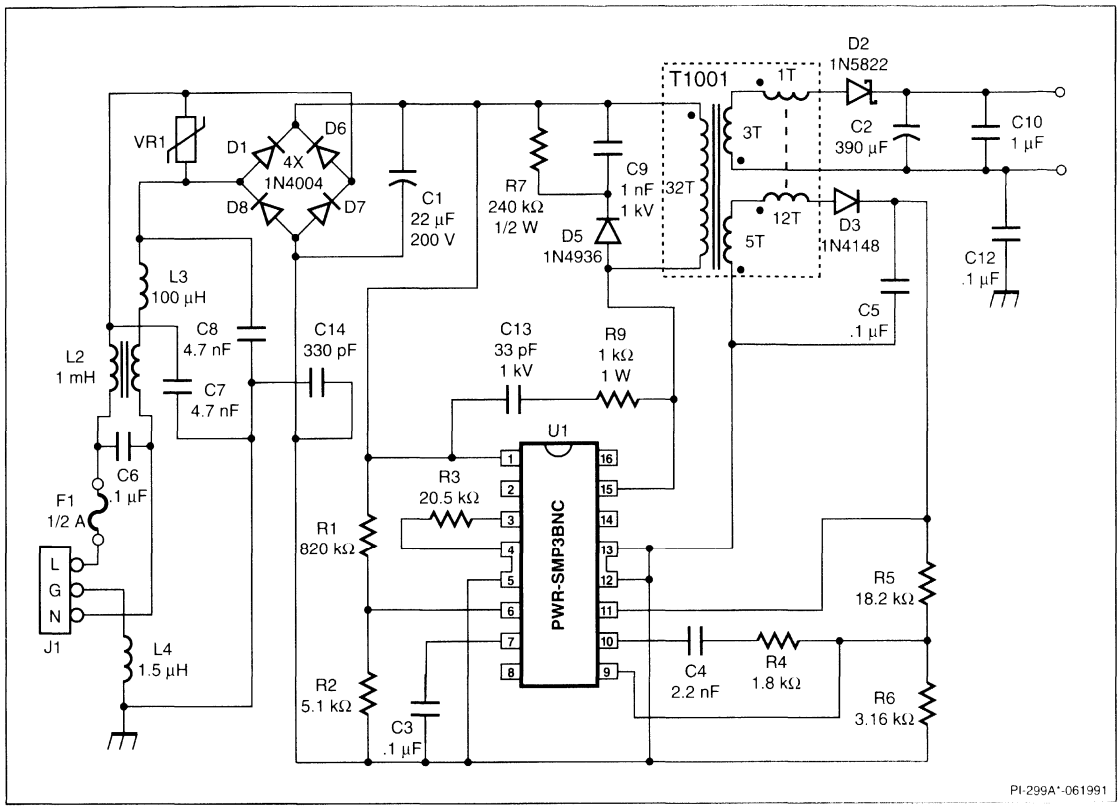


Figure 3. Schematic Diagram of the PWR-EVAL1 Power Supply.

General Circuit Description

The PWR-EVAL1 is an isolated Buck-Boost or flyback switching power supply topology[1]. The power supply is implemented using the PWR-SMP3BNC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1001 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 140 VAC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding of T1001. The PWR-SMP3 has been designed for a bias voltage (pin 11), of 8.5 volts. The effective transformer volts-per-turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. The three main elements that affect the regulation of the output voltage are; maintenance of a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

The circuit groups in the schematic Figure 3 are as follows. L2, L3, L4, C6, C7, C8, C12, and C14 form the EMI filter. D1, D6, D7, D8, and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. The voltage divider formed by R1 and R2 set the input voltage that activates the input undervoltage and overvoltage shutdown functions. D5, C9 and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C13 and R9 damp the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP3. C3 and C5 are bypass capacitors.

Forward compatibility with higher power PWR-SMP products can be achieved by connecting pin 15 and 16 together on the printed circuit board.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	22 µF, 200 V	UVX2D220MPA	Nichicon (America)
C2	390 µF, 35 V	UPL1V391MPH	Nichicon (America)
C3, C5, C12	100 nF, 50 V	K104Z20Z5UFVBWN	Mepco/Centralab
C6	100 nF-S, 250 VAC	QXW2E104KTPT	Nichicon (America)
C4	2.2 nF, 50 V	K222M15X7RFVAWA	Mepco/Centralab
C14	330 pF-S, 250 VAC	440LT33	Cera-Mite(Sprague)
C7, C8	4.7 nF-S, 250 VAC	440LD47	Cera-Mite(Sprague)
C9	1 nF, 1 kV	D102P29Z5UNAAEM	Mepco/Centralab
C10	1 µF, 25 V	TCD21E1E105M	Marcon
C13	33 pF, 1 kV	5GAQ33	Sprague Electric
D1, D6-D8		1N4005	Motorola
D2		1N5822	Motorola
D3		1N4148	Motorola
D5		1N4936	Motorola
F1	1/2 A, 125 VAC	252.500	Littlefuse/Tracor
L2	1 mH	SC-01 10G	Tokin
L3	100 µH	90-37	Coilcraft
L4	1.5 µH	2673200201	Fair-Rite Products
R1	820 kΩ, 1/4 W, 5%	5043CX820K0J	Mepco/Centralab
R2	5.1 kΩ, 1/4 W, 5%	5043CX5K100J	Mepco/Centralab
R3	20.5 kΩ, 1/4 W, 1%	5043ED20K50F	Mepco/Centralab
R4	1.8 kΩ, 1/4 W, 5%	5043CXK1K80J	Mepco/Centralab
R5	18.2 kΩ, 1/4 W, 1%	5043ED18K20F	Mepco/Centralab
R6	3.16 kΩ, 1/4 W, 1%	5043ED3K160F	Mepco/Centralab
R7	240 kΩ, 1/2 W, 5%	5053CX240KJ	Mepco/Centralab
R9	1 kΩ, 1 W, 5%	5073YL1K00J	Mepco/Centralab
U1		PWR-SMP3BNC	Power Integrations, Inc.
VR1	130 VAC	V130LA1	Harris
T1	5 V Output	T1001	Custom *
J1	Plug Socket	C6480	USD Products/Cooper
	P C Board	SMP100-1-PCB	Custom **
	Shield (Optional)	SMP100-1-BOX	Custom ***

Custom Components:

* Qualified manufacturers are:

Datatronics	(714) 928-7731	FAX: (714) 928-7701
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin Magnetics	(415) 490-7500	FAX: (415) 490-7502

** Manufacturer is:

Martex Circuits, Inc.
885 Maude Ave.
Mountain View, Ca. 94043
(415)965-3005

*** Drawing is available from Power Integrations, Inc.

Figure 4. Parts List for the PWR-EVAL1

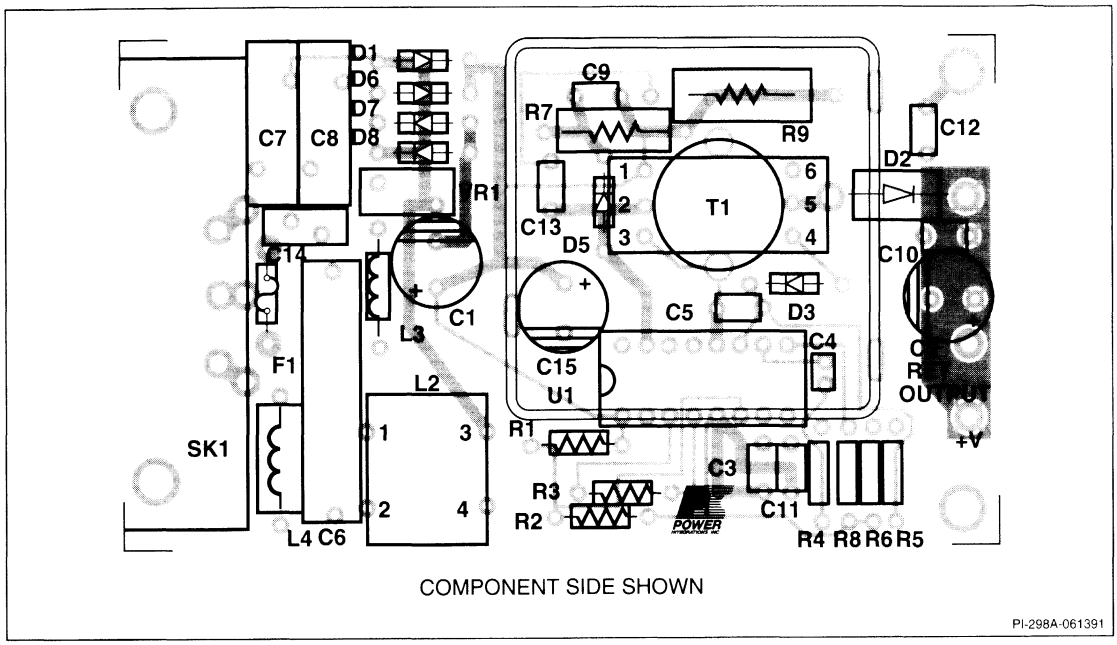


Figure 5. Component Legend of the PWR-EVAL1.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 was measured by applying a DC input voltage to the PWR-EVAL1.

Load Regulation (Figure 6) - The amount of output voltage change for a change in output current is referred to as load regulation. The output changes 5% for a 10% to 100% load current range. Below 10% of rated load the output voltage rises due to the leakage inductance of the transformer[2]. Non-ideal load regulation is caused by the resistance of the transformer output winding, the output rectifier series resistance, and the imperfect coupling between the output winding and the voltage feedback winding. The toroid pulse transformer improves the load regulation by minimizing the effect of the leakage inductance voltage spike on the feedback winding voltage.

The circuit in Figure 3 uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation of ± 5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on the features and trade-offs of feedback winding regulation and optical feedback regulation.

Line Regulation (Figure 7) - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage is 0.5% for a input voltage change of 50 V(rms) or 100 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first cut transformer design procedure. Efficiency at full load and nominal line voltage is 65%.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typical output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[3].

$$PF = \frac{P_{in}}{V_{in} \times I_{in}}$$

The power factor of the PWR-EVAL1 with a 5 W load is approximately 0.6.

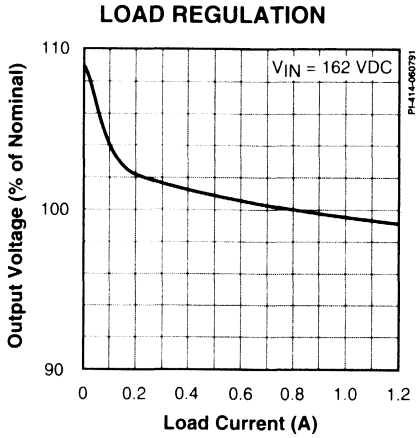


Figure 6.

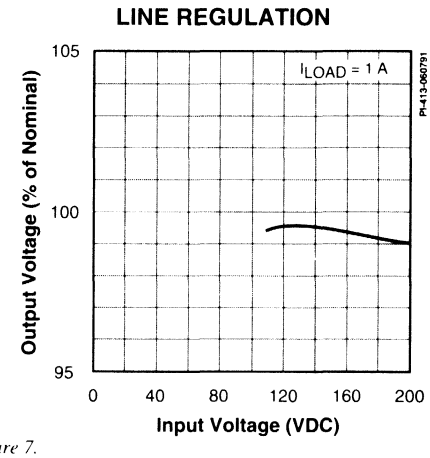


Figure 7.

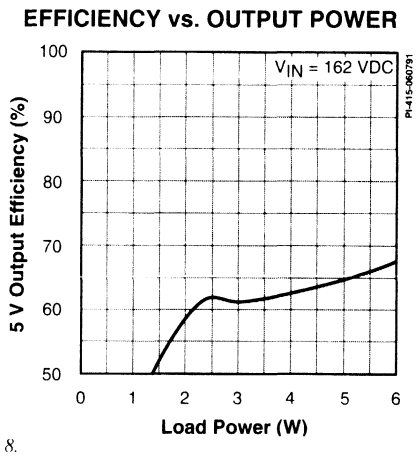


Figure 8.

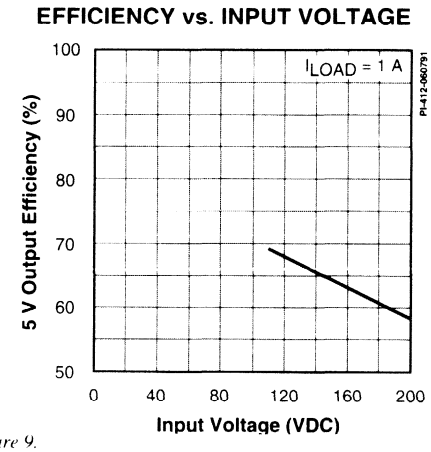


Figure 9.

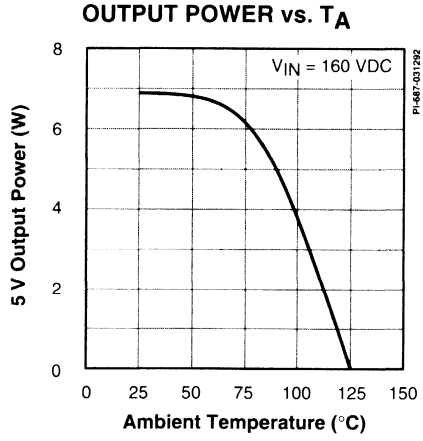


Figure 10.

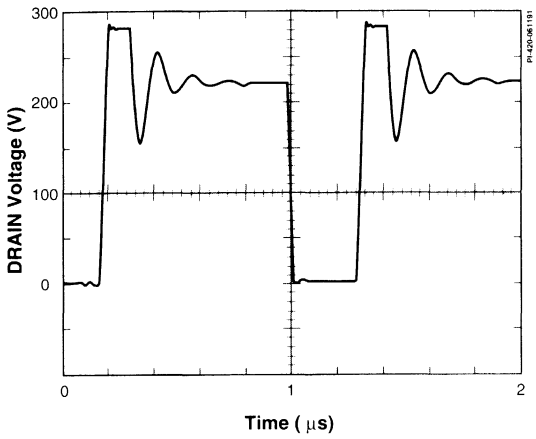


Figure 11. Drain-source Voltage of the PWR-SMP3.

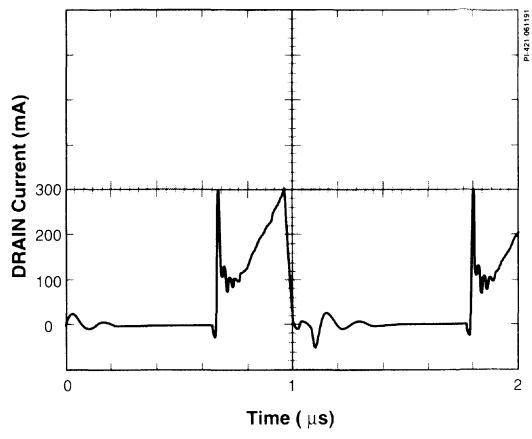


Figure 12. Drain Current of the PWR-SMP3.

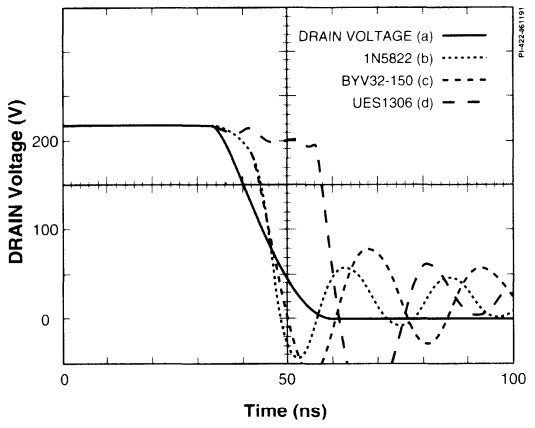


Figure 13. Recovery Times of Output Rectifier Diodes.

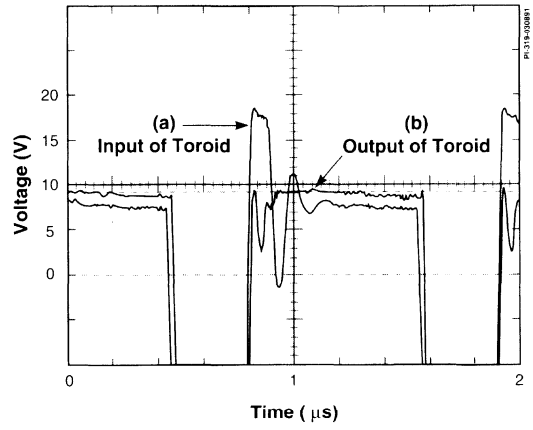


Figure 14. Pulse Transformer Winding Voltages.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a 1N5822 Schottky diode. Figure 13(c) is the anode of D2 when D2 is a BYV32-150 (150 V, 20 A, 35 ns) diode. Figure 13(d) is the anode of D2 when D2 is a UES1306 (400 V, 5 A, 50 ns) diode. The 1N5822 and BYV32-150 exhibit approximately 6 ns recovery times in the circuit, providing good functionality. However, the UES1306 exhibits a 22 ns recovery time in the circuit. This length of recovery time does not work well in the circuit.

The feedback bias supply winding voltage on each side of the pulse transformer winding is shown in Figures 14(a) and (b). This waveform is very important when load voltage regulation is being investigated. Waveform 14(a) is the voltage on the

power transformer side of the pulse transformer. Waveform 14(b) is the voltage on the rectifier side of the pulse transformer. Notice how the pulse transformer has cancelled the leakage inductance spike voltage present on the feedback winding of the power transformer.

Power Supply Turn On Sequence

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the feedback winding and filter provides bias current and turns off the pre-regulator when the power supply is operating. The bias supply voltage at turn-on is shown in Figure 15. It is important to notice how closely the output voltage is coupled to the feedback bias supply. The amount of voltage overshoot is a function of the control loop compensation. If the control loop is made slower by modifying R4 and C4, the overshoot will increase.

The 5.6 volt V_S voltage on pin 7 is derived from pin 11 with a linear regulator. An external bypass capacitor on the V_S pin provides a path for the gate drive switching noise currents to flow.

Output Voltage

The output voltage is controlled by the transformer turns ratio. The PWR-SMP3BNC control circuit will regulate the rectified V_{BIAS} feedback voltage (pin 11) to a typical value of 8.45 V. The output voltage can be estimated by multiplying the output-to-feedback turns ratio by the feedback voltage. A precise method of determining the output voltage would take into account the specific rectifier voltage drop, the resistance of the output winding of the transformer, and the equivalent series resistance of the output capacitor.

The output voltage can be adjusted using the transformer turns ratio. The output voltage can be coarsely tuned by increasing the number of junction voltage drops for D3 and fine tuned with the voltage divider R5 and R6. The R5-R6 voltage divider ratio can be adjusted with a voltage trim resistor (R8).

A higher precision of output voltage regulation can be achieved by sensing and regulating the output voltage directly. This can be accomplished by the use of a secondary side referenced error amplifier and optical coupler circuit as described in AN-8.

Note that V_{BIAS} (pin 11) must be between 8.25 V and 9 V to cut off the high-voltage pre-regulator within U1. Additional information on transformer design is available in AN-7.

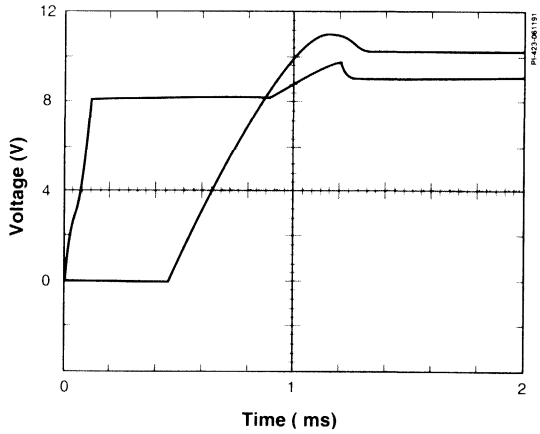


Figure 15. Bias Regulator-Feedback Supply Relationship.

Output Transformer T1001

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies. The T1001 has passed the review of Underwriters Laboratories for use in 110 VAC applications.

The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Toroid Pulse Transformer

The pulse transformer is part of the standard transformer T1001. The transformer generates a voltage pulse on its primary from the rate of change of current in the output rectifier[4]. This voltage pulse is scaled and placed in series with the feedback winding.

The voltage on the output of the pulse transformer is equal, in phase and proportional to the leakage inductance voltage spike. The peak output voltage of the series connection of the feedback winding and the pulse transformer secondary is proportional to the output voltage and is not influenced by the leakage inductance voltage spike. The cancellation effect of the pulse transformer can be seen in Figure 14.

Output Transformer T1001 (cont.)

Magnetics Design

The standard transformer has a primary winding with 32 turns of 36 AWG magnet wire, a feedback winding of 5 turns of 36 AWG magnet wire and an output winding of 3 turns of 300 V rated insulated 24 AWG wire. The insulation on the secondary wire meets the voltage breakdown and safety requirements of Underwriters Laboratories.

The pulse transformer has a one turn primary and 12 turns of 36 AWG magnet wire as a secondary.

The nominal primary inductance is 175 µH. The maximum leakage inductance measured on the primary is 13 µH. Approximately 80% of the leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 5 MHz.

The resistance of the primary winding is 1.2 Ω. The resistance of the secondary winding is 0.01 Ω. The resistance of the feedback winding is 0.084 Ω.

The core is a 14 mm x 8 mm pot core. The core material is Siemens M33. This material is a high frequency low loss Ni-Zn ferrite. The A_l value is 171 nH/T^2. The pulse transformer core is Philips 1041T060-4C4.

The power transformer peak flux density at 3 watts is 560 gauss. The peak flux density at 5 watts is 696 gauss. The AC flux density at 5 watts is 565 gauss.

The primary saturation current at 100°C, 2500 gauss, is 1.14 amperes.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.35}{2 \times 8 \times 10^5 \times (0.35 - 0.238)} = 186\mu H$$

where the peak switch current is between the typical current with V_{DS} of 10 V and the minimum current limit current. The primary inductance calculations for the PWR-SMP3 with 5 watts output show an inductance of 186 µH. The efficiency of the PWR-SMP3 at 5 watts and 100 VDC is 60%. The input power will be 8.33 W (5 W divided by 0.6). The average input current at 100 VDC will be 0.0833 A (8.33 W divided by 100 V). The average on time current with a 35% duty cycle is 0.238 A (.0833 A divided by 0.35). The primary inductance L_p equals 186 µH. The nominal primary inductance of the T1001 is 175 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds / turn = 0).

$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.35}{(1 - 0.35)} \times \frac{115 - 5}{5 + 0.5} = 10.77$$

Single Output Voltage

The standard transformer design can be modified for voltages other than 5 volts. This is achieved by changing the secondary winding to feedback winding turns ratio. The output voltage can be fine tuned by adjusting the R5, R6 voltage divider. However, the voltage on pin 11 of the PWR-SMP3BNC must be within the voltage range specified in the data sheet.

If the turns count on the secondary is greater than three, a larger core will be required to accommodate the larger number of insulated turns on the bobbin. Multiple output voltages are also possible (refer to AN-7).

Output Transformer T1001 (cont.)

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C13 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C13 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package, the ambient temperature[15], and the peak switching transistor current limit circuit. The available output power as a function of input voltage for an 80°C temperature rise (junction to ambient) is shown in Figure 16.

Thermal Characteristics

The PWR-SMP3BNC is packaged in a 16-pin plastic power DIP package[16]. This package offers a lower thermal impedance as compared to a standard plastic DIP package. The thermal impedance from junction to ambient and from junction to case are 43°C/Watt and 6°C/Watt respectively. Soldered connections to the heat spreading "wings" (pins 4, 5, 12, and 13) provide a good thermal path while the DIP form factor maintains compatibility with automatic insertion equipment for low cost assembly. The thermal impedance from case to local ambient on a typical power supply board is 43-6 = 37°C/W. The local ambient temperature can be 10°C above ambient due to heating from other components on the printed circuit board.

The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and the transformer and damping network capacitances[17], and the losses in the pre-regulator when it is active. Figure 17 is the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 18. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this figure to determine the total AC losses in the circuit.

Additional information on thermal management is available in AN-9.

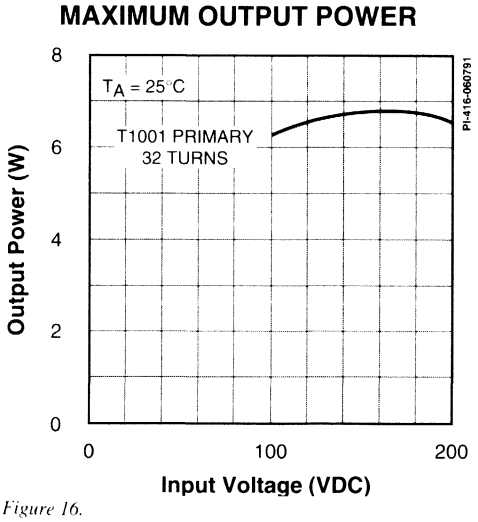


Figure 16.

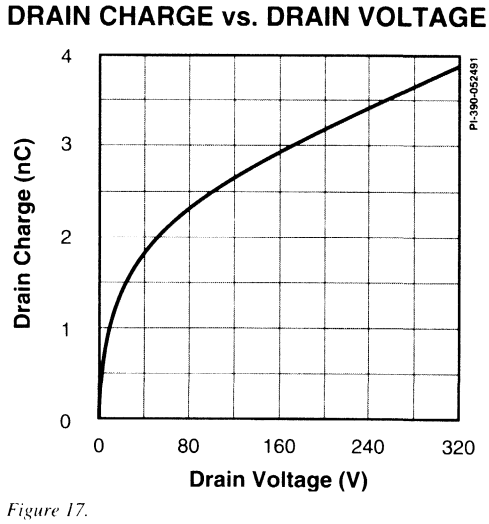


Figure 17.

3

Current Limit

The current limit circuit is internal to the PWR-SMP3BNC and is a peak detection type of circuit. The circuit monitors the current flowing in the switching transistor. When the current exceeds the typical value of 425 mA for 100 ns the switching transistor is turned off for the rest of the oscillator cycle. The effect on the output voltage can be seen in Figure 19. The shape of the current limit function is very close to a constant power curve[8]. This is because the circuit regulates the peak current in the transformer primary providing a constant energy delivery to the core during current limit, thus a constant power output in current limit.

Current limit is implemented within the integrated circuit by applying a current sense signal to a comparator input. The comparator triggers a latch which turns the power transistor off until the next clock cycle.

Operating Frequency

The operating frequency of the PWR-EVAL1 is typically 900 kHz. The frequency of operation is not adjustable. The timing capacitor for the oscillator is internal to the PWR-SMP3BNC. Other members of the PWR-SMP family have programmable operating frequency. The printed circuit board has a location for this frequency setting capacitor C11 connected to pin 8 of U1.

Voltage Control Loop

The PWR-SMP3BNC has a voltage-mode control circuit[9]. The DC input to output voltage transfer function when operating in the continuous current mode is:

$$\frac{V_O}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[10]. The duty cycle is controlled by the output voltage error amplifier. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[11,12] is included in the documentation disk. T1, U1, R4, R5, C2 and C4 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The model for the operating point duty cycle transformation uses a transconductance generator and a voltage gain stage. The coefficients of the small signal pulse width modulator transfer-function generators are calculated by knowing the primary reflex voltage (output voltage plus rectifier forward drop times the transformer turns ratio), the duty cycle of the operating point of interest and the load resistance transformed to the primary of the transformer:

$$R = R_O \times \left(\frac{N_P}{N_S}\right)^2 = 5 \times \left(\frac{32}{3}\right)^2 = 569\Omega$$

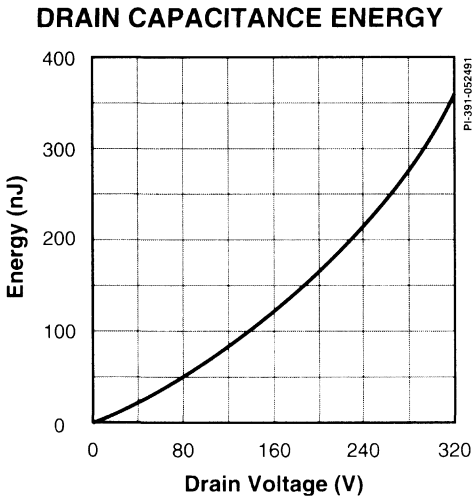


Figure 18.

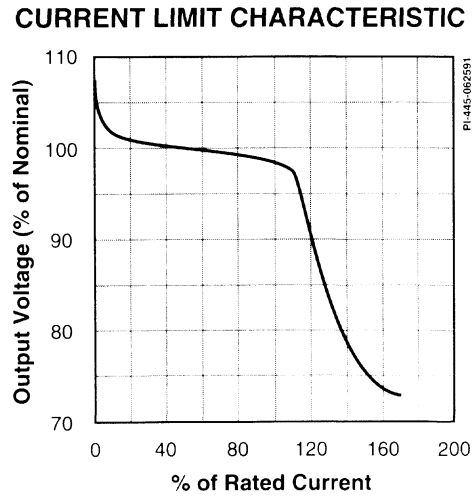


Figure 19.

The voltage generator gain:

$$E = \frac{-V}{D^2} = \frac{-59}{(0.269)^2} = -813$$

The current generator gain:

$$J = \frac{-V}{(1-D)^2 \times R} = \frac{-59}{(1-0.269)^2 \times 569} = -0.19426$$

The current generator is to provide the negative input impedance effect of a switching regulator and can be neglected if the resonant frequency of the EMI filter is much higher than the control loop frequencies of interest.

The measured power supply open loop gain/phase response curve is shown in Figure 20. The control loop has 85 degrees phase margin, an open loop unity gain crossover frequency of 29 kHz and 11.6 dB gain margin at 178 kHz with a 5 watt load. This provides 45 dB of gain at 120 Hz for power line ripple rejection.

The output ripple voltage at the power line frequency can be estimated by knowing the open loop gain of the regulator, the transformer turns ratio and the operating duty cycle of the flyback switching regulator. The output peak to peak ripple voltage at the power line frequency can be calculated from the following equation:

$$V_{o(pp)} = \frac{V_{in(pp)} \times \frac{N_S}{N_P} \times \frac{D}{1-D}}{A_V} = \frac{20 \times \frac{3}{32} \times \frac{0.27}{1-0.27}}{178} = 3.9\text{mV}$$

The DC model for the error amplifier within the integrated circuit is shown in Figure 21. Figure 22, the error amplifier open-loop gain/phase response curve, shows that the amplifier is stable in the unity gain feedback configuration.

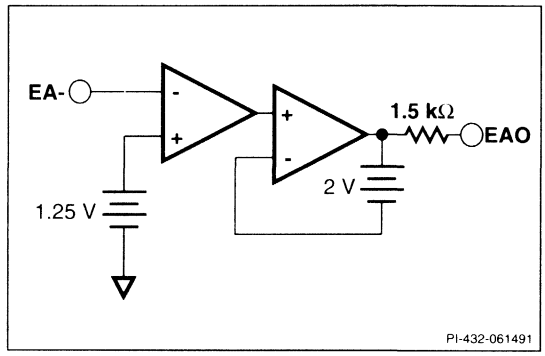


Figure 21. Error Amplifier Equivalent Circuit.

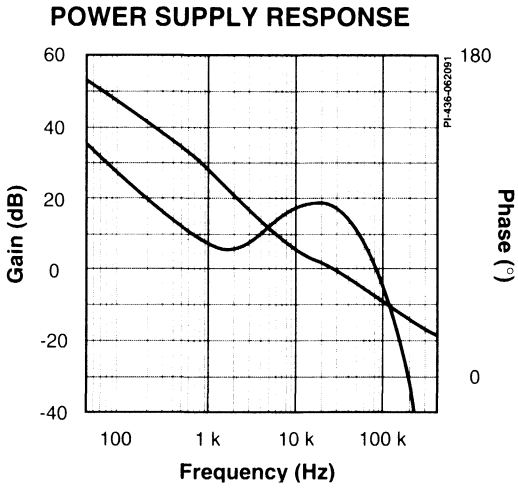


Figure 20.

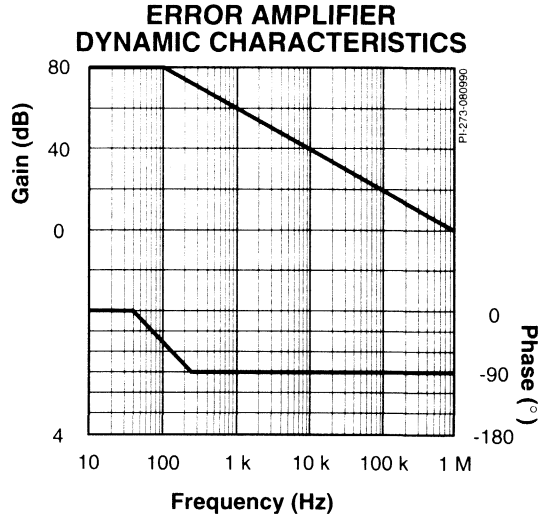


Figure 22.

Protection Features

Overtemperature
The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 135°C and keeps it off until the junction temperature decreases 45°C[13].

Input Overvoltage Protection
The voltage divider R1 and R2 sets the point where the input overvoltage comparator will inhibit the power supply output. The switching power transistor will be turned off when pin 6 exceeds 1.25 V. For the PWR-EVAL1, this translates to an input voltage of:

$$1.25 \times \frac{825.1}{5.1} = 202\text{V}$$

The switching power transistor will be turned back on when pin 6 drops below 1.2 V. For the PWR-EVAL1, this translates to an input voltage of:

$$1.2 \times \frac{825.1}{5.1} = 194\text{V}$$

Input Undervoltage Protection
The switching power transistor will be turned off when pin 6 drops below 0.34 volts. This translates to:

$$0.34 \times \frac{825.1}{5.1} = 55\text{V}$$

The switching power transistor will be turned back on when pin 6 exceeds 0.39 volts. This translates to:

$$0.39 \times \frac{825.1}{5.1} = 63\text{V}$$

Test Mode

The OV/UV control (pin 6) controls the built in test logic of the integrated circuit. The built-in test logic turns on the power transistor continuously when the voltage on pin 6 is equal to the pin 7 voltage (5.6 volts) +/- 1.5 V Do not put the circuit in test mode while operating in a power supply circuit as this could destroy the PWR-SMP3.

Control Circuit Undervoltage Protection
The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is typically 5 volts on pin 7.

Input Filtering and Rectification
D1, D6, D7, D8 and C1 perform the input rectification and filtering function. The rectifier diodes should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage rating on C1 is equal to the peak value of the maximum rectified input voltage, 200 V for 115 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitor, C1, can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage the power supply will provide a regulated output voltage at maximum power, and the minimum AC input voltage[14]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 when the input bridge diodes stop conducting, and V_2 is the voltage on C1 when the input bridge diodes start conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the input capacitor value.

Input Surge Current

When line voltage is applied to the power supply a surge of current flows in the input of the power supply to charge the input storage capacitor C1[15]. The magnitude of current must be within the surge ratings of the power switch, fuse and input rectifiers. The surge current is limited by the resistance of the EMI filter. L3, the differential mode filter inductor contributes the majority of the EMI filter resistance of 8 Ω. This limits the peak surge current to 160 V/8 Ω = 20 A.

EMI Considerations

This power supply was designed to meet worldwide EMI (FCC, part 15, subpart J) and safety (UL1950 and IEC950) specifications. Figure 23 is a plot of the conducted EMI relative to the FCC specification limits.

Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L3 and C6 filter differential mode conducted emissions.

Common Mode Filter
L2, L4, C7, C8, C12, and C14 filter common mode conducted emission currents[16]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C12 couples high-frequency noise back to the system chassis ground. C7, C8, and C14 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP3. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L4 in series with the ground lead of the power connector is a "lossy" bead and is equivalent to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

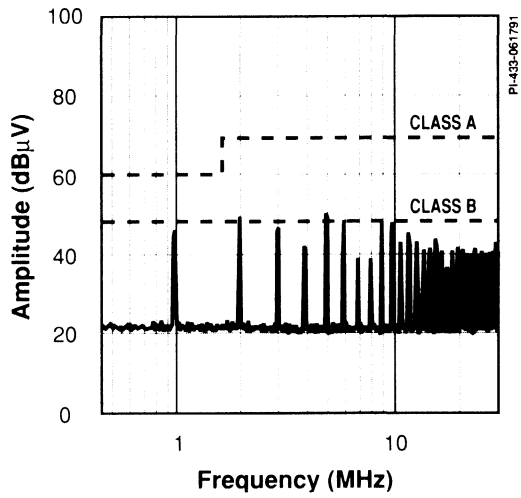


Figure 23. EMI Plot of the PWR-EVAL1.

Safety Agency Requirements

The PWR-EVAL1 has been evaluated to the UL1950 specification by Underwriters Laboratories. The PWR-EVAL1 is an Underwriters Laboratories recognized component. The UL file number is E131417. The evaluation project (90SC03754) was completed October 8, 1990. The file is available to customers of Power Integrations.

Additional information on safety and layout-related issues is available in DA-2.

Documentation Disks

The PWR-EVAL1 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL1 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README1.BAT	(This file) contains a summary and last minute information on PWR-EVAL1
PWB1001B.APR	Aperture file with assigned D-codes
EVAL1.BOM	Bill of Materials file
EVAL1ASY.DWG	Assembly drawing file
FAB1001B.DWG	Fabrication drawing for the PC board
SHLD12.DWG	Fabrication drawing for the optional shield over the power supply
1001B.G23	Single laser plot file for all layers of the PCB
EVAL1.LIB	Library file of the part symbols used in both schematics
EVAL1.SCH	Schematic file of PWR-EVAL1
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES1.TXT	Functional description of the power supply circuitry used in PWR-EVAL1
ICDESC1.TXT	Functional description of the PWR-SMP3 integrated circuit used in PWR-EVAL1
EVL1COST.TXT	Estimated parts cost
T1001 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD 286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README1.BAT and the EVAL1.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations on request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP3.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

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14 Tartar, Ralph E., Principles of Solid-state Power Conversion Howard W. Sams & Co., Inc., 1985, p. 232

15 Hirshberg, Walter "Optimizing Line Inrush Design in Off-Line Converters" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, E3.1-E3.7

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PWR-EVAL2

PWR-SMP110 Evaluation Board

110 VAC Input
Isolated 5 V, 10 W Output

Product Highlights

Isolated 5 V Output from 110 VAC Input
- Up to 10 watts of output power can be supplied
- Isolation is provided by transformer designed to UL specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits
- Input overvoltage shutdown
- Input undervoltage lockout
- Thermal Shutdown

Designed to Meet Regulatory Standards
- Layout designed to meet UL/CSA requirements
- Designed to meet FCC Class A

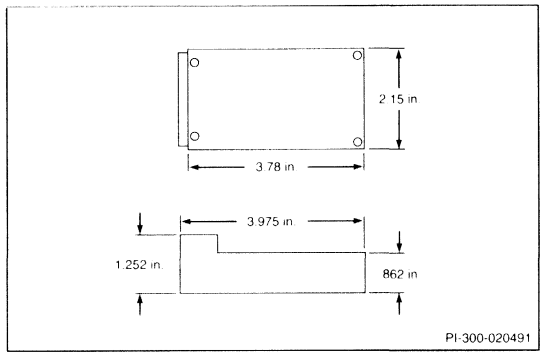

Figure 1. Evaluation Board Overall Physical Dimensions.

Description

The PWR-EVAL2 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP110BNC power supply IC.

The PWR-SMP110, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a switchmode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP110 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP110 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL2 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

PARAMETER	LIMITS
Input Voltage Range	85 to 130 VAC
Input Frequency Range	47 to 440 Hz
Output Voltage Range	4.5 to 5.5 VDC
Load Current Range	0.06 to 2 A
Temperature Range	0 to 70°C
Efficiency	> 65%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	OPERATING VOLTAGE
PWR-EVAL2	110 VAC INPUT 5 VDC OUTPUT @ 10 W

3

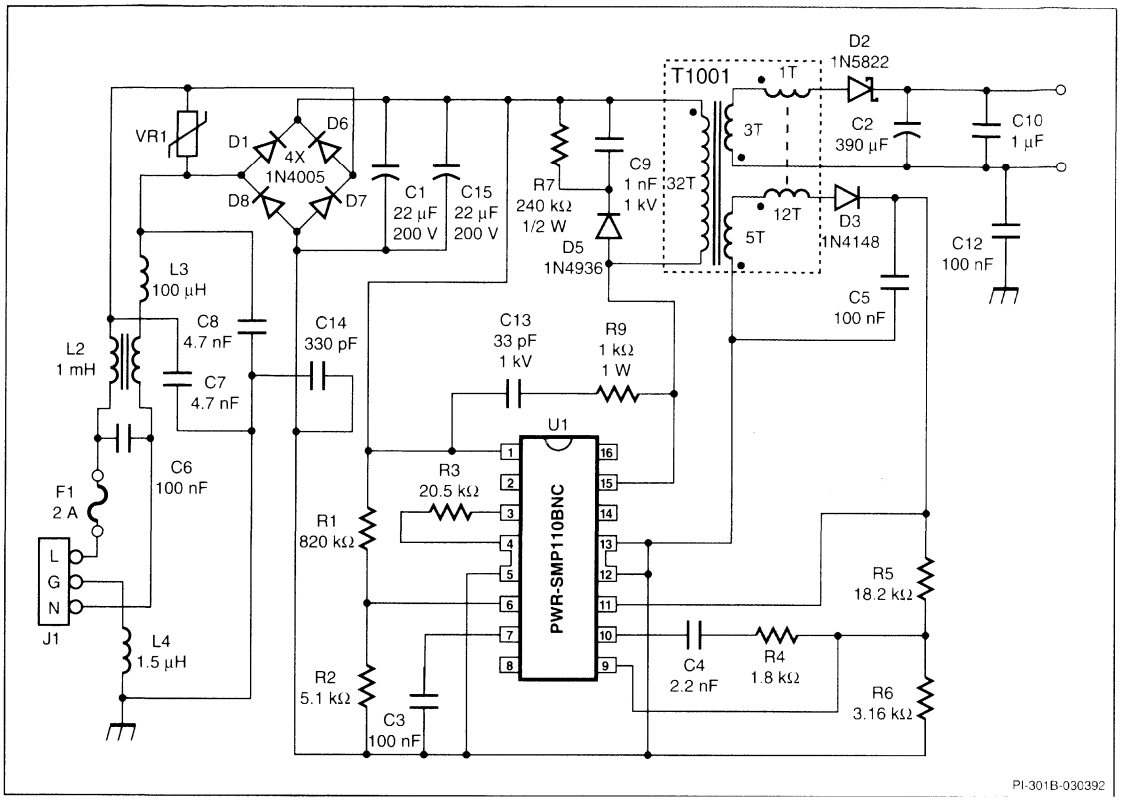

Figure 3. Schematic Diagram of the PWR-EVAL2 Power Supply.

General Circuit Description

The PWR-EVAL2 is an isolated Buck-Boost or flyback switching power supply topology[1]. The power supply is implemented using the PWR-SMP110BNC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1001 standard transformer (see DA-3), will produce a 5 volt, 10 watt power supply that will operate from 85 to 140 VAC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding of T1001. The PWR-SMP110 has been designed for a bias voltage (pin 11), of 8.5 volts. The effective transformer volts-per-turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. The three main elements that affect the regulation of the output voltage are: maintenance of a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

The circuit groups in the schematic Figure 3 are as follows. L2, L3, L4, C6, C7, C8, C12, and C14 form the EMI filter. D1, D6, D7, D8, and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. The voltage divider formed by R1 and R2 set the input voltage that activates the input undervoltage and overvoltage shutdown functions. D5, C9 and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C13 and R9 damp the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP110. C3 and C5 are bypass capacitors.

Forward compatibility with higher power PWR-SMP products can be achieved by connecting pin 15 and 16 together on the printed circuit board.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1, C15	22 µF, 200 V	UVX2D220MPA	Nichicon (America)
C2	390 µF, 35 V	UPL1V391MPH	Nichicon (America)
C3, C5, C12	100 nF, 50 V	K104Z20Z5UFVBWN	Mepco/Centralab
C6	100 nF-S, 250 VAC	QXW2E104KTPT	Nichicon (America)
C4	2.2 nF, 50 V	K222M15X7RFVAWA	Mepco/Centralab
C14	330 pF-S, 250 VAC	440LT33	Cera-Mite(Sprague)
C7, C8	4.7 nF-S, 250 VAC	440LD47	Cera-Mite(Sprague)
C9	1 nF, 1 kV	D102P29Z5UNAAEM	Mepco/Centralab
C10	1 µF, 25 V	TCD21E1E105M	Marcon
C13	33 pF, 1 kV	5GAQ33	Sprague Electric
D1, D6-D8		1N4005	Motorola
D2		1N5822	Motorola
D3		1N4148	Motorola
D5		1N4936	Motorola
F1	2 A, 125 VAC	252.002	Littlefuse/Tracor
L2	1 mH	SC-01-10G	Tokin
L3	100 µH	90-37	Coilcraft
L4	1.5 µH	2673200201	Fair-Rite Products
R1	820 kΩ, 1/4 W, 5%	5043CX820K0J	Mepco/Centralab
R2	5.1 kΩ, 1/4 W, 5%	5043CX5K100J	Mepco/Centralab
R3	20.5 kΩ, 1/4 W, 1%	5043ED20K50F	Mepco/Centralab
R4	1.8 kΩ, 1/4 W, 5%	5043CXK1K80J	Mepco/Centralab
R5	18.2 kΩ, 1/4 W, 1%	5043ED18K20F	Mepco/Centralab
R6	3.16 kΩ, 1/4 W, 1%	5043ED3K160F	Mepco/Centralab
R7	240 kΩ, 1/2 W, 5%	5053CX240KJ	Mepco/Centralab
R9	1 kΩ, 1 W, 5%	5073YL1K00J	Mepco/Centralab
U1		PWR-SMP110BNC	Power Integrations, Inc.
VR1	130 VAC	V130LA1	Harris
T1	5 V Output	T1001	Custom *
J1	Plug Socket	C6480	USD Products/Cooper
	P C Board	SMP100-1-PCB	Custom **
	Shield (Optional)	SMP100-1-BOX	Custom ***

Custom Components:

* Qualified manufacturers are:

Datatronics	(714) 928-7731	FAX: (714) 928-7701
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin Magnetics	(415) 490-7500	FAX: (415) 490-7502

** Manufacturer is:
Martex Circuits, Inc.
885 Maude Ave.
Mountain View, Ca. 94043
(415)965-3005

*** Drawing is available from Power Integrations, Inc.

Figure 4. Parts List for the PWR-EVAL2

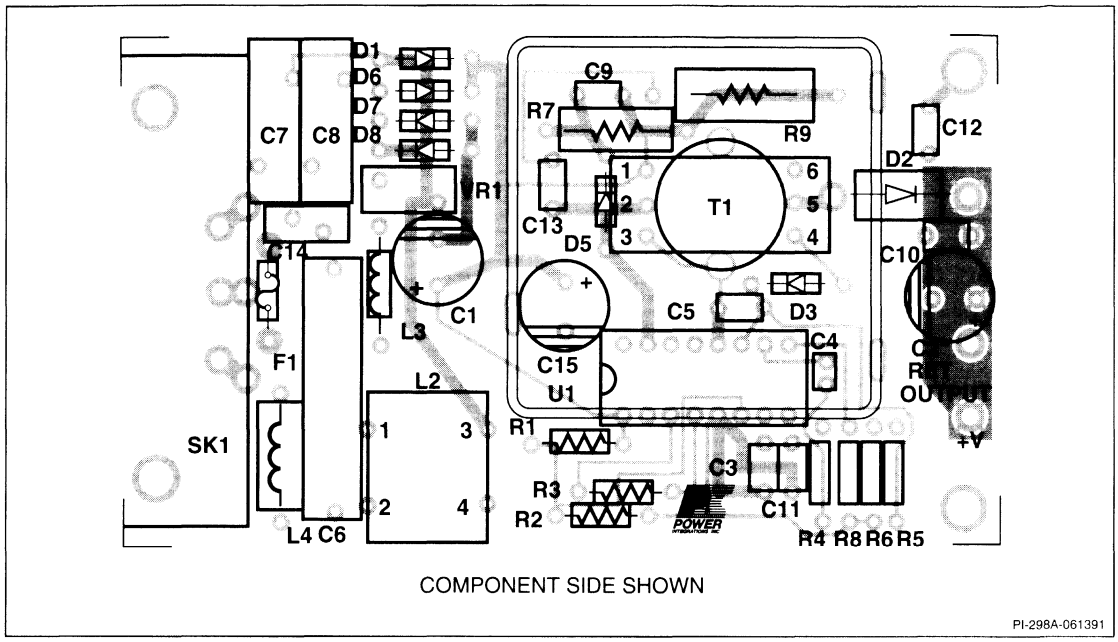

Figure 5. Component Legend of the PWR-EVAL2.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 was measured by applying a DC input voltage to the PWR-EVAL2.

Load Regulation (Figure 6) - The amount of output voltage change for a change in output current is referred to as load regulation. The output changes 5% for a 10% to 100% load current range. Below 10% of rated load the output voltage rises due to the leakage inductance of the transformer[2]. Non-ideal load regulation is caused by the resistance of the transformer output winding, the output rectifier series resistance, and the imperfect coupling between the output winding and the voltage feedback winding. The toroid pulse transformer improves the load regulation by minimizing the effect of the leakage inductance voltage spike on the feedback winding voltage.

The circuit in Figure 3 uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation of ± 5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on the features and trade-offs of feedback winding regulation and optical feedback regulation.

Line Regulation (Figure 7) - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage is 0.5% for a input voltage change of 50 V(rms) or 100 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first cut transformer design procedure. Efficiency at full load and nominal line voltage is 65%.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typical output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[3].

$$PF = \frac{P_{in}}{V_{in} \times I_{in}}$$

The power factor of the PWR-EVAL2 with a 5 W load is approximately 0.6.

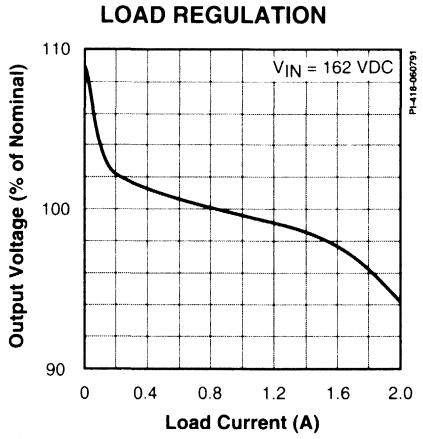

Figure 6.

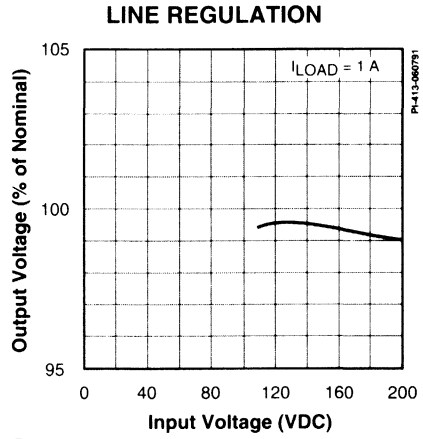

Figure 7.

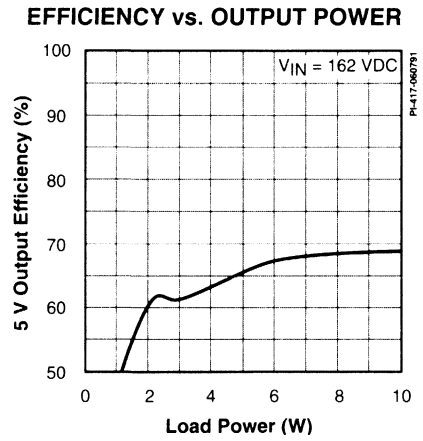

Figure 8.

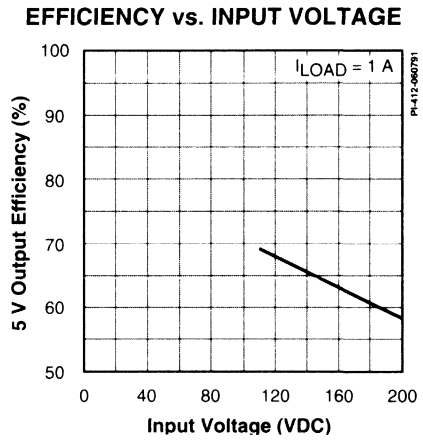

Figure 9.

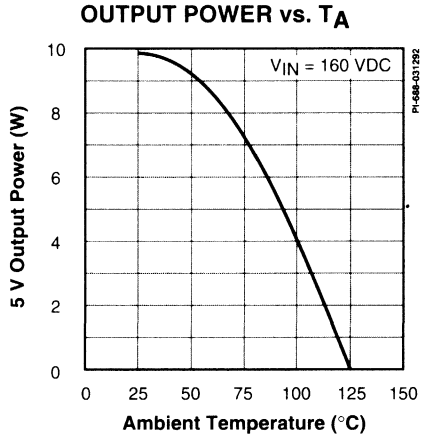

Figure 10.

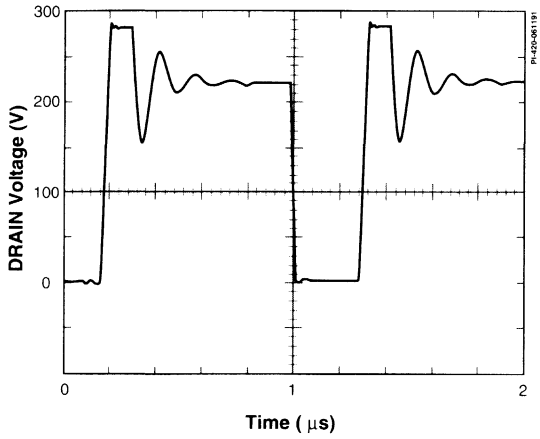

Figure 11. Drain-source Voltage of the PWR-SMP110.

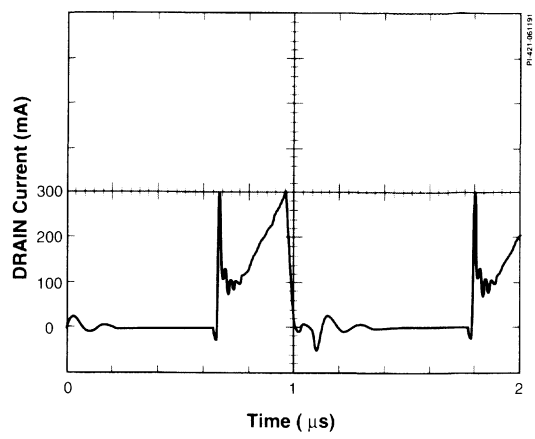

Figure 12. Drain Current of the PWR-SMP110.

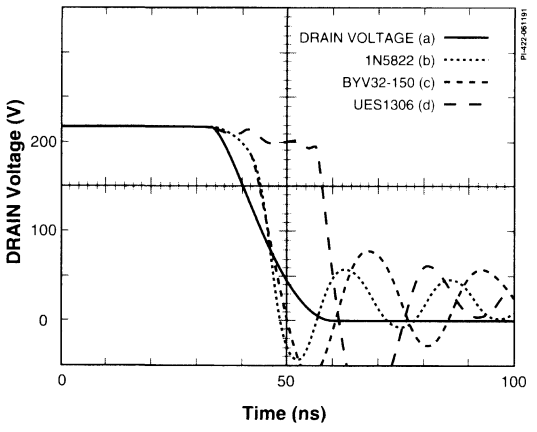

Figure 13. Recovery Times of Output Rectifier Diodes.

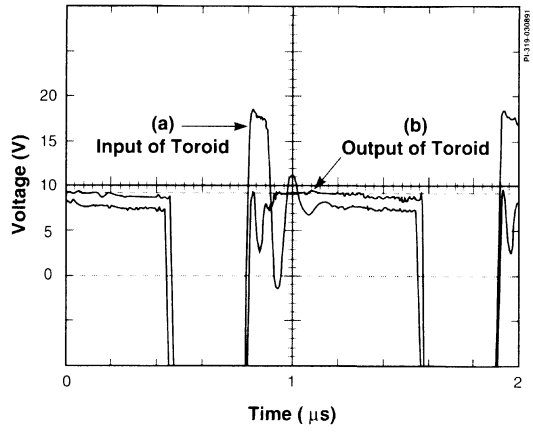

Figure 14. Pulse Transformer Winding Voltages.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a 1N5822 Schottky diode. Figure 13(c) is the anode of D2 when D2 is a BYV32-150 (150 V, 20 A, 35 ns) diode. Figure 13(d) is the anode of D2 when D2 is a UES1306 (400 V, 5 A, 50 ns) diode. The 1N5822 and BYV32-150 exhibit approximately 6 ns recovery times in the circuit, providing good functionality. However, the UES1306 exhibits a 22 ns recovery time in the circuit. This length of recovery time does not work well in the circuit.

The feedback bias supply winding voltage on each side of the pulse transformer winding is shown in Figures 14(a) and (b). This waveform is very important when load voltage regulation is being investigated. Waveform 14(a) is the voltage on the

power transformer side of the pulse transformer. Waveform 14(b) is the voltage on the rectifier side of the pulse transformer. Notice how the pulse transformer has cancelled the leakage inductance spike voltage present on the feedback winding of the power transformer.

Power Supply Turn On Sequence

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the feedback winding and filter provides bias current and turns off the pre-regulator when the power supply is operating. The bias supply voltage at turn-on is shown in Figure 15. It is important to notice how closely the output voltage is coupled to the feedback bias supply. The amount of voltage overshoot is a function of the control loop compensation. If the control loop is made slower by modifying R4 and C4, the overshoot will increase.

The 5.6 volt V_S voltage on pin 7 is derived from pin 11 with a linear regulator. An external bypass capacitor on the V_S pin provides a path for the gate drive switching noise currents to flow.

Output Voltage

The output voltage is controlled by the transformer turns ratio. The PWR-SMP110BNC control circuit will regulate the rectified V_{BIAS} feedback voltage (pin 11) to a typical value of 8.45 V. The output voltage can be estimated by multiplying the output-to-feedback turns ratio by the feedback voltage. A precise method of determining the output voltage would take into account the specific rectifier voltage drop, the resistance of the output winding of the transformer, and the equivalent series resistance of the output capacitor.

The output voltage can be adjusted using the transformer turns ratio. The output voltage can be coarsely tuned by increasing the number of junction voltage drops for D3 and fine tuned with the voltage divider R5 and R6. The R5-R6 voltage divider ratio can be adjusted with a voltage trim resistor (R8).

A higher precision of output voltage regulation can be achieved by sensing and regulating the output voltage directly. This can be accomplished by the use of a secondary side referenced error amplifier and optical coupler circuit as described in AN-8.

Note that V_{BIAS} (pin 11) must be between 8.25 V and 9 V to cut off the high-voltage pre-regulator within U1. Additional information on transformer design is available in AN-7.

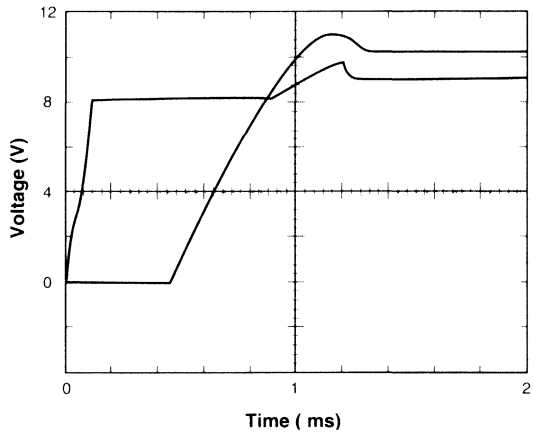

Figure 15. Bias Regulator-Feedback Supply Relationship.

Output Transformer T1001

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies. The T1001 has passed the review of Underwriters Laboratories for use in 110 VAC applications.

The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Toroid Pulse Transformer

The pulse transformer is part of the standard transformer T1001. The transformer generates a voltage pulse on its primary from the rate of change of current in the output rectifier[4]. This voltage pulse is scaled and placed in series with the feedback winding.

The voltage on the output of the pulse transformer is equal, in phase and proportional to the leakage inductance voltage spike. The peak output voltage of the series connection of the feedback winding and the pulse transformer secondary is proportional to the output voltage and is not influenced by the leakage inductance voltage spike. The cancellation effect of the pulse transformer can be seen in Figure 14.

3

Output Transformer T1001 (cont.)

Magnetics Design

The standard transformer has a primary winding with 32 turns of 36 AWG magnet wire, a feedback winding of 5 turns of 36 AWG magnet wire and an output winding of 3 turns of 300 V rated insulated 24 AWG wire. The insulation on the secondary wire meets the voltage breakdown and safety requirements of Underwriters Laboratories.

The pulse transformer has a one turn primary and 12 turns of 36 AWG magnet wire as a secondary.

The nominal primary inductance is 175 µH. The maximum leakage inductance measured on the primary is 13 µH. Approximately 80% of the leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 5 MHz.

The resistance of the primary winding is 1.2 Ω. The resistance of the secondary winding is 0.01 Ω. The resistance of the feedback winding is 0.084 Ω.

The core is a 14 mm x 8 mm pot core. The core material is Siemens M33. This material is a high frequency low loss Ni-Zn ferrite. The A_L value is 171 nH/T^2. The pulse transformer core is Philips 1041T060-4C4.

The power transformer peak flux density at 3 watts is 560 gauss. The peak flux density at 5 watts is 696 gauss. The AC flux density at 5 watts is 565 gauss.

The primary saturation current at 100°C, 2500 gauss, is 1.14 amperes.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.35}{2 \times 6.5 \times 10^5 \times (0.36 - 0.22)} = 183 \mu H$$

where the peak switch current is between the typical current with V_{DS} of 10 V and the minimum current limit current. The primary inductance calculations for the PWR-SMP110 with 5 watts output show an inductance of 183 µH. The efficiency of the PWR-SMP110 at 5 watts and 100 VDC is 65%. The input power will be 7.7 W (5 W divided by 0.65). The average input current at 100 VDC will be 0.077 A (7.7 W divided by 100 V). The average on time current with a 35% duty cycle is 0.22 A (.077 A divided by 0.35). The primary inductance L_p equals 183 µH. The nominal primary inductance of the T1001 is 175 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds / turn = 0).

$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.35}{(1 - 0.35)} \times \frac{115 - 5}{5 + 0.5} = 10.77$$

Single Output Voltage

The standard transformer design can be modified for voltages other than 5 volts. This is achieved by changing the secondary winding to feedback winding turns ratio. The output voltage can be fine tuned by adjusting the R5, R6 voltage divider. However, the voltage on pin 11 of the PWR-SMP110BNC must be within the voltage range specified in the data sheet.

If the turns count on the secondary is greater than three, a larger core will be required to accommodate the larger number of insulated turns on the bobbin. Multiple output voltages are also possible (refer to AN-7).

Output Transformer T1001 (cont.)

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C13 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C13 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package, the ambient temperature[5], and the peak switching transistor current limit circuit. The available output power as a function of input voltage for an 80°C temperature rise (junction to ambient) is shown in Figure 16.

Thermal Characteristics

The PWR-SMP110BNC is packaged in a 16-pin plastic power DIP package[6]. This package offers a lower thermal impedance as compared to a standard plastic DIP package. The thermal impedance from junction to ambient and from junction to case are 43°C/Watt and 6°C/Watt respectively. Soldered connections to the heat spreading "wings" (pins 4, 5, 12, and 13) provide a good thermal path while the DIP form factor maintains compatibility with automatic insertion equipment for low cost assembly. The thermal impedance from case to local ambient on a typical power supply board is 43-6 = 37°C/W. The local ambient temperature can be 10°C above ambient due to heating from other components on the printed circuit board.

The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and the transformer and damping network capacitances[7], and the losses in the pre-regulator when it is active. Figure 17 is the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 18. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this Figure to determine the total AC losses in the circuit.

Additional information on thermal management is available in AN-9.

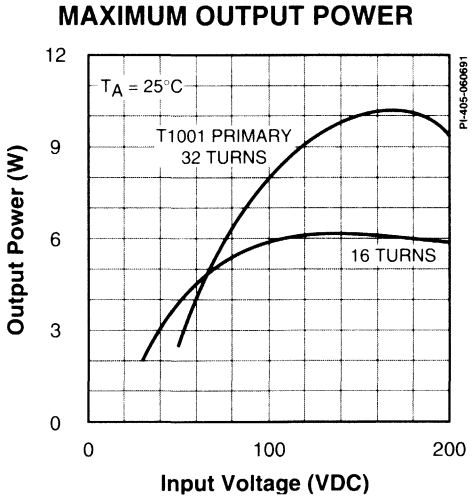

Figure 16.

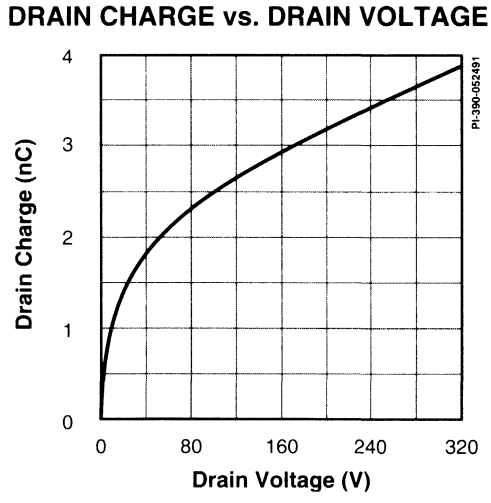

Figure 17.

3

Current Limit

The current limit function of the PWR-SMP110BNC uses the internal over temperature protection function and the constant current characteristic of the output switching transistor. An over current condition on the output will cause the current in the switching transistor to increase. The output switching transistor turns into a constant current source above the rated switching current and below the maximum rated current, when the fault condition causes the switch current to approach this current the power dissipation in the switching transistor increases to a sufficient level that the over temperature protection circuit turns the power supply off until the junction temperature cools typically 45°C from the thermal shutdown temperature. The output power vs. input voltage curve of Figure 16 can provide an estimate of the power available for 25°C ambient.

Operating Frequency

The operating frequency of the PWR-EVAL2 is typically 850 kHz. A timing capacitor of 25 pF for the oscillator is internal to the PWR-SMP110BNC. The frequency of operation is adjustable and the printed circuit board has a location for an external frequency setting capacitor C11 connected to pin 8 of U1. The nominal operating frequency can be estimated with the following formula:

$$f = \frac{67.4\mu A}{\frac{2.2V}{25pF + C_{EXT}}}$$

Voltage Control Loop

The PWR-SMP110BNC has a voltage-mode control circuit[9]. The DC input to output voltage transfer function when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[10]. The duty cycle is controlled by the output voltage error amplifier. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[11,12] is included in the documentation disk. T1, U1, R4, R5, C2 and C4 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The model for the operating point duty cycle transformation uses a transconductance generator and a voltage gain stage. The coefficients of the small signal pulse width modulator transfer-function generators are calculated by knowing the primary reflex voltage (output voltage plus rectifier forward drop times the transformer turns ratio), the duty cycle of the operating point of interest and the load resistance transformed to the primary of the transformer:

$$R = R_O \times \left(\frac{N_P}{N_S}\right)^2 = 5 \times \left(\frac{32}{3}\right)^2 = 569\Omega$$

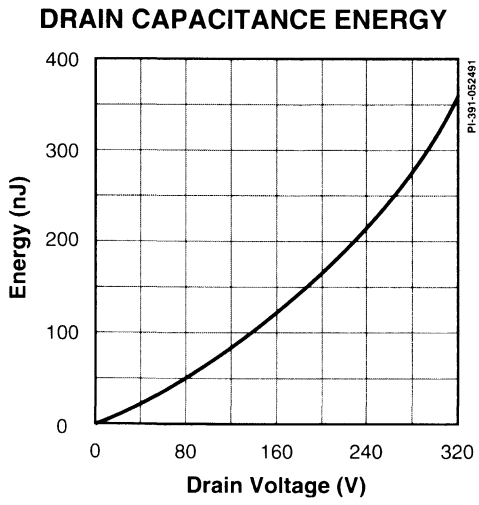

Figure 18.

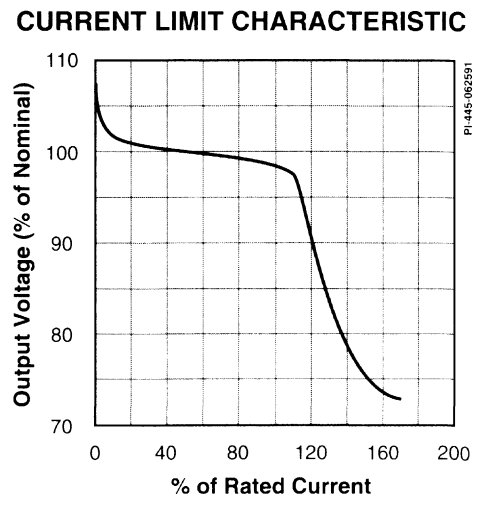

Figure 19.

The voltage generator gain:

$$E = \frac{-V}{D^2} = \frac{-59}{(0.269)^2} = -813$$

The current generator gain:

$$J = \frac{-V}{(1-D)^2 \times R} = \frac{-59}{(1-0.269)^2 \times 569} = -0.19426$$

The current generator is to provide the negative input impedance effect of a switching regulator and can be neglected if the resonant frequency of the EMI filter is much higher than the control loop frequencies of interest.

The measured power supply open loop gain/phase response curve is shown in Figure 20. The control loop has 85 degrees phase margin, an open loop unity gain crossover frequency of 29 kHz and 11.6 dB gain margin at 178 kHz with a 5 watt load. This provides 45 dB of gain at 120 Hz for power line ripple rejection.

The output ripple voltage at the power line frequency can be estimated by knowing the open loop gain of the regulator, the transformer turns ratio and the operating duty cycle of the flyback switching regulator. The output peak to peak ripple voltage at the power line frequency can be calculated from the following equation:

$$V_{o(pp)} = \frac{V_{in(pp)} \times \frac{N_S}{N_P} \times \frac{D}{1-D}}{A_V} = \frac{20 \times \frac{3}{32} \times \frac{0.27}{1-0.27}}{178} = 3.9\text{mV}$$

The DC model for the error amplifier within the integrated circuit is shown in Figure 21. Figure 22, the error amplifier open-loop gain/phase response curve, shows that the amplifier is stable in the unity gain feedback configuration.

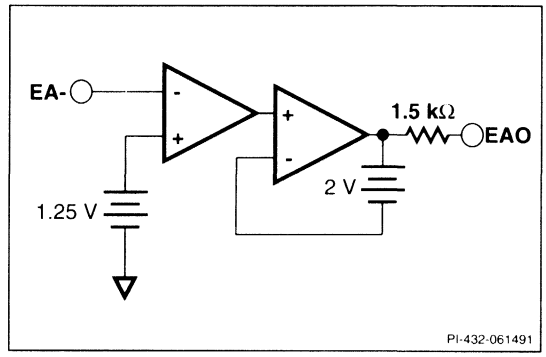

Figure 21. Error Amplifier Equivalent Circuit.

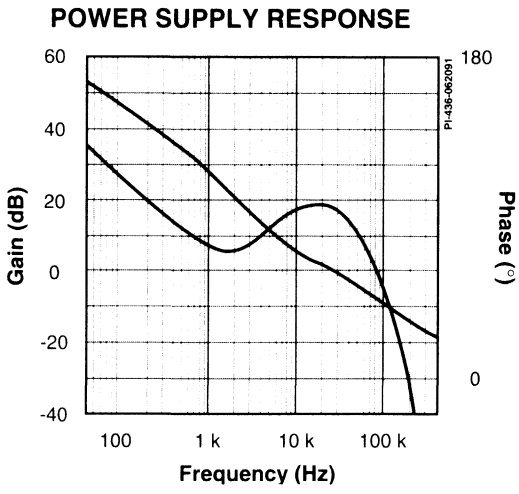

Figure 20.

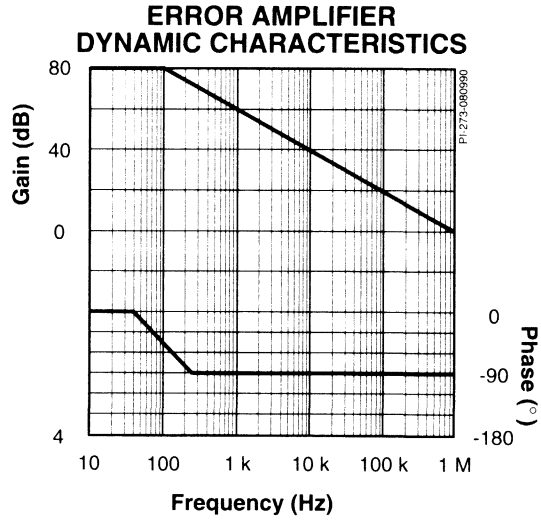

Figure 22.

Protection Features

Overtemperature
The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 135°C and keeps it off until the junction temperature decreases 45°C[13].

Input Overvoltage Protection
The voltage divider R1 and R2 sets the point where the input overvoltage comparator will inhibit the power supply output. The switching power transistor will be turned off when pin 6 exceeds 1.25 V. For the PWR-EVAL2, this translates to an input voltage of:

$$1.25 \times \frac{825.1}{5.1} = 202\text{V}$$

The switching power transistor will be turned back on when pin 6 drops below 1.2 V. For the PWR-EVAL2, this translates to an input voltage of:

$$1.2 \times \frac{825.1}{5.1} = 194\text{V}$$

Input Undervoltage Protection
The switching power transistor will be turned off when pin 6 drops below 0.34 volts. This translates to:

$$0.34 \times \frac{825.1}{5.1} = 55\text{V}$$

The switching power transistor will be turned back on when pin 6 exceeds 0.39 volts. This translates to:

$$0.39 \times \frac{825.1}{5.1} = 63\text{V}$$

Test Mode
The OV/UV control (pin 6) controls the built in test logic of the integrated circuit. The built-in test logic turns on the power transistor continuously when the voltage on pin 6 is equal to the pin 7 voltage (5.6 volts) +/- 1.5 V Do not put the circuit in test mode while operating in a power supply circuit as this could destroy the PWR-SMP110.

Control Circuit Undervoltage Protection
The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is typically 5 volts on pin 7.

Input Filtering and Rectification
D1, D6, D7, D8, C1, and C15 perform the input rectification and filtering function. The rectifier diodes should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage ratings on C1 and C15 are equal to the peak value of the maximum rectified input voltage, 200 V for 115 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitors C1 and C15 can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage the power supply will provide a regulated output voltage at maximum power, and the minimum AC input voltage[14]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 and C15 when the input bridge diodes stop conducting, and V_2 is the voltage on C1 and C15 when the input bridge diodes start conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the input capacitor value.

Input Surge Current

When line voltage is applied to the power supply a surge of current flows in the input of the power supply to charge the input storage capacitors C1 and C15[15]. The magnitude of current must be within the surge ratings of the power switch, fuse and input rectifiers. The surge current is limited by the resistance of the EMI filter. L3, the differential mode filter inductor contributes the majority of the EMI filter resistance of 8 Ω. This limits the peak surge current to 160 V/8 Ω = 20 A.

EMI Considerations

This power supply was designed to meet worldwide EMI (FCC, part 15, subpart J) and safety (UL1950 and IEC950) specifications. Figure 23 is a plot of the conducted EMI relative to the FCC specification limits.

Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L3 and C6 filter differential mode conducted emissions.

Common Mode Filter
L2, L4, C7, C8, C12, and C14 filter common mode conducted emission currents[16]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C12 couples high-frequency noise back to the system chassis ground. C7, C8, and C14 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP110. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L4 in series with the ground lead of the power connector is a "lossy" bead and is equivalent to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

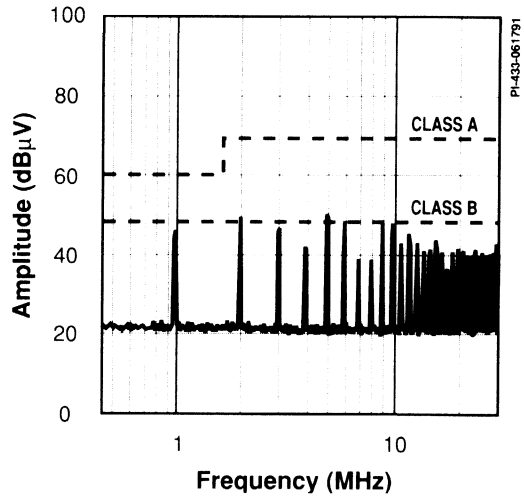

Figure 23. EMI Plot of the PWR-EVAL2.

Safety Agency Requirements

The PWR-EVAL2 has been designed to meet UL1950. The design is based on the PWR-EVAL1 which is a recognized component (UL file #E131417). The same PC board and power transformer are used for both the PWR-EVAL1 and the PWR-EVAL2.

Additional information on safety and layout-related issues is available in DA-2.

Documentation Disks

The PWR-EVAL2 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL2 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README2.BAT	(This file) contains a summary and last minute information on PWR-EVAL2
PWB1001B.APR	Aperture file with assigned D-codes
EVAL2.BOM	Bill of Materials file
EVAL2ASY.DWG	Assembly drawing file
FAB1001B.DWG	Fabrication drawing for the PC board
SHLD12.DWG	Fabrication drawing for the optional shield over the power supply
1001B.G23	Gerber file of all layers
EVAL2.LIB	Library file of the part symbols used in both schematics
EVAL2.SCH	Schematic file of PWR-EVAL2
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES2.TXT	Functional description of the power supply circuitry used in PWR-EVAL2
ICDESC2.TXT	Functional description of the PWR-SMP110 integrated circuit used in PWR-EVAL2
EVL2COST.TXT	Estimated parts cost
T1001 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README2.BAT and the EVAL2.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations on request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP110.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

References

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2 Wilson Jr.,Thomas "Cross Regulation in an Energy-Storage DC-to-DC Converter with Two Regulated Outputs" PESC 77 Record, pp. 190-199

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5 Davis, Paul A. "Thermal Packaging Concepts in Power Supply Design" HFPC 89 Proceedings, May 1989, pp. 446-458

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7 Keller, R., Leman, B. "New Integrated Technology Combines 800 V High-Speed Power MOSFET Switch with Pulse Width Modulation Control Circuitry for Power System Applications" Proceedings, High Frequency Power Conversion International June 1991, p. 61

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9 Middlebrook, R.D. "Power Electronics: Topologies, Modeling and Measurement" Proceedings of the IEEE International Symposium on Circuits and Systems, 1981 Record, April 27-29 1981

10 Severns, R.P., Gordon, E. Modern DC-DC Switchmode Power Converter Circuits Van Nostrand Reinhold Company, p 231

11 Middlebrook, R.D., Cuk, Slobodan, "Modeling and Analysis Methods for DC-to-DC Switching Converters" Proceedings of the IEEE International Semiconductor Power Converter Conference, 1977 Record, pp. 90-111

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13 Thermal Shutdown Application notes: National Semiconductor AN-82, AN-103

14 Tartar, Ralph E., Principles of Solid-state Power Conversion Howard W. Sams & Co., Inc., 1985, p. 232

15 Hirshberg, Walter "Optimizing Line Inrush Design in Off-Line Converters" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, E3.1-E3.7

16 Nave, Mark J. "Measuring, Suppressing, and Filtering Common Mode Emissions in Switch-Mode Power Supplies" HFPC 89 Proceedings, May 1989, pp. 285-293

PWR-EVAL3

PWR-SMP120 Evaluation Board

110 VAC Input
Isolated 5 V, 20 W Output

POWER INTEGRATIONS, INC.

Product Highlights

Isolated 5 V Output from 110 VAC Input

- Up to 20 watts of output power can be supplied
- Isolation is provided by transformer designed to UL specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits

- Input overvoltage shutdown
- Input undervoltage lockout
- Integrated current limit
- Thermal Shutdown

Designed to Meet Regulatory Standards

- Layout designed to meet UL/CSA requirements
- Designed to meet FCC Class A

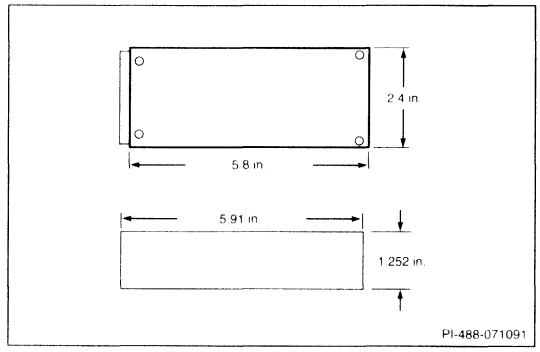

Figure 1. Evaluation Board Overall Physical Dimensions.

Description

The PWR-EVAL3 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP120BNC power supply IC.

The PWR-SMP120, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a switchmode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP120 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP120 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL3 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

PARAMETER	LIMITS
Input Voltage Range	85 to 130 VAC
Input Frequency Range	47 to 440 Hz
Output Voltage Range	4.5 to 5.5 VDC
Load Current Range	0.6 to 4 A
Temperature Range	0 to 70°C
Efficiency	> 78%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	OPERATING VOLTAGE
PWR-EVAL3	110 VAC INPUT 5 VDC OUTPUT @ 20W

3

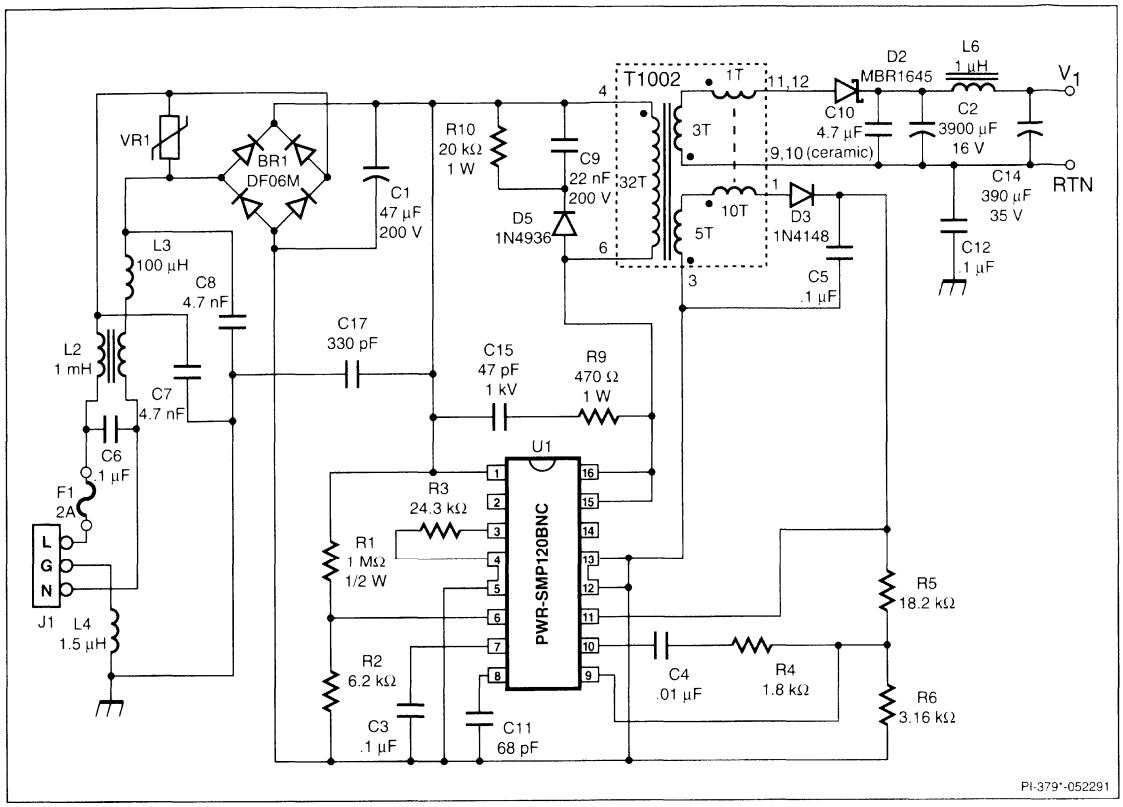

Figure 3. Schematic Diagram of the PWR-EVAL3 Power Supply.

General Circuit Description

The PWR-EVAL3 is an isolated Buck-Boost or flyback switching power supply topology[1]. The power supply is implemented using the PWR-SMP120BNC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 20 watt power supply that will operate from 85 to 140 VAC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding of T1002. The PWR-SMP120 has been designed for a bias voltage (pin 11), of 8.5 volts. The effective transformer volts-per-turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. The three main elements that affect the regulation of the output voltage are; maintenance of a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

The circuit groups in the schematic Figure 3 are as follows. L2, L3, L4, C6, C7, C8, C12, and C17 form the EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. The voltage divider formed by R1 and R2 set the input voltage that activates the input undervoltage and overvoltage shutdown functions. D5, C9 and R7 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP120. C3 and C5 are bypass capacitors.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	47 µF, 200 V	UVX2D470MHA	Nichicon (America)
C2	3900 µF, 16 V	UPL1V392MRH6	Nichicon (America)
C3, C5, C12	100 nF, 50 V	K104Z20Z5UFVBWN	Mepco/Centralab
C4	10 nF, 50 V	K103M15X7RFVBWA	Mepco/Centralab
C6	100 nF-S, 250 VAC	QXW2E104KTPT	Nichicon (America)
C7, C8	4.7 nF-S, 250 VAC	440LD47	Cera-Mite(Sprague)
C9	22 nF, 200 V	C320C223K2R5CA	KOA
C10	4.7 µF, 25 V	TCD41E1H475M	Marcon
C11	68 pF	K680J15COGFVBWA	Mepco/Centralab
C14	390 µF, 35 V	UPL1V391MPH	Nichicon (America)
C15	47 pF, 1 kV	5GAQ47	Cera-Mite(Sprague)
BR1	1 A, 600 V	DF06M	General Instrument
D2		MRB1645	Motorola
D3		1N4148	Motorola
D5		1N4936	Motorola
F1	2 A, 125 VAC	230.002	Littlefuse/Tracor
L2	1 mH	SC-01-10G	Tokin
L3	100 µH	LFC101K	Inductor Supply
L4	1.5 µH	2673200201	Fair-Rite Products
L6	1 µH	CTX1-4FR	Coiltronics
R1	1 MΩ, 1/2 W, 5%	5053CX1M000J	Mepco/Centralab
R2	6.2 kΩ, 1/4 W, 5%	5043CXK6K280J	Mepco/Centralab
R3	24.3 kΩ, 1/4 W, 1%	5043ED24K30F	Mepco/Centralab
R4	1.8 kΩ, 1/4 W, 5%	5043CXK1K80J	Mepco/Centralab
R5	18.2 kΩ, 1/4 W, 1%	5043ED18K20F	Mepco/Centralab
R6	3.16 kΩ, 1/4 W, 1%	5043ED3K160F	Mepco/Centralab
R9	470 Ω, 1 W, 5%	5073YL470R0J	Mepco/Centralab
R10	20 kΩ, 1 W, 5%	5053CX20K00J	Mepco/Centralab
U1		PWR-SMP120BNC	Power Integrations, Inc.
VR1	130 VAC	V130LA1	Harris
T1	5 V Output	T1002	Custom *
J1	Plug Socket	C6480	USD Products/Cooper
	P C Board	PWB-1002B	Custom **

Custom Components:

* Qualified manufacturers are:

AT&T Microelectronics	(800) 372-2447	FAX: (214) 284-8282
Datatronics	(714) 928-7731	FAX: (714) 928-7701
Delta (Taiwan)	(02) 7164822	FAX: (02) 7169764
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin (Japan)	(03) 402-6166	FAX: (03) 497-9756

** Manufacturer is:

CBR
116 Minnis Court
Milpitas, CA 95035
(408) 946-3446

*** Drawing is available from Power Integrations, Inc.

Figure 4. Parts List for the PWR-EVAL3

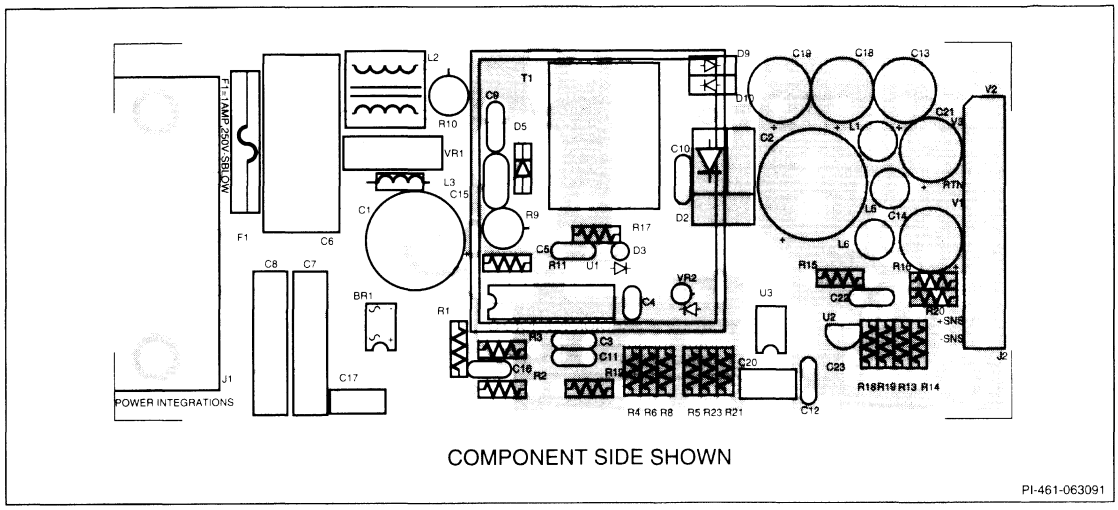

Figure 5. Component Legend of the PWR-EVAL3.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 was measured by applying a DC input voltage to the PWR-EVAL3.

Load Regulation (Figure 6) - The amount of output voltage change for a change in output current is referred to as load regulation. The output changes 10% for a 10% to 100% load current range. Below 10% of rated load the output voltage rises due to the leakage inductance of the transformer[2]. Non-ideal load regulation is caused by the resistance of the transformer output winding, the output rectifier series resistance, and the imperfect coupling between the output winding and the voltage feedback winding. The toroid pulse transformer improves the load regulation by minimizing the effect of the leakage inductance voltage spike on the feedback winding voltage.

The circuit in Figure 3 uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and setibility of ± 5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on the features and trade-offs of feedback winding regulation and optical feedback regulation.

Line Regulation (Figure 7) - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage is 1% for a input voltage change of 50 V(rms) or 200 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first cut transformer design procedure. Efficiency at full load and nominal line voltage is 78%.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typical output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[3].

$$PF = \frac{P_{in}}{V_{in} \times I_{in}}$$

The power factor of the PWR-EVAL3 with a 20 W load is approximately 0.6.

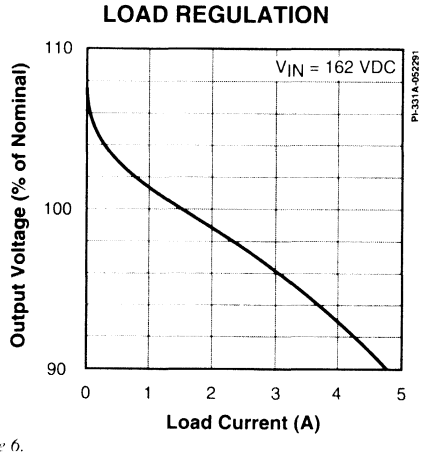

Figure 6.

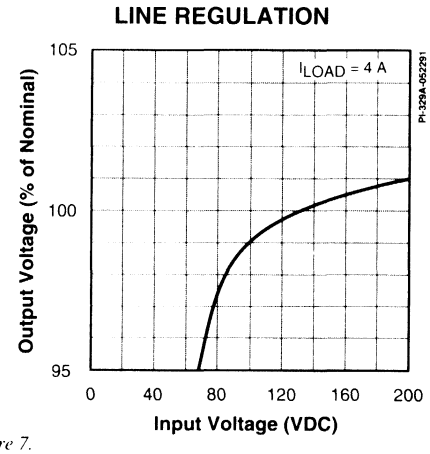

Figure 7.

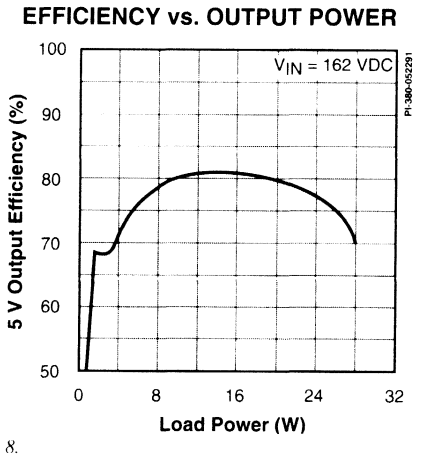

Figure 8.

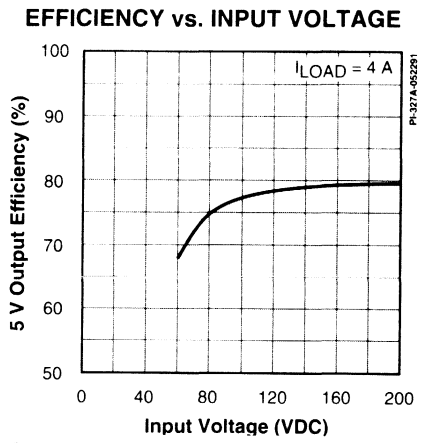

Figure 9.

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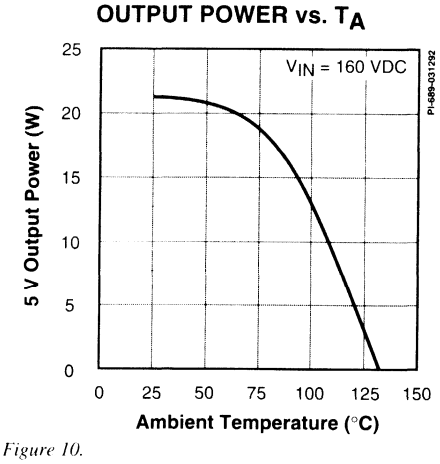


Figure 10.

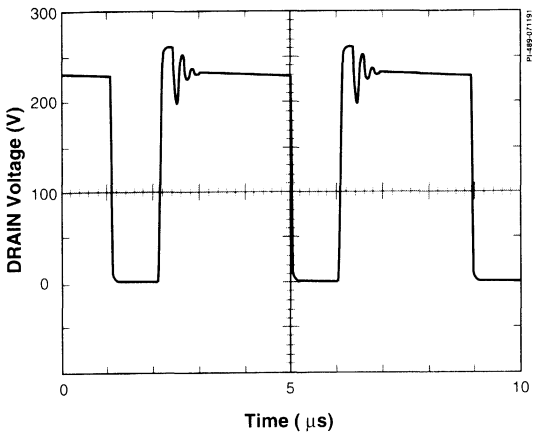


Figure 11. Drain-source Voltage of the PWR-SMP120.

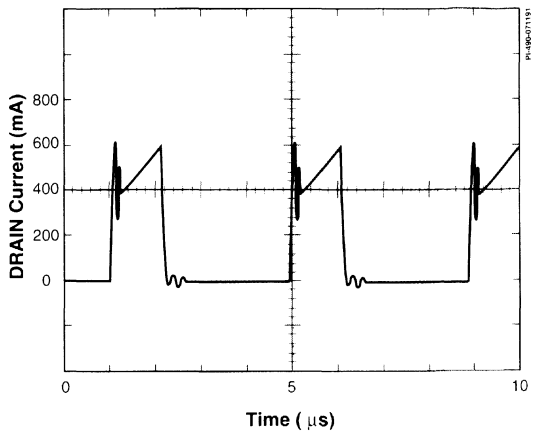


Figure 12. Drain Current of the PWR-SMP120.

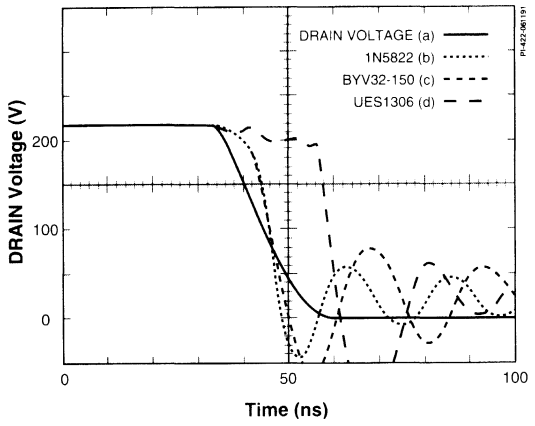


Figure 13. Recovery Times of Output Rectifier Diodes.

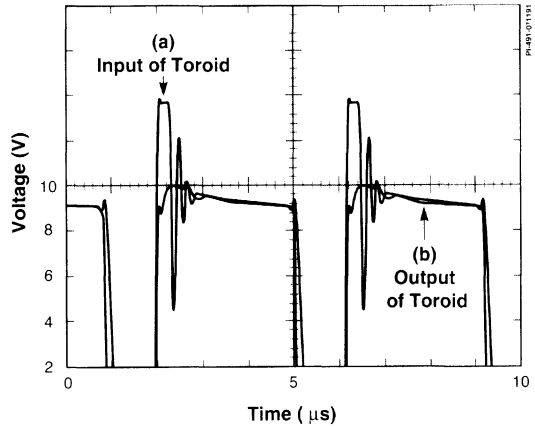


Figure 14. Pulse Transformer Winding Voltages.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a MBR1645 Schottky diode. Figure 13(c) is the anode of D2 when D2 is a BYV32-150 (150 V, 20 A, 35 ns) diode. Figure 13(d) is the anode of D2 when D2 is a UES1306 (400 V, 5 A, 50 ns) diode. The MBR1645 and BYV32-150 exhibit approximately 6 ns recovery times in the circuit, providing good functionality. However, the UES1306 exhibits a 22 ns recovery time in the circuit. This length of recovery time does not work well in the circuit.

The feedback bias supply winding voltage on each side of the pulse transformer winding is shown in Figures 14(a) and (b). This waveform is very important when load voltage regulation is being investigated. Waveform 14(a) is the voltage on the

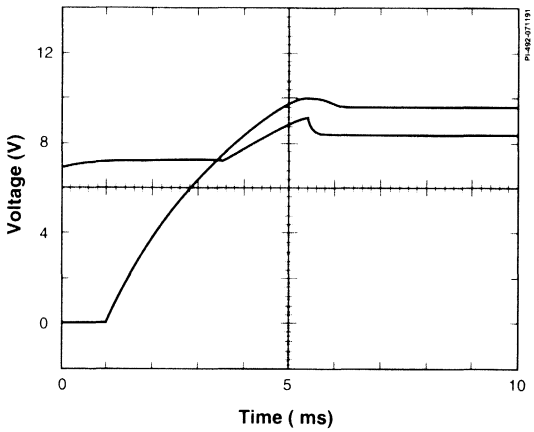


Figure 15. Bias Regulator-Feedback Supply Relationship.

power transformer side of the pulse transformer. Waveform 14(b) is the voltage on the rectifier side of the pulse transformer. Notice how the pulse transformer has cancelled the leakage inductance spike voltage present on the feedback winding of the power transformer.

Power Supply Turn On Sequence

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. This regulator maintains the voltage on pin 11 at approximately 7.5 V. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the feedback winding and filter provides bias current and turns off the pre-regulator when the power supply is operating. The bias supply voltage at turn-on is shown in Figure 15. It is important to notice how closely the output voltage is coupled to the feedback bias supply. The amount of voltage overshoot is a function of the control loop compensation. If the control loop is made slower by modifying R4 and C4, the overshoot will increase.

The 5.6 volt V_S voltage on pin 7 is derived from pin 11 with a second linear regulator. An external bypass capacitor on the V_S pin provides a path for the gate drive switching noise currents to flow.

Output Voltage

The output voltage is controlled by the transformer turns ratio. The PWR-SMP120BNC control circuit will regulate the rectified V_{BIAS} feedback voltage (pin 11) to a typical value of 8.45 V. The output voltage can be estimated by multiplying the output-to-feedback turns ratio by the feedback voltage. A precise method of determining the output voltage would take into account the specific rectifier voltage drop, the resistance of the output winding of the transformer, and the equivalent series resistance of the output capacitor.

The output voltage can be adjusted using the transformer turns ratio. The output voltage can be coarsely tuned by increasing the number of junction voltage drops for D3 and fine tuned with the voltage divider R5 and R6. The R5-R6 voltage divider ratio can be adjusted with a voltage trim resistor (R8).

A higher precision of output voltage regulation can be achieved by sensing and regulating the output voltage directly. This can be accomplished by the use of a secondary side referenced error amplifier and optical coupler circuit as described in AN-8.

Note that V_{BIAS} (pin 11) must be between 8.25 V and 9 V to cut off the high-voltage pre-regulator within U1. Additional information on transformer design is available in AN-7.

Output Transformer T1002

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies.

The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Toroid Pulse Transformer

The pulse transformer is part of the standard transformer T1002. The transformer generates a voltage pulse on its primary from the rate of change of current in the output rectifier[4]. This voltage pulse is scaled and placed in series with the feedback winding.

The voltage on the output of the pulse transformer is equal, in phase and proportional to the leakage inductance voltage spike. The peak output voltage of the series connection of the feedback

Output Transformer T1002 (cont.)

winding and the pulse transformer secondary is proportional to the output voltage and is not influenced by the leakage inductance voltage spike. The cancellation effect of the pulse transformer can be seen in Figure 14.

Magnetics Design

The standard transformer has a primary winding with 32 turns of 30 AWG magnet wire, a feedback winding of 5 turns of 35 AWG magnet wire and an output winding of 3 turns with two wires bifilar wound of 300 V rated insulated 24 AWG wire. The insulation on the secondary wire meets the voltage breakdown and safety requirements of Underwriters Laboratories.

The pulse transformer has a one turn primary and 10 turns of 35 AWG magnet wire secondary.

The nominal primary inductance is 738 µH. The maximum leakage inductance measured on the primary is 18 µH. Approximately 80% of the leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 1 MHz.

The resistance of the primary winding is 0.54 Ω. The resistance of the secondary winding is 0.005 Ω. The resistance of the feedback winding is 0.037Ω.

The core is a PQ 2016 style core. The core material is Magnetics Inc "P" material. The AL value is 721 nH/T^2. The pulse transformer core is Micrometals T30-8/90 powdered iron toroid.

The power transformer AC flux density at 20 watts and 250 kHz is 773 gauss.

The primary saturation current at 100°C, 3800 gauss, is 1.02 ampere.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.45}{2 \times 3.3 \times 10^5 \times (0.9 - 0.556)} = 188\mu H$$

where the peak switch current is between the typical current with V_{DS} of 10 V and the minimum current limit current. The primary inductance calculations for the PWR-SMP120 with 20 watts output show an inductance of 188 µH. The efficiency of the PWR-SMP120 at 20 watts and 100 VDC is 80%. The input power will be 25 W (20 V divided by 0.8). The average input current at 100 VDC will be 0.25 A (25 W divided by 100 V). The average on time current with a 45% duty cycle is 0.556 A (.25 A divided by 0.45). The primary inductance L_p equals 188 µH. The nominal primary inductance of the T1002 is 738 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds / turn = 0).

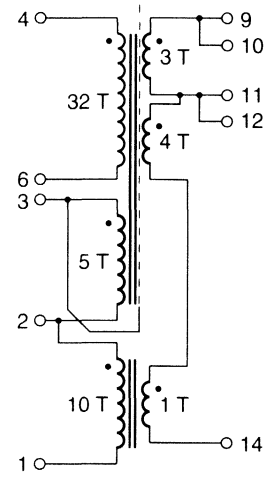
$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.45}{(1 - 0.45)} \times \frac{115 - 5}{5 + 0.5} = 16.4$$

Single Output Voltage

The standard transformer design can be modified for voltages other than 5 volts. This is achieved by changing the secondary winding to feedback winding turns ratio. The output voltage can be fine tuned by adjusting the R5, R6 voltage divider. However, the voltage on pin 11 of the PWR-SMP120BNC must be within the voltage range specified in the data sheet.

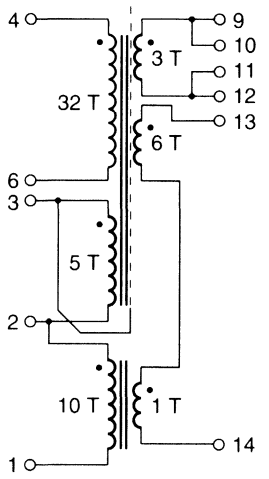


CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	+5 V OUTPUT
14	+12 V OUTPUT

PI-428-061391

Figure 16. 5/12 V Transformer Schematic Diagram.



CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	N/C
13	+5 V OUTPUT
14	+15 V OUTPUT

PI-429-061391

Figure 17. 5/15 V Transformer Schematic Diagram.

Output Transformer T1002 (cont.)

The output voltage can be increased to 12 volts by increasing the secondary to 7 turns. The transformer will generate 1.8 volts/turn less a 0.6 volt diode drop yields 12 volts.

The output voltage can be increased to 15 volts by increasing the secondary to 8 turns and increasing the number of junctions in D3 to two. The two junctions for D3 increases the output to 1.96 volts/turn. A 0.6 volt diode drop will yield a 15 volt output.

Multiple Output Voltages

The number of output voltages can be increased by adding additional output turns and voltage taps. A 5 volt and 12 volt output can be achieved with a 7 turn winding with a tap at 3 turns as shown in Figure 16. Figure 17 shows how a 5 volt and 15 volt output can be achieved with a 6 turn winding and a 3 turn winding. This scheme creates two separate supplies, 5 V and 10.5 V, and connects them in series.

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C15 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C15 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1.

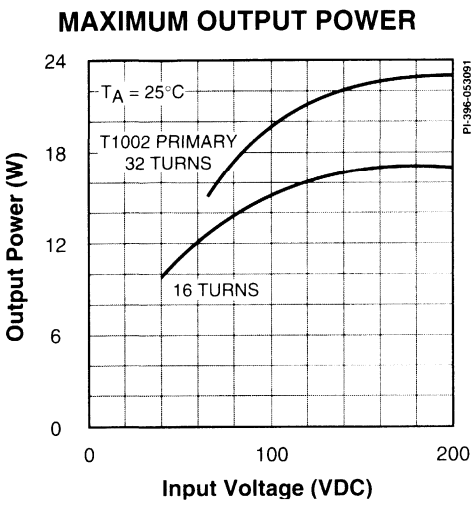


Figure 18.

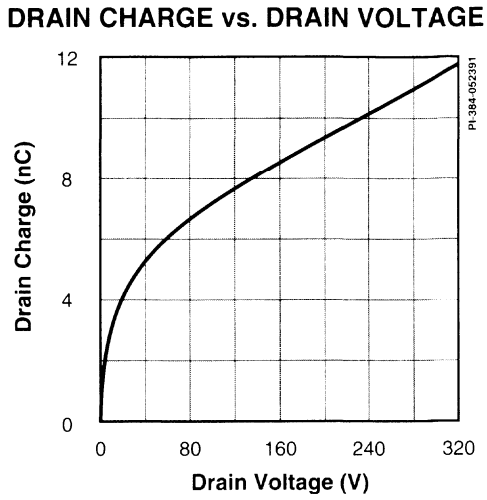


Figure 19.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package, the ambient temperature[5], and the peak switching transistor current limit circuit. The available output power as a function of input voltage for an 80°C temperature rise (junction to ambient) is shown in Figure 18.

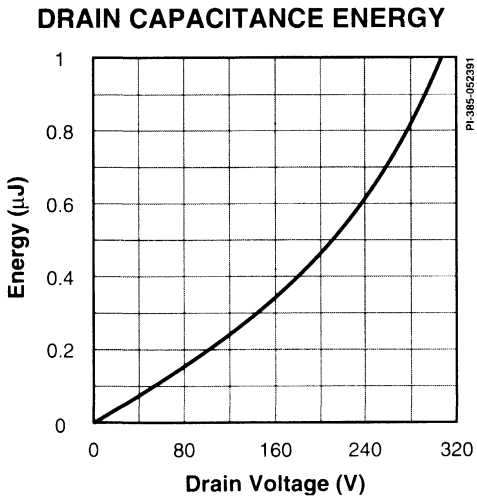


Figure 20.

Thermal Characteristics

The PWR-SMP120BNC is packaged in a 16-pin plastic power DIP package[6]. This package offers a lower thermal impedance as compared to a standard plastic DIP package. The thermal impedance from junction to ambient and from junction to case are 43°C/Watt and 6°C/Watt respectively. Soldered connections to the heat spreading "wings" (pins 4, 5, 12, and 13) provide a good thermal path while the DIP form factor maintains compatibility with automatic insertion equipment for low cost assembly. The thermal impedance from case to local ambient on a typical power supply board is 43-6 = 37°C/W. The local ambient temperature can be 10°C above ambient due to heating from other components on the printed circuit board.

The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and the transformer and damping network capacitances[7], and the losses in the pre-regulator when it is active. Figure 19 is the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 20. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this Figure to determine the total AC losses in the circuit.

Additional information on thermal management is available in AN-9.

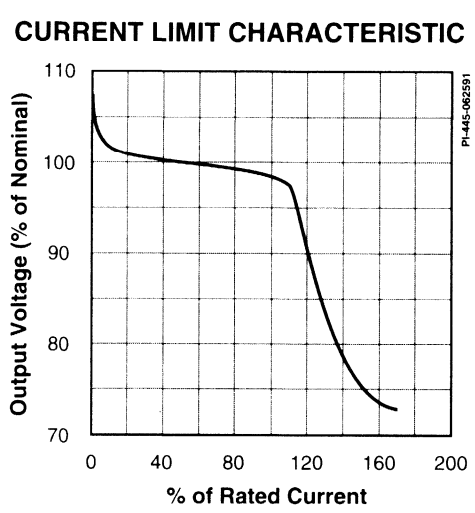


Figure 21.

Current Limit

The current limit circuit is internal to the PWR-SMP120BNC and is a peak detection type of circuit. The circuit monitors the current flowing in the switching transistor. When the current exceeds the typical value of 1.1 A for 100 ns the switching transistor is turned off for the rest of the oscillator cycle. The effect on the output voltage can be seen in Figure 21. The shape of the current limit function is very close to a constant power curve[8]. This is because the circuit regulates the peak current in the transformer primary providing a constant energy delivery to the core during current limit, thus a constant power output in current limit.

Current limit is implemented within the integrated circuit by applying a current sense signal to a comparator input. The comparator triggers a latch which turns the power transistor off until the next clock cycle.

Operating Frequency

The operating frequency of the PWR-EVAL3 is typically 330 kHz. A timing capacitor of 25 pF for the oscillator is internal to the PWR-SMP120BNC. The frequency of operation is adjustable and the printed circuit board has a location for an external frequency setting capacitor C11 connected to pin 8 of U1. The nominal operating frequency can be estimated with the following formula:

$$f = \frac{67.4\mu A}{\frac{2.2V}{25pF + C_{EXT}}}$$

Voltage Control Loop

The PWR-SMP120BNC has a voltage-mode control circuit[9]. The DC input to output voltage transfer function when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[10]. The duty cycle is controlled by the output voltage error amplifier. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[11,12] is included in the documentation disk. T1, U1, R4, R5, C2 and C4 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The model for the operating point duty cycle transformation uses a transconductance generator and a voltage gain stage. The coefficients of the small signal pulse width modulator transfer-function generators are calculated by knowing the primary reflex voltage (output voltage plus rectifier forward drop times the transformer turns ratio), the duty cycle of the operating point of interest and the load resistance transformed to the primary of the transformer:

$$R = R_O \times \left(\frac{N_P}{N_S}\right)^2 = 5 \times \left(\frac{32}{3}\right)^2 = 569\Omega$$

The voltage generator gain:

$$E = \frac{-V}{D^2} = \frac{-59}{(0.269)^2} = -813$$

The current generator gain:

$$J = \frac{-V}{(1-D)^2 \times R} = \frac{-59}{(1-0.269)^2 \times 569} = -0.19426$$

The current generator is to provide the negative input impedance effect of a switching regulator and can be neglected if the resonant frequency of the EMI filter is much higher than the control loop frequencies of interest.

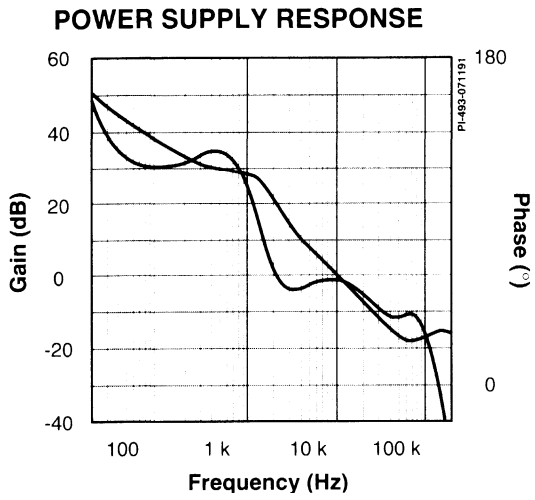


Figure 22.

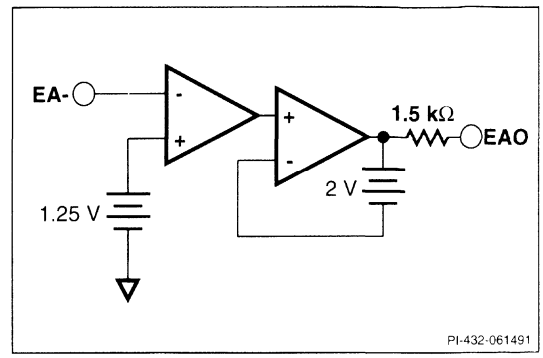


Figure 23. Error Amplifier Equivalent Circuit.

The measured power supply open loop gain/phase response curve is shown in Figure 22. The control loop has 57 degrees phase margin, an open loop unity gain crossover frequency of 10.5 kHz and 15 dB gain margin at 138 kHz with a 20 watt load. This provides 38 dB of gain at 120 Hz for power line ripple rejection.

The output ripple voltage at the power line frequency can be estimated by knowing the open loop gain of the regulator, the transformer turns ratio and the operating duty cycle of the flyback switching regulator. The output peak to peak ripple voltage at the power line frequency can be calculated from the following equation:

$$V_{o(pp)} = \frac{V_{in(pp)} \times \frac{N_S}{N_P} \times \frac{D}{1-D}}{A_V} = \frac{20 \times \frac{3}{32} \times \frac{0.27}{1-0.27}}{80} = 8.7\text{mV}$$

The DC model for the error amplifier within the integrated circuit is shown in Figure 23. Figure 24, the error amplifier open-loop gain/phase response curve, shows that the amplifier is stable in the unity gain feedback configuration.

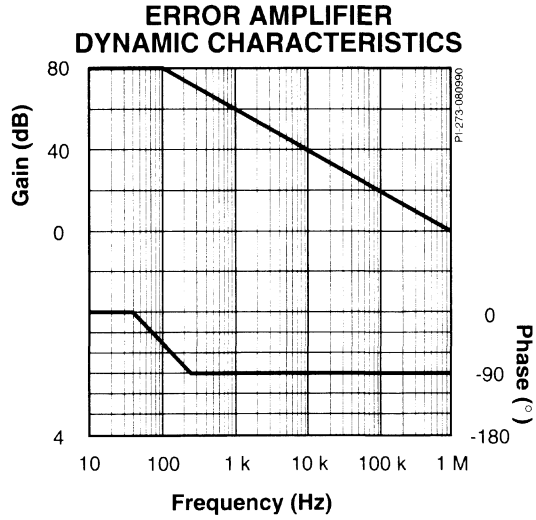


Figure 24.

Protection Features

Overtemperature

The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 135°C and keeps it off until the junction temperature decreases 45°C[13].

Input Overvoltage Protection

The voltage divider R1 and R2 sets the point where the input overvoltage comparator will inhibit the power supply output. The switching power transistor will be turned off when pin 6 exceeds 1.25 V. For the PWR-EVAL3, this translates to an input voltage of:

$$1.25 \times \frac{825.1}{5.1} = 202\text{V}$$

The switching power transistor will be turned back on when pin 6 drops below 1.2 V. For the PWR-EVAL3, this translates to an input voltage of:

$$1.2 \times \frac{825.1}{5.1} = 194\text{V}$$

Input Undervoltage Protection

The switching power transistor will be turned off when pin 6 drops below 0.34 volts. This translates to:

$$0.34 \times \frac{825.1}{5.1} = 55\text{V}$$

The switching power transistor will be turned back on when pin 6 exceeds 0.39 volts. This translates to:

$$0.39 \times \frac{825.1}{5.1} = 63\text{V}$$

Test Mode

The OV/UV control (pin 6) controls the built in test logic of the integrated circuit. The built-in test logic turns on the power transistor continuously when the voltage on pin 6 is equal to the pin 7 voltage (5.6 volts) +/- 1.5 V Do not put the circuit in test mode while operating in a power supply circuit as this could destroy the PWR-SMP120.

Control Circuit Undervoltage Protection

The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is typically 5 volts on pin 7.

Input Filtering and Rectification

BR1 and C1 perform the input rectification and filtering function. The rectifier diodes should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage rating on C1 is equal to the peak value of the maximum rectified input voltage, 200 V for 115 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitor, C1, can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage the power supply will provide a regulated output voltage at maximum power, and the minimum AC input voltage[14]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 when the input bridge diodes stop conducting, and V_2 is the voltage on C1 when the input bridge diodes start conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the input capacitor value.

Input Surge Current

When line voltage is applied to the power supply a surge of current flows in the input of the power supply to charge the input storage capacitor C1[15]. The magnitude of current must be within the surge ratings of the power switch, fuse and input rectifiers. The surge current is limited by the resistance of the EMI filter. L3, the differential mode filter inductor contributes the majority of the EMI filter resistance of 8 Ω. This limits the peak surge current to 160 V/8 Ω = 20 A.

EMI Considerations

This power supply was designed to meet worldwide EMI (FCC, part 15, subpart J) and safety (UL1950 and IEC950) specifications. Figure 25 is a plot of the conducted EMI relative to the FCC specification limits.

Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L3 and C6 filter differential mode conducted emissions.

Common Mode Filter
L2, L4, C7, C8, C12, and C17 filter common mode conducted emission currents[16]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C12 couples high-frequency noise back to the system chassis ground. C7, C8, and C17 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP120. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L4 in series with the ground lead of the power connector is a "lossy" bead and is equivalent to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

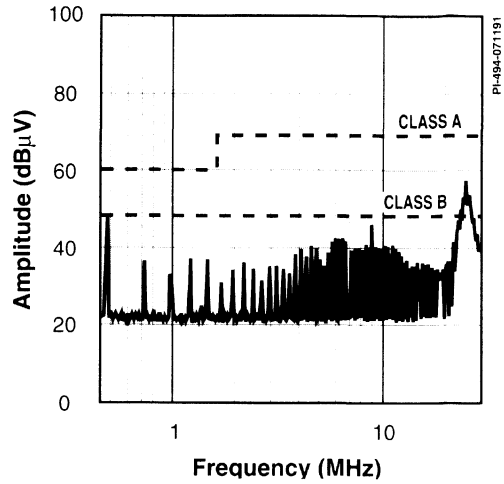


Figure 25. EMI Plot of the PWR-EVAL3.

Documentation Disks

The PWR-EVAL3 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL3 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README3.BAT	(This file) contains a summary and last minute information on the PWR-EVAL3
PWB1002B.APR	Aperture file with assigned D-codes
EVAL3.BOM	Bill of Materials file
EVAL3ASY.DWG	Assembly drawing file
FAB1002B.DWG	Fabrication drawing for the PC board
1002BCL.G23	Copper layers gerber file
1002BSM.G23	Solder mask layers gerber file
1002BSKP.G23	Padmaster gerber file
EVAL3.LIB	Library file of the parts used in the schematic
PWB1002B.NCD	NC drill file for computerized drilling of the PCB
EVAL3.SCH	Schematic file of PWR-EVAL3
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES3.TXT	Functional description of the power supply circuitry used in PWR-EVAL3
ICDESC3.TXT	Functional description of the PWR-SMP120 integrated circuit used in PWR-EVAL3
EVL3COST.TXT	Estimated parts cost
T1002 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD 286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README3.BAT and the EVAL3.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations on request.

3

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP120.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use or modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

References

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PWR-EVAL4

PWR-SMP400 Evaluation Board

48 VDC Input
Isolated 5 V, 5 W Output

POWER INTEGRATIONS, INC.

Product Highlights

Isolated 5 V Output from 48 VDC Input

- Up to 5 watts of output power can be supplied
- Isolation is provided by high frequency transformer
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits

- Input overvoltage shutdown
- Input undervoltage lockout
- Integrated current limit
- Thermal Shutdown

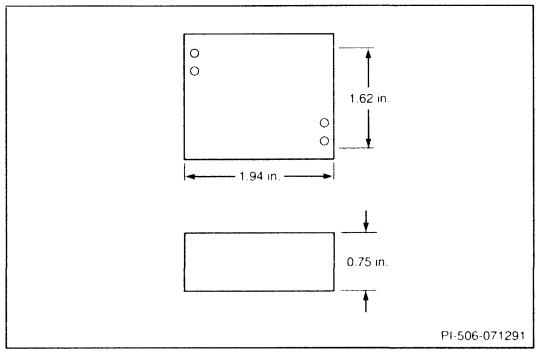


Figure 1. Evaluation Board Overall Physical Dimensions.

Description

The PWR-EVAL4 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP400BNC power supply IC.

The PWR-SMP400, intended for distributed power and telecommunications power supply applications, combines a high-voltage power MOSFET switch, a switchmode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP400 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP400 include PBX line cards, feature phones, LANs, modems, and distributed power systems in the commercial/industrial marketplace.

The PWR-EVAL4 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

PARAMETER	LIMITS
Input Voltage Range	30 to 72 VDC
Output Voltage Range	4.5 to 5.5 VDC
Load Current Range	0.6 to 1 A
Temperature Range	0 to 70°C
Efficiency	> 65%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	OPERATING VOLTAGE
PWR-EVAL4	48 VDC INPUT 5 VDC OUTPUT @ 5 W

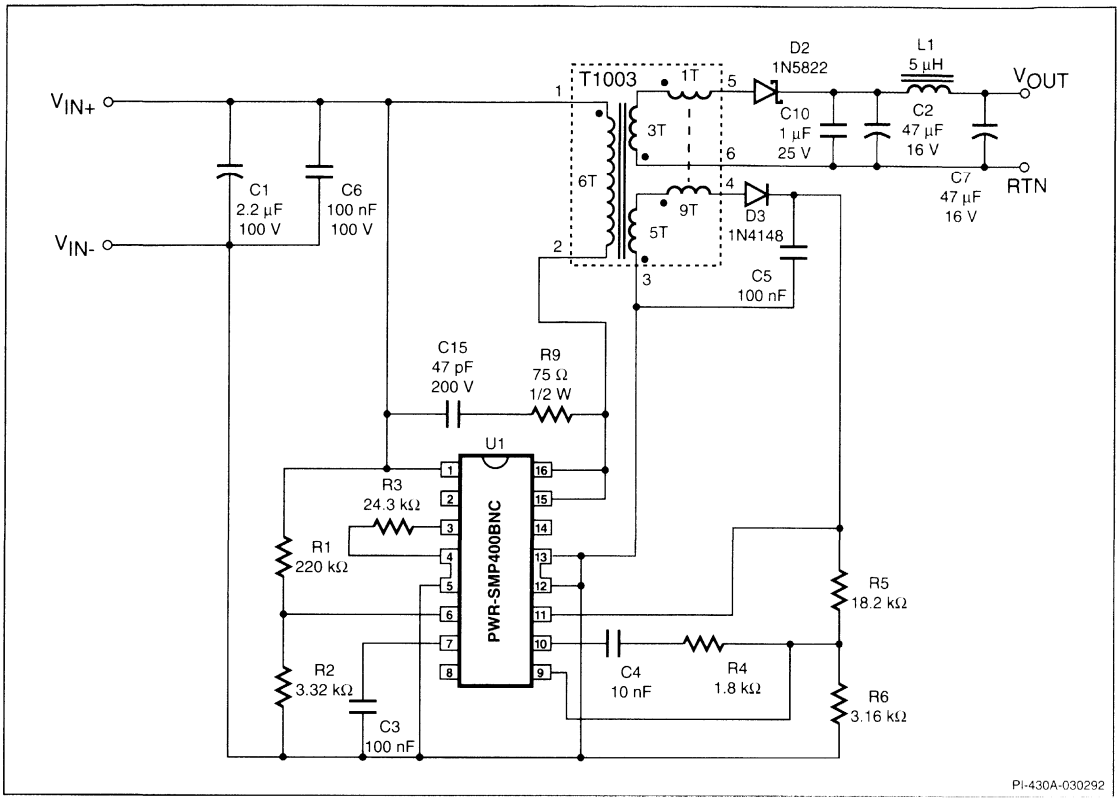


Figure 3. Schematic Diagram of the PWR-EVAL4 Power Supply.

General Circuit Description

The PWR-EVAL4 is an isolated Buck-Boost or flyback switching power supply topology[1]. The power supply is implemented using the PWR-SMP400BNC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1003 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 30 to 72 VDC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding of T1003. The PWR-SMP400 has been designed for a bias voltage (pin 11), of 8.5 volts. The effective transformer volts-per-turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. The three main elements that affect the regulation of the output voltage are; maintenance of a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

The circuit groups in the schematic Figure 3 are as follows. C1 and C6 form the EMI filter. The voltage divider formed by R1 and R2 set the input voltage that activates the input undervoltage and overvoltage shutdown functions. C15 and R9 damp the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, C14 and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP400. C3 and C5 are bypass capacitors.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	2.2 µF, 100 V	UVX2A2R2MAA	Nichicon (America)
C2, C7	47 µF, 16 V	16SA47M	Sanyo
C3, C5	100 nF, 50 V	K104Z20Z5UFVCWN	Mepco/Centralab
C4	10 nF, 50 V	K103M15X7RFVBWA	Mepco/Centralab
C6	100 nF, 100 V	K104Z20Z5UHVCWN	Mepco/Centralab
C10	1 µF, 25 V	TCD21E1E105	Marcon
C15	47 pF, 200 V	K470K15COGHVAWA	Mepco/Centralab
D2		IN5822	Motorola
D3		1N4148	Motorola
L1	5 µH, 1 A	CTX5-1-FR	Coiltronics
R1	220 kΩ, 1/4 W, 5%	5043CX220K0J	Mepco/Centralab
R2	3.32 kΩ, 1/4 W, 1%	5043ED3K32OF	Mepco/Centralab
R3	24.3 kΩ, 1/4 W, 1%	5043ED24K30F	Mepco/Centralab
R4	1.82 kΩ, 1/4 W, 5%	5043CXK1K80J	Mepco/Centralab
R5	18.2 kΩ, 1/4 W, 1%	5043ED18K20F	Mepco/Centralab
R6	3.16 kΩ, 1/4 W, 1%	5043ED3K160F	Mepco/Centralab
R9	75 Ω, 1/2 W, 5%	5053YL470R0J	Mepco/Centralab
U1		PWR-SMP400BNC	Power Integrations, Inc.
T1		T1003 *	Custom *
	PC Board	ASSY1003	Custom**

Custom Components:

* Qualified manufacturers are:

Datatronics	(714) 928-7731 FAX: (714) 928-7701
Inductor Supply	(714) 978-2277 FAX: (714) 978-2411
Renco Electronics	(800) 645-5828 FAX: (516) 586-5562
Tokin Magnetics	(415) 490-7500 FAX: (415) 490-7502

** Manufacturer is:

CBR
1116 Minnis Court
Milpitas, CA 95035
(408) 946-3446

Figure 4. Parts List for the PWR-EVAL4

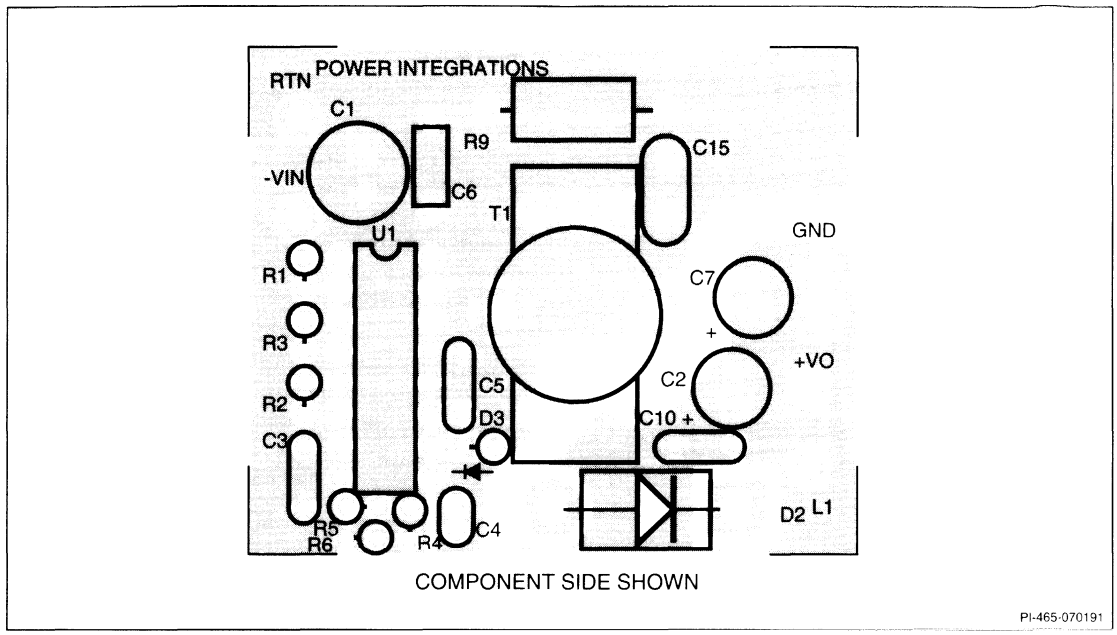


Figure 5. Component Legend of the PWR-EVAL4.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 was measured by applying a DC input voltage to the PWR-EVAL4.

Load Regulation (Figure 6) - The amount of output voltage change for a change in output current is referred to as load regulation. The output changes 5% for a 10% to 100% load current range. Below 10% of rated load the output voltage rises due to the leakage inductance of the transformer[2]. Non-ideal load regulation is caused by the resistance of the transformer output winding, the output rectifier series resistance, and the imperfect coupling between the output winding and the voltage feedback winding. The toroid pulse transformer improves the load regulation by minimizing the effect of the leakage inductance voltage spike on the feedback winding voltage.

The circuit in Figure 3 uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and setibility of ± 5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on the features and trade-offs of feedback winding regulation and optical feedback regulation.

Line Regulation (Figure 7) - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage is 1% for a input voltage change of 40 V(rms) or 250 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first cut transformer design procedure. Efficiency at full load and nominal line voltage is 70%.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typical output power capability with a nominal input voltage.

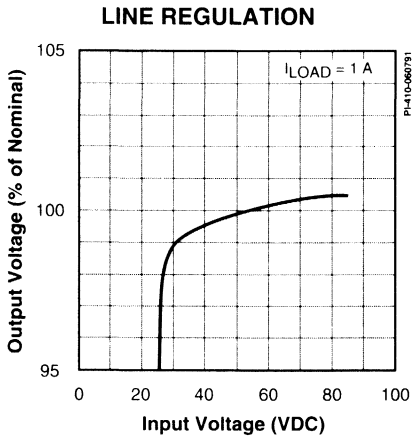


Figure 6.

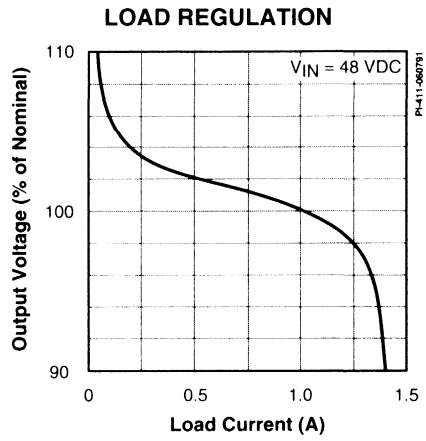


Figure 7.

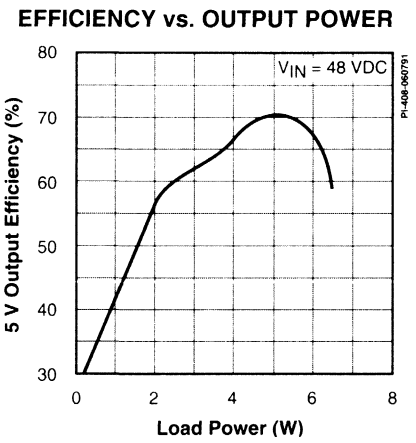


Figure 8.

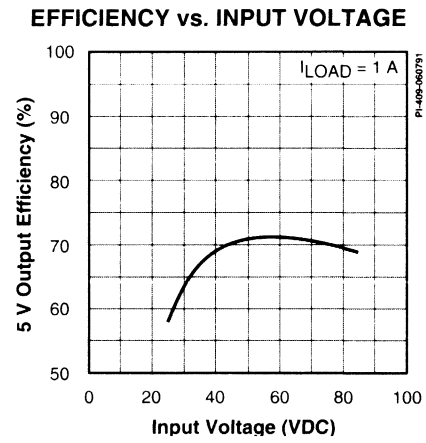


Figure 9.

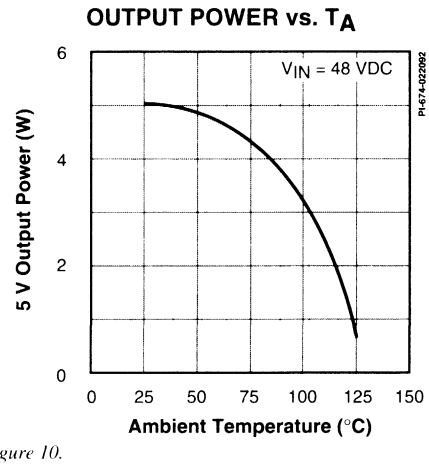


Figure 10.

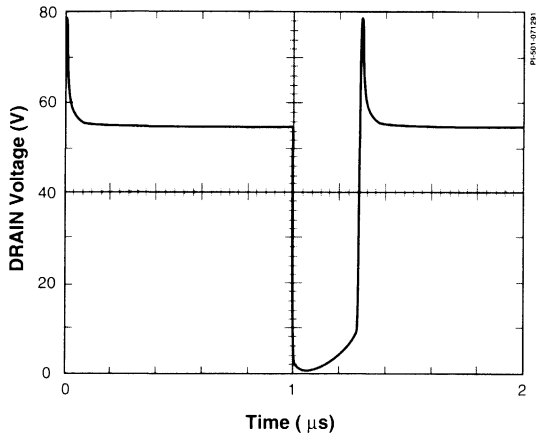


Figure 11. Drain-source Voltage of the PWR-SMP400.

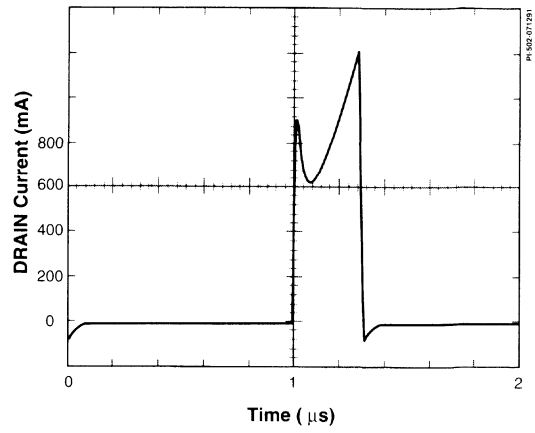


Figure 12. Drain Current of the PWR-SMP400.

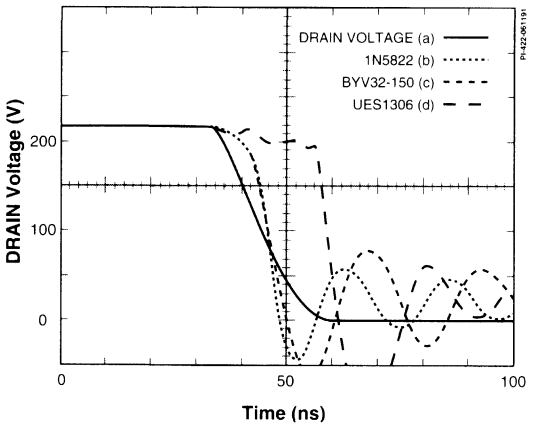


Figure 13. Recovery Times of Output Rectifier Diodes.

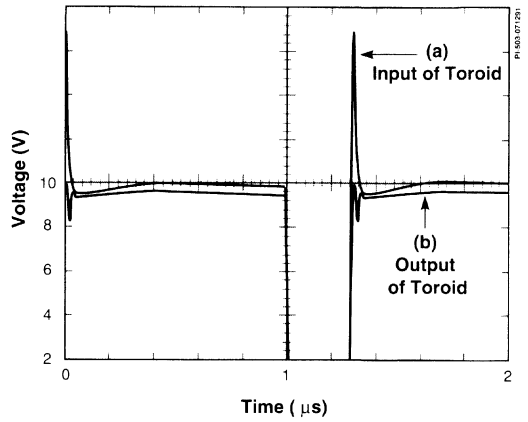


Figure 14. Pulse Transformer Winding Voltages.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a 1N5822 Schottky diode. Figure 13(c) is the anode of D2 when D2 is a BYV32-150 (150 V, 20 A, 35 ns) diode. Figure 13(d) is the anode of D2 when D2 is a UES1306 (400 V, 5 A, 50 ns) diode. The 1N5822 and BYV32-150 exhibit approximately 6 ns recovery times in the circuit, providing good functionality. However, the UES1306 exhibits a 22 ns recovery time in the circuit. This length of recovery time does not work well in the circuit.

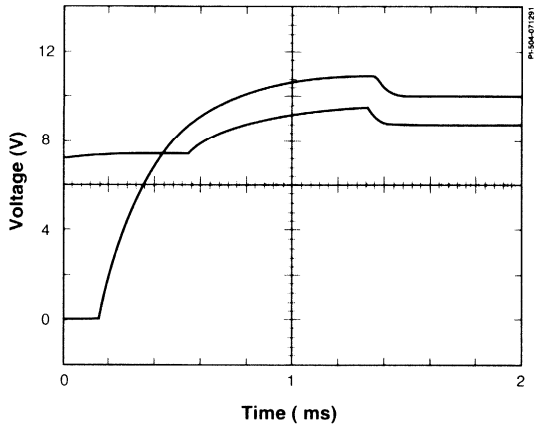


Figure 15. Bias Regulator-Feedback Supply Relationship.

The feedback bias supply winding voltage on each side of the pulse transformer winding is shown in Figures 14(a) and (b). This waveform is very important when load voltage regulation is being investigated. Waveform 14(a) is the voltage on the power transformer side of the pulse transformer. Waveform 14(b) is the voltage on the rectifier side of the pulse transformer. Notice how the pulse transformer has cancelled the leakage inductance spike voltage present on the feedback winding of the power transformer.

Power Supply Turn On Sequence

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. This regulator maintains the voltage on pin 11 at approximately 7.5 V. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the feedback winding and filter provides bias current and turns off the pre-regulator when the power supply is operating. The bias supply voltage at turn-on is shown in Figure 15. It is important to notice how closely the output voltage is coupled to the feedback bias supply. The amount of voltage overshoot is a function of the control loop compensation. If the control loop is made slower by modifying R4 and C4, the overshoot will increase.

The 5.6 volt V_S voltage on pin 7 is derived from pin 11 with a second linear regulator. An external bypass capacitor on the V_S pin provides a path for the gate drive switching noise currents to flow.

Output Voltage

The output voltage is controlled by the transformer turns ratio. The PWR-SMP400BNC control circuit will regulate the rectified V_{BIAS} feedback voltage (pin 11) to a typical value of 8.45 V. The output voltage can be estimated by multiplying the output-to-feedback turns ratio by the feedback voltage. A precise method of determining the output voltage would take into account the specific rectifier voltage drop, the resistance of the output winding of the transformer, and the equivalent series resistance of the output capacitor.

The output voltage can be adjusted using the transformer turns ratio. The output voltage can be coarsely tuned by increasing the number of junction voltage drops for D3 and fine tuned with the voltage divider R5 and R6. The R5-R6 voltage divider ratio can be adjusted with a voltage trim resistor (R8).

A higher precision of output voltage regulation can be achieved by sensing and regulating the output voltage directly. This can be accomplished by the use of a secondary side referenced error amplifier and optical coupler circuit as described in AN-8.

Note that V_{BIAS} (pin 11) must be between 8.25 V and 9 V to cut off the high-voltage pre-regulator within U1. Additional information on transformer design is available in AN-7.

3

Output Transformer T1003

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies.

The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Toroid Pulse Transformer

The pulse transformer is part of the standard transformer T1003. The transformer generates a voltage pulse on its primary from the rate of change of current in the output rectifier[4]. This voltage pulse is scaled and placed in series with the feedback winding.

The voltage on the output of the pulse transformer is equal, in phase and proportional to the leakage inductance voltage spike. The peak output voltage of the series connection of the feedback winding and the pulse transformer secondary is proportional to the output voltage and is not influenced by the leakage inductance voltage spike. The cancellation effect of the pulse transformer can be seen in Figure 14.

Magnetics Design

The standard transformer has a primary winding with 6 turns of 30 AWG magnet wire, a feedback winding of 5 turns of 35 AWG magnet wire and an output winding of 3 turns of 300 V rated insulated 24 AWG wire. The insulation on the secondary wire meets the voltage breakdown and safety requirements of Underwriters Laboratories.

The pulse transformer has a one turn primary and 9 turns of 35 AWG magnet wire secondary.

The nominal primary inductance is 14.5 µH. The maximum leakage inductance measured on the primary is 4 µH. Approximately 80% of the leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 5 MHz.

The resistance of the primary winding is 0.12 Ω. The resistance of the secondary winding is 0.036 Ω. The resistance of the feedback winding is 0.34 Ω.

The core is a 14 mm x 8 mm pot core. The core material is Magnetics Inc "P" material. The AL value is 400 nH/T^2. The pulse transformer core is Philips 104IT060-4C4.

The power transformer AC flux density at 5 watts and 750 kHz is 635 gauss.

The primary saturation current at 100°C, 2500 gauss, is 2.6 ampere.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{25 \times 0.35}{2 \times 7.5 \times 10^5 \times (0.9 - 0.75)} = 39\mu H$$

where the peak switch current is between the typical current with V_{DS} of 10 V and the minimum current limit current. The primary inductance calculations for the PWR-SMP400 with 5 watts output show an inductance of 39 µH. The efficiency of the PWR-SMP400 at 5 watts and 30 VDC is 63%. The input power will be 7.9 W (5 W divided by 0.63). The average input current at 30 VDC will be 0.263 A (7.9 W divided by 30 V). The average on time current with a 35% duty cycle is 0.75 A (0.263 A divided by 0.35). The primary inductance L_p equals 39 µH. The nominal primary inductance of the T1003 is 14.5 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum

duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds / turn = 0).

$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.35}{(1 - 0.35)} \times \frac{30 - 5}{5 + 0.5} = 2.4$$

Single Output Voltage

The standard transformer design can be modified for voltages other than 5 volts. This is achieved by changing the secondary winding to feedback winding turns ratio. The output voltage can be fine tuned by adjusting the R5, R6 voltage divider. However, the voltage on pin 11 of the PWR-SMP400BNC must be within the voltage range specified in the data sheet.

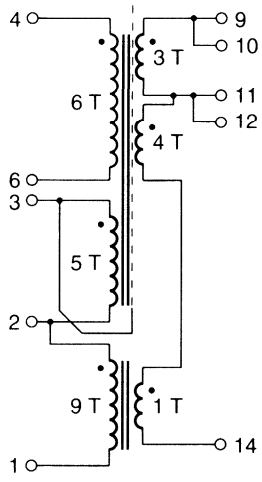
If the turns count on the secondary is greater than three, a larger core will be required to accommodate the larger number of insulated turns on the bobbin.

The output voltage can be increased to 12 volts by increasing the secondary to 7 turns. The transformer will generate 1.8 volts/turn less a 0.6 volt diode drop yields 12 volts.

The output voltage can be increased to 15 volts by increasing the secondary to 8 turns and increasing the number of junctions in D3 to two. The two junctions for D3 increases the output to 1.96 volts/turn. A 0.6 volt diode drop will yield a 15 volt output.

Multiple Output Voltages

The number of output voltages can be increased by adding additional output turns and voltage taps. A 5 volt and 12 volt output can be achieved with a 7 turn winding with a tap at 3 turns as shown in Figure 16. Figure 17 shows how a 5 volt and 15 volt output can be achieved with a 6 turn winding and a 3 turn winding. This scheme creates two separate supplies, 5 V and 10.5 V, and connects them in series.



CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	+5 V OUTPUT
14	+12 V OUTPUT

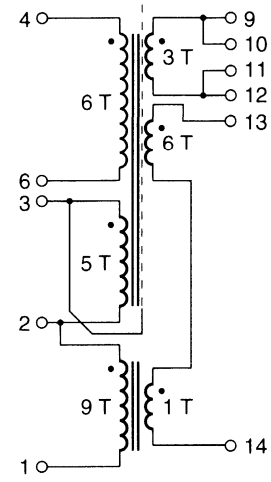
PI-507-071291

Figure 16. 5/12 V Transformer Schematic Diagram.

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by R9 and the voltage on C15, the primary damping network.

C15 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C15 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1.



CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	N/C
13	+5 V OUTPUT
14	+15 V OUTPUT

PI-508-071291

Figure 17. 5/15 V Transformer Schematic Diagram.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package, the ambient temperature[5], and the peak switching transistor current limit circuit. The available output power as a function of input voltage for an 80°C temperature rise (junction to ambient) is shown in Figure 18.

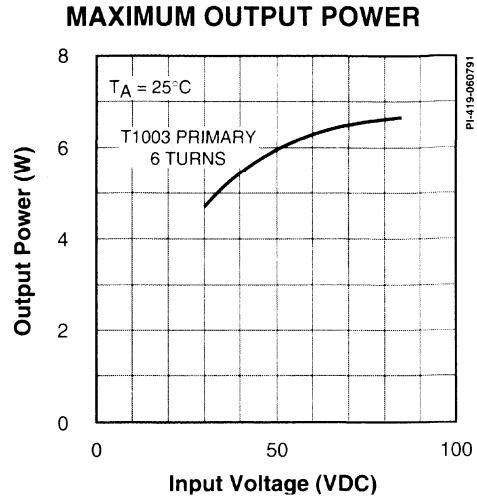


Figure 18.

Thermal Characteristics

The PWR-SMP400BNC is packaged in a 16-pin plastic power DIP package[6]. This package offers a lower thermal impedance as compared to a standard plastic DIP package. The thermal impedance from junction to ambient and from junction to case are 43°C/Watt and 6°C/Watt respectively. Soldered connections to the heat spreading "wings" (pins 4, 5, 12, and 13) provide a good thermal path while the DIP form factor maintains compatibility with automatic insertion equipment for low cost assembly. The thermal impedance from case to local ambient on a typical power supply board is 43-6 = 37°C/W. The local ambient temperature can be 10°C above ambient due to heating from other components on the printed circuit board.

The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and the transformer and damping network capacitances[7], and the losses in the pre-regulator when it is active. Figure 19 is the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 20. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this figure to determine the total AC losses in the circuit.

Additional information on thermal management is available in AN-9.

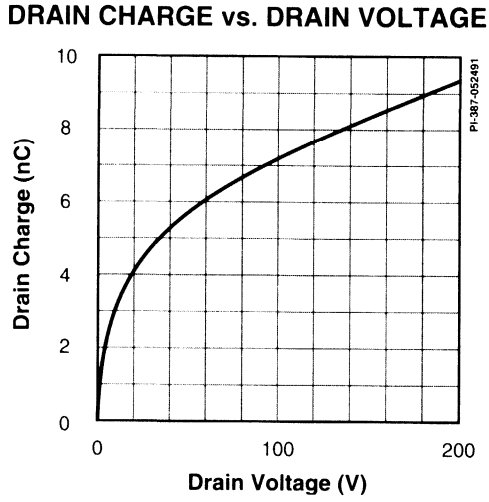


Figure 19.

Current Limit

The current limit circuit is internal to the PWR-SMP400BNC and is a peak detection type of circuit. The circuit monitors the current flowing in the switching transistor. When the current exceeds the typical value of 1.1 A for 100 ns the switching transistor is turned off for the rest of the oscillator cycle. The effect on the output voltage can be seen in Figure 21. The shape of the current limit function is very close to a constant power curve[8]. This is because the circuit regulates the peak current in the transformer primary providing a constant energy delivery to the core during current limit, thus a constant power output in current limit.

Current limit is implemented within the integrated circuit by applying a current sense signal to a comparator input. The comparator triggers a latch which turns the power transistor off until the next clock cycle.

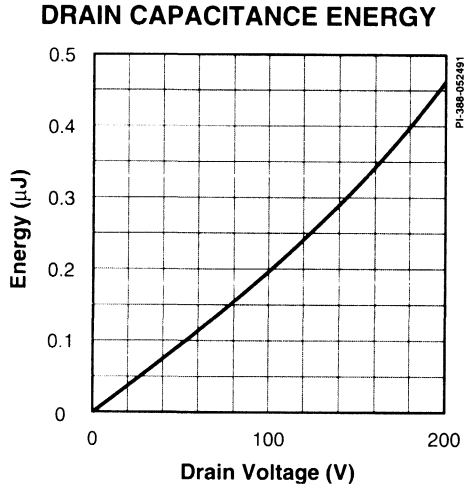


Figure 20.

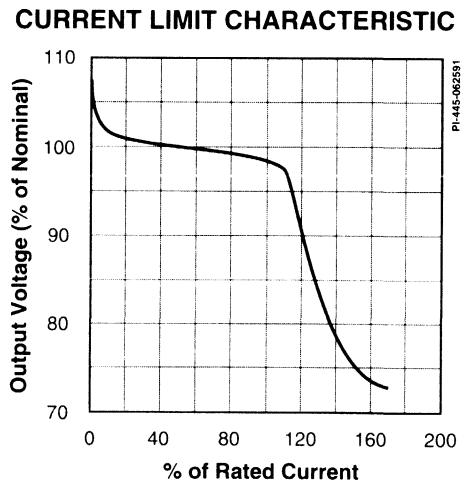


Figure 21.

3

Operating Frequency

The operating frequency of the PWR-EVAL4 is typically 750 kHz. A timing capacitor of 25 pF for the oscillator is internal to the PWR-SMP400BNC. The frequency of operation is adjustable, pin 8 of U1. An approximate formula for nominal operating frequency is:

$$f = \frac{\frac{67.4\mu A}{2.2V}}{25pF + C_{EXT}}$$

Voltage Control Loop

The PWR-SMP400BNC has a voltage-mode control circuit[9]. The DC input to output voltage transfer function when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[10]. The duty cycle is controlled by the output voltage error amplifier. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[11,12] is included in the documentation disk. T1, U1, R4, R5, C2, C4 and C14 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The model for the operating point duty cycle transformation uses a transconductance generator and a voltage gain stage. The coefficients of the small signal pulse width modulator transfer-function generators are calculated by knowing the primary reflex voltage (output voltage plus rectifier forward drop times the transformer turns ratio), the duty cycle of the operating point of interest and the load resistance transformed to the primary of the transformer:

$$R = R_O \times \left(\frac{N_P}{N_S}\right)^2 = 5 \times \left(\frac{6}{3}\right)^2 = 20\Omega$$

The voltage generator gain:

$$E = \frac{-V}{D^2} = \frac{-11}{(0.269)^2} = -153$$

The current generator gain:

$$J = \frac{-V}{(1-D)^2 \times R} = \frac{-11}{(1-0.269)^2 \times 20} = -1.03$$

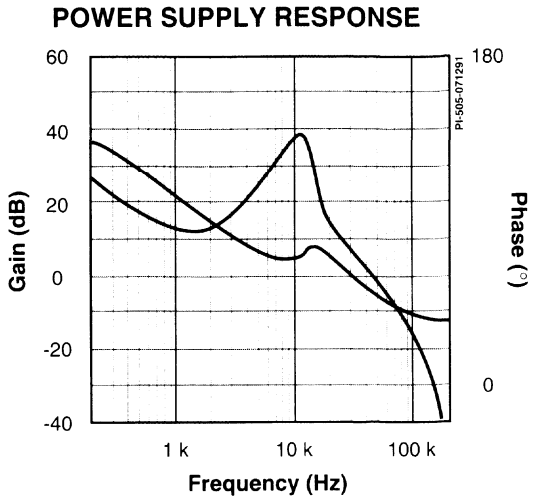


Figure 22.

The current generator is to provide the negative input impedance effect of a switching regulator and can be neglected if the resonant frequency of the EMI filter is much higher than the control loop frequencies of interest.

The measured power supply open loop gain/phase response curve is shown in Figure 22. The control loop has 72 degrees phase margin, an open loop unity gain crossover frequency of 17 kHz and 19 dB gain margin at 170 kHz with a 5 watt load.

The DC model for the error amplifier within the integrated circuit is shown in Figure 23. Figure 24, the error amplifier open-loop gain/phase response curve, shows that the amplifier is stable in the unity gain feedback configuration.

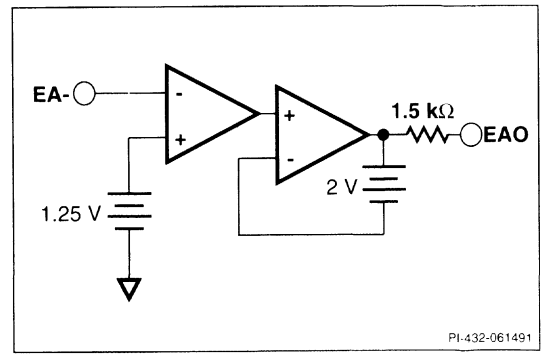


Figure 23. Error Amplifier Equivalent Circuit.

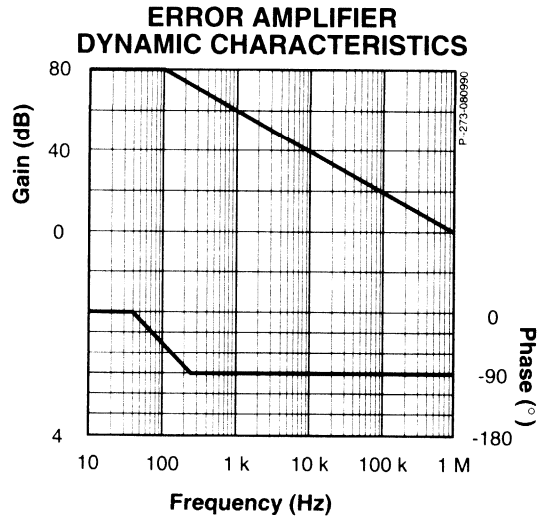


Figure 24.

Protection Features

Overtemperature

The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 135°C and keeps it off until the junction temperature decreases 45°C[13].

Input Overvoltage Protection

The voltage divider R1 and R2 sets the point where the input overvoltage comparator will inhibit the power supply output. The switching power transistor will be turned off when pin 6 exceeds 1.25 V. For the PWR-EVAL4, this translates to an input voltage of:

$$1.25 \times \frac{223.32}{3.32} = 84\text{V}$$

The switching power transistor will be turned back on when pin 6 drops below 1.2 V. For the PWR-EVAL4, this translates to an input voltage of:

$$1.2 \times \frac{223.32}{3.32} = 80.7\text{V}$$

Input Undervoltage Protection

The switching power transistor will be turned off when pin 6 drops below 0.34 volts. This translates to:

$$0.34 \times \frac{223.32}{3.32} = 22.9\text{V}$$

The switching power transistor will be turned back on when pin 6 exceeds 0.39 volts. This translates to:

$$0.39 \times \frac{223.31}{3.32} = 26.2\text{V}$$

Test Mode

The OV/UV control (pin 6) controls the built in test logic of the integrated circuit. The built-in test logic turns on the power transistor continuously when the voltage on pin 6 is equal to the pin 7 voltage (5.6 volts) +/- 1.5 V Do not put the circuit in test mode while operating in a power supply circuit as this could destroy the PWR-SMP400.

Control Circuit Undervoltage Protection

The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is typically 5 volts on pin 7.

Documentation Disks

The PWR-EVAL4 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL4 design. Both disks high density MS-DOS format. Each of these disks contain the following files:

README4.BAT	(This file) contains a summary and last minute information on PWR-EVAL4
PWB1001B.APR	Aperture file with assigned D-codes
EVAL4.BOM	Bill of Materials file
EVAL4ASY.DWG	Assembly drawing file
FAB1003B.DWG	Fabrication drawing for the PC board
1003B.G23	Gerber file of all layers
EVAL4.LIB	Library file of the part symbols used in both schematics
PWB1003B.NCD	NC drill file for computerized drilling of the PCB
EVAL4.SCH	Schematic file of PWR-EVAL4
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES4.TXT	Functional description of the power supply circuitry used in PWR-EVAL4
ICDESC4.TXT	Functional description of the PWR-SMP400 integrated circuit used in PWR-EVAL4
EVL4COST.TXT	Estimated parts cost
T1003 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README4.BAT and the EVAL4.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations on request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP400.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

References

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7 Keller, R., Leman, B. "New Integrated Technology Combines 800 V High-Speed Power MOSFET Switch with Pulse Width Modulation Control Circuitry for Power System Applications" Proceedings, High Frequency Power Conversion International June 1991, p. 61

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12 Keller, Richard, "The Off-Line Converter as a Closed Loop System: Loop Design, Measurement and Analysis" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, A2.1-A2.9

13 Thermal Shutdown Application notes: National Semiconductor AN-82, AN-103

14 Tartar, Ralph E., Principles of Solid-state Power Conversion Howard W. Sams & Co., Inc., 1985, p. 232

15 Hirshberg, Walter "Optimizing Line Inrush Design in Off-Line Converters" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, E3.1-E3.7

16 Nave, Mark J. "Measuring, Suppressing, and Filtering Common Mode Emissions in Switch-Mode Power Supplies" HFPC 89 Proceedings, May 1989, pp. 285-293

PWR-EVAL5

PWR-SMP210 Evaluation Board

110/220 VAC Input
Isolated 5 V, 5/10 W Output

POWER INTEGRATIONS, INC.®

Product Highlights

Isolated 5 V Output from 110/220 VAC Input
- Up to 10 watts of output power can be supplied
- Isolation is provided by transformer designed to UL/VDE specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits
- Input overvoltage shutdown
- Input undervoltage lockout
- External current limit
- Thermal Shutdown

Designed to Meet Regulatory Standards
- Layout designed to meet UL/CSA/VDE requirements
- Meets DIN VDE 0805/05.90 Level B, RPM

Description

The PWR-EVAL5 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP210BNC power supply IC.

The PWR-SMP210, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a switchmode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP210 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP210 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL5 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

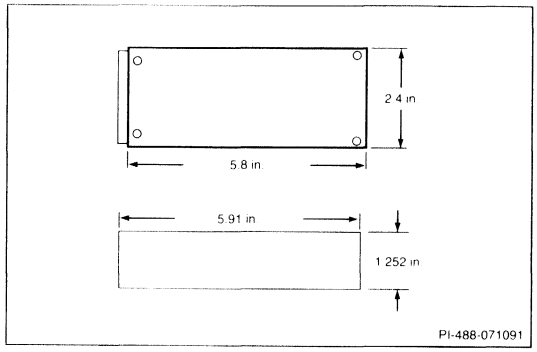


Figure 1. Evaluation Board Overall Physical Dimensions.

PARAMETER	LIMITS
Input Voltage Range	85 to 265 VAC
Input Frequency Range	47 to 440 Hz
Output Voltage Range	4.5 to 5.5 VDC
Load Current Range	0.06 to 1 A
Temperature Range	0 to 70°C
Efficiency	> 76%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	**OPERATING VOLTAGE**
PWR-EVAL5	220 VAC INPUT 5 VDC OUTPUT @ 10 W
	110/220 VAC INPUT 5 VDC OUTPUT @ 5 W

3

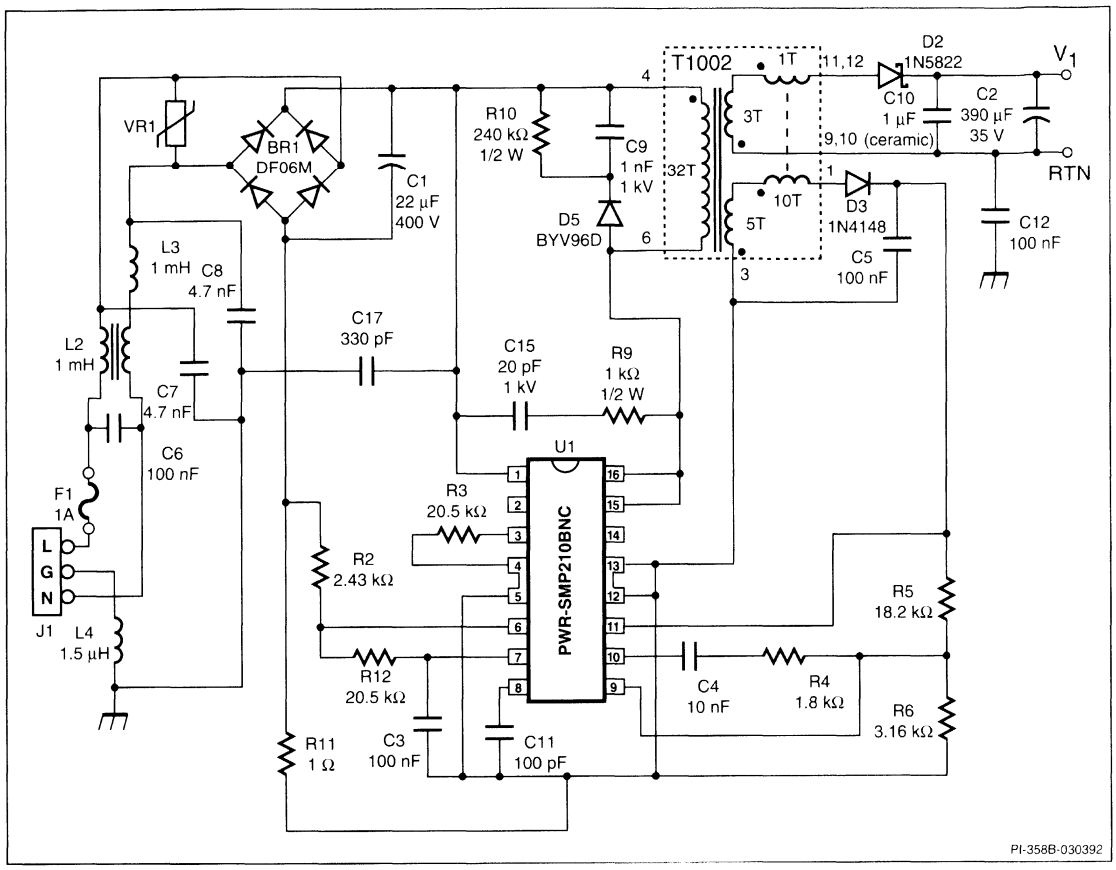


Figure 3. Schematic Diagram of the PWR-EVAL5 Power Supply.

General Circuit Description

The PWR-EVAL5 is an isolated Buck-Boost or flyback switching power supply topology[1]. The power supply is implemented using the PWR-SMP210BNC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1002 standard transformer (see DA-3), will produce a 5 volt, 5 watt power supply that will operate from 85 to 265 VAC input voltage. The output voltage is selected by the turns ratio of the output winding to the feedback winding of T1002. The PWR-SMP210 has been designed for a bias voltage (pin 11), of 8.5 volts. The effective transformer volts-per-turn can be fine tuned if necessary by the number of junctions in D3. The diode D2 should be a Schottky rectifier to reduce diode switching losses. The three main elements that affect the regulation of the output voltage are; maintenance of a constant feedback winding voltage, tight coupling of the power transformer, and the use of a pulse transformer to cancel the leakage inductance voltage spike.

The circuit groups in the schematic Figure 3 are as follows. L2, L3, L4, C6, C7, C8, C12, and C17 form the EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. D5, C9 and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the leakage inductance ringing voltage. The damping network improves the regulation of the output voltage. R5 and R6 set the feedback voltage to 8.5 volts. R4, R5, C2, C4, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP210. C3 and C5 are bypass capacitors. R2, R11, and R12 set the primary current limit threshold.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	22 µF, 400 V	UVX2G220MHA	Nichicon (America)
C2	390 µF, 35 V	UPL1V391MPH6	Nichicon (America)
C3, C5, C12	100 nF, 50 V	K104Z20Z5UFVBWN	Mepco/Centralab
C4	10 nF, 50 V	K103M15X7RFVBWA	Mepco/Centralab
C6	100 nF-S, 250 VAC	QXW2E104KTPT	Nichicon (America)
C7, C8	4.7 nF-S, 250 VAC	440LD47	Cera-Mite (Sprague)
C9	1 nF, 1 kV	D102P29Z5UNAAEM	Mepco/Centralab
C10	1 µF, 25 V	TCD21E1E105	Marcon
C11	100 pF, 50 V	K101J15COGFVBWA	Mepco/Centralab
C15	20 pF, 1 kV	5GAQ20	Cera-Mite (Sprague)
C17	330 pF-S, 250 VAC	440LD47	Cera-Mite (Sprague)
BR1	1 A, 600 V	DF06M	General Instrument
D2		1N5822	Motorola
D3		1N4148	Motorola
D5		BYV96D	General Instrument
F1	1 A, 250 VAC	230.001	Littlefuse/Tracor
L2	1 mH	SC-01-10G	Tokin
L3	1000 µH	RL1160-1000	Renco
L4	1.5 µH	2673200201	Fair-Rite Products
R2	2.43 kΩ, 1/4 W, 1%	5043ED2K430F	Mepco/Centralab
R3, R12	20.5 kΩ, 1/4 W, 1%	5043ED20K50F	Mepco/Centralab
R4	1.8 kΩ, 1/4 W, 5%	5043CXK1K80J	Mepco/Centralab
R5	18.2 kΩ, 1/4 W, 1%	5043ED18K20F	Mepco/Centralab
R6	3.16 kΩ, 1/4 W, 1%	5043ED3K160F	Mepco/Centralab
R9	1 kΩ, 1 W, 5%	5073YL1K00J	Mepco/Centralab
R10	240 kΩ, 1/2 W, 5%	5053CX240KJ	Mepco/Centralab
R11	1 Ω, 1/4 W, 2%	5043ED1R000G	Mepco/Centralab
U1		PWR-SMP210BNC	Power Integrations, Inc.
VR1	275 VAC	V275LA1	General Electric
T1		T1002	Custom*
J1	Plug Socket	C6480	USD Products/Cooper
	PC Board	ASSY 1002-B	Custom**

Custom Components:

* Qualified manufacturers are:

AT&T Microelectronics	(800) 372-2447	FAX: (214) 284-8282
Datatronics	(714) 928-7731	FAX: (714) 928-7701
Delta (Taiwan)	(02) 7164822	FAX: (02) 7169764
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin (Japan)	(03) 402-6166	FAX: (03) 497-9756

** Manufacturer is:

CBR Circuits
116 Minnis Court
Milpitas, CA 95035
(408) 946-3446

Figure 4. Parts List for the PWR-EVAL5

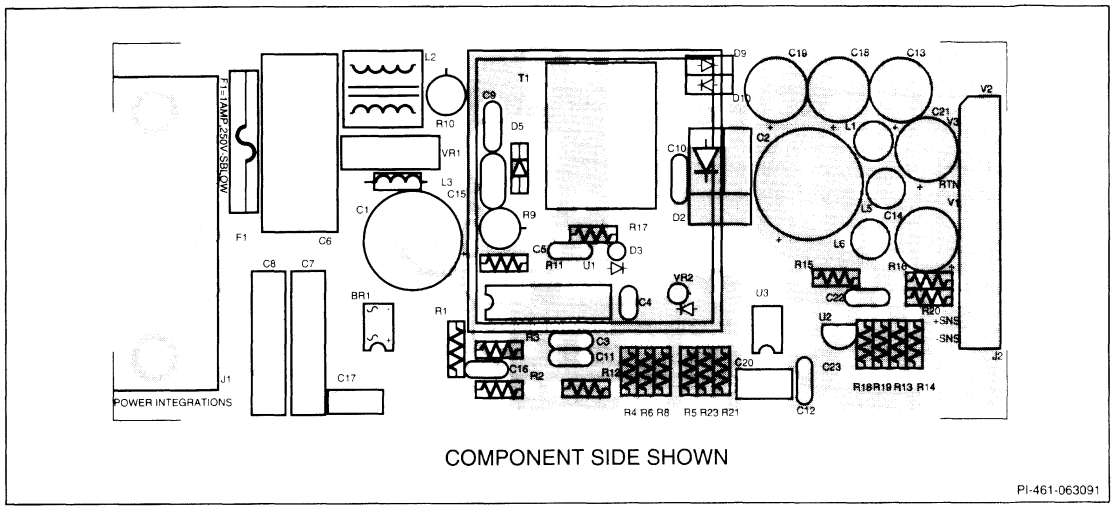


Figure 5. Component Legend of the PWR-EVAL5.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 was measured by applying a DC input voltage to the PWR-EVAL5.

Load Regulation (Figure 6) - The amount of output voltage change for a change in output current is referred to as load regulation. The output changes 5% for a 10% to 100% load current range. Below 10% of rated load the output voltage rises due to the leakage inductance of the transformer[2]. Non-ideal load regulation is caused by the resistance of the transformer output winding, the output rectifier series resistance, and the imperfect coupling between the output winding and the voltage feedback winding. The toroid pulse transformer improves the load regulation by minimizing the effect of the leakage inductance voltage spike on the feedback winding voltage.

The circuit in Figure 3 uses a secondary winding to monitor and regulate the output voltage. This technique can provide regulation and setibility of ± 5%. If tighter regulation is required for a given application, an optical feedback technique can be used. See AN-8 for further information on the features and trade-offs of feedback winding regulation and optical feedback regulation.

Line Regulation (Figure 7) - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage is 0.5% for a input voltage change of 100 V(rms) or 50 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first cut transformer design procedure. Efficiency at full load and nominal line voltage is 76%.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typical output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[3].

$$PF = \frac{P_{in}}{V_{in} \times I_{in}}$$

The power factor of the PWR-EVAL5 with a 5 W load is approximately 0.6.

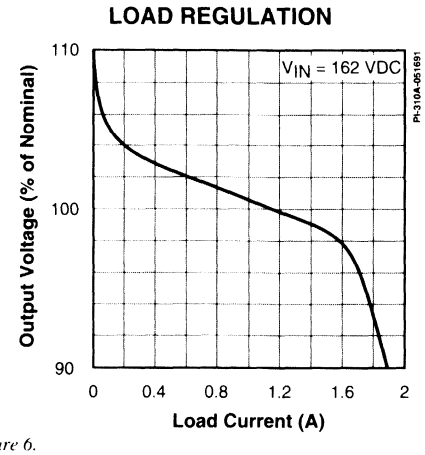


Figure 6.

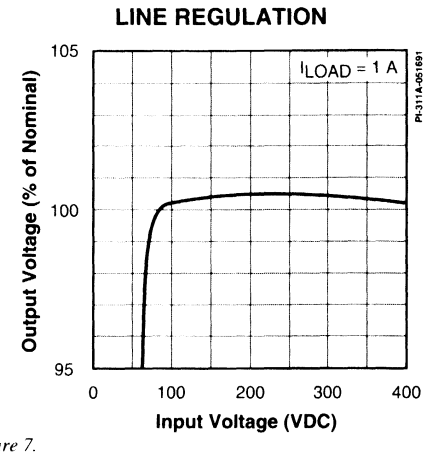


Figure 7.

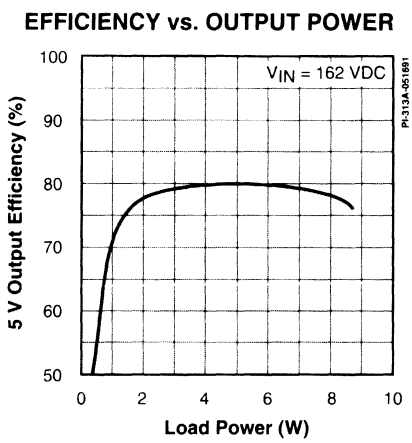


Figure 8.

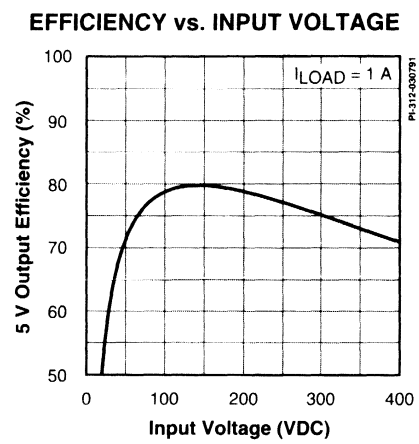


Figure 9.

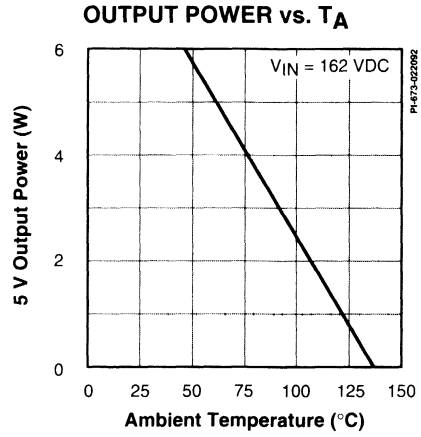


Figure 10.

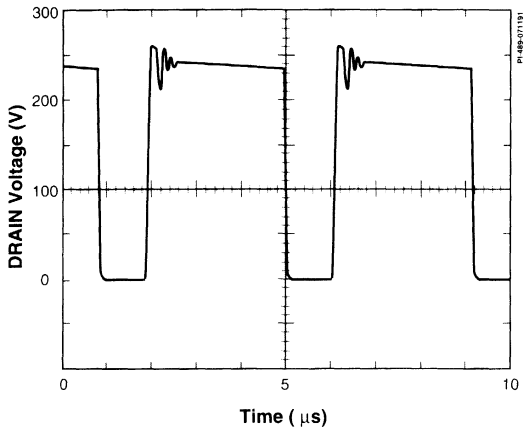


Figure 11. Drain-source Voltage of the PWR-SMP210.

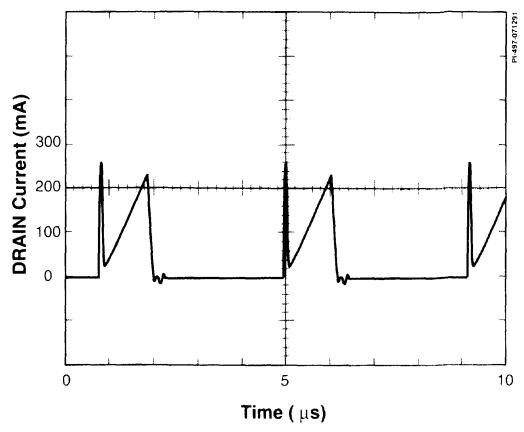


Figure 12. Drain Current of the PWR-SMP210.

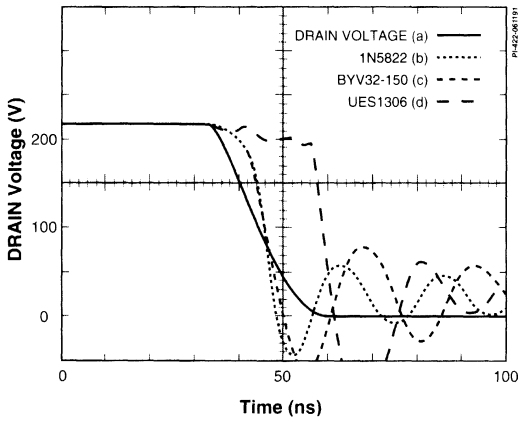


Figure 13. Recovery Times of Output Rectifier Diodes.

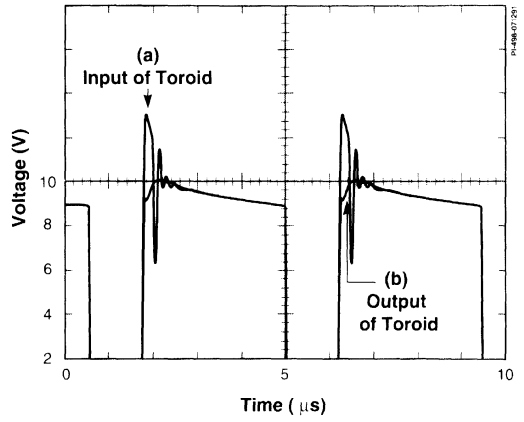


Figure 14. Pulse Transformer Winding Voltages.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a 1N5822 Schottky diode. Figure 13(c) is the anode of D2 when D2 is a BYV32-150 (150 V, 20 A, 35 ns) diode. Figure 13(d) is the anode of D2 when D2 is a UES1306 (400 V, 5 A, 50 ns) diode. The 1N5822 and BYV32-150 exhibit approximately 6 ns recovery times in the circuit, providing good functionality. However, the UES1306 exhibits a 22 ns recovery time in the circuit. This length of recovery time does not work well in the circuit.

The feedback bias supply winding voltage on each side of the pulse transformer winding is shown in Figures 14(a) and (b). This waveform is very important when load voltage regulation is being investigated. Waveform 14(a) is the voltage on the

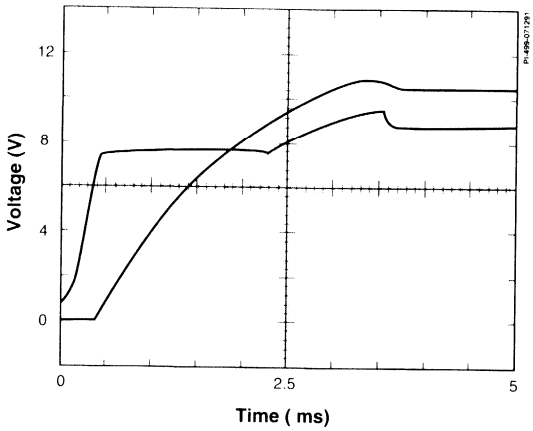


Figure 15. Bias Regulator-Feedback Supply Relationship.

power transformer side of the pulse transformer. Waveform 14(b) is the voltage on the rectifier side of the pulse transformer. Notice how the pulse transformer has cancelled the leakage inductance spike voltage present on the feedback winding of the power transformer.

Power Supply Turn On Sequence

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. This regulator maintains the voltage on pin 11 at approximately 7.5 V. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the feedback winding and filter provides bias current and turns off the pre-regulator when the power supply is operating. The bias supply voltage at turn-on is shown in Figure 15. It is important to notice how closely the output voltage is coupled to the feedback bias supply. The amount of voltage overshoot is a function of the control loop compensation. If the control loop is made slower by modifying R4 and C4, the overshoot will increase.

The 5.6 volt V_S voltage on pin 7 is derived from pin 11 with a second linear regulator. An external bypass capacitor on the V_S pin provides a path for the gate drive switching noise currents to flow.

Output Voltage

The output voltage is controlled by the transformer turns ratio. The PWR-SMP210BNC control circuit will regulate the rectified V_{BIAS} feedback voltage (pin 11) to a typical value of 8.45 V. The output voltage can be estimated by multiplying the output-to-feedback turns ratio by the feedback voltage. A precise method of determining the output voltage would take into account the specific rectifier voltage drop, the resistance of the output winding of the transformer, and the equivalent series resistance of the output capacitor.

The output voltage can be adjusted using the transformer turns ratio. The output voltage can be coarsely tuned by increasing the number of junction voltage drops for D3 and fine tuned with the voltage divider R5 and R6. The R5-R6 voltage divider ratio can be adjusted with a voltage trim resistor (R8).

A higher precision of output voltage regulation can be achieved by sensing and regulating the output voltage directly. This can be accomplished by the use of a secondary side referenced error amplifier and optical coupler circuit as described in AN-8.

Note that V_{BIAS} (pin 11) must be between 8.25 V and 9 V to cut off the high-voltage pre-regulator within U1. Additional information on transformer design is available in AN-7.

Output Transformer T1002

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies. The T1002 is being submitted to TUV Rheinland for safety review in 220 VAC applications.

The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Toroid Pulse Transformer

The pulse transformer is part of the standard transformer T1002. The transformer generates a voltage pulse on its primary from the rate of change of current in the output rectifier[4]. This voltage pulse is scaled and placed in series with the feedback winding.

Output Transformer T1002 (cont.)

The voltage on the output of the pulse transformer is equal, in phase and proportional to the leakage inductance voltage spike. The peak output voltage of the series connection of the feedback winding and the pulse transformer secondary is proportional to the output voltage and is not influenced by the leakage inductance voltage spike. The cancellation effect of the pulse transformer can be seen in Figure 14.

Magnetics Design

The standard transformer has a primary winding with 32 turns of 30 AWG magnet wire, a feedback winding of 5 turns of 35 AWG magnet wire and an output winding of 3 turns with two wires bifilar wound of 300 V rated insulated 24 AWG wire. The insulation on the secondary wire meets the voltage breakdown and safety requirements of Underwriters Laboratories.

The pulse transformer has a one turn primary and 10 turns of 35 AWG magnet wire secondary.

The nominal primary inductance is 738 µH. The maximum leakage inductance measured on the primary is 18 µH. Approximately 80% of the leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 1 MHz.

The resistance of the primary winding is 0.54 Ω. The resistance of the secondary winding is 0.005 Ω. The resistance of the feedback winding is 0.37Ω.

The core is a PQ 2016 style core. The core material is Magnetics Inc "P" material. The AL value is 721 nH/T^2. The pulse transformer core is Micrometals T30-8/90 powdered iron toroid.

The power transformer AC flux density at 5 watts and 250 kHz is 773 gauss.

The primary saturation current at 100°C, 3800 gauss, is 1.02 ampere.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.48}{2 \times 2.5 \times 10^5 \times (0.35 - 0.137)} = 428\mu H$$

where the peak switch current is between the typical current with V_{DS} of 10 V and the minimum current limit current. The primary inductance calculations for the PWR-SMP210 with 5 watts output show an inductance of 428 µH. The efficiency of the PWR-SMP210 at 5 watts and 100 VDC is 76%. The input power will be 6.58 W (5 W divided by 0.76). The average input current at 100 VDC will be 0.0658 A (6.58 W divided by 100 V). The average on time current with a 48% duty cycle is 0.137 A (0.0658 A divided by 0.48). The primary inductance L_p equals 428 µH. The nominal primary inductance of the T1002 is 738 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds / turn = 0).

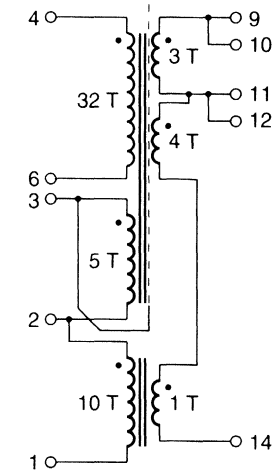
$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.48}{(1 - 0.48)} \times \frac{115 - 5}{5 + 0.5} = 18.5$$

Single Output Voltage

The standard transformer design can be modified for voltages other than 5 volts. This is achieved by changing the secondary winding to feedback winding turns ratio. The output voltage can be fine tuned by adjusting the R5, R6 voltage divider. However, the voltage on pin 11 of the PWR-SMP210BNC must be within the voltage range specified in the data sheet.

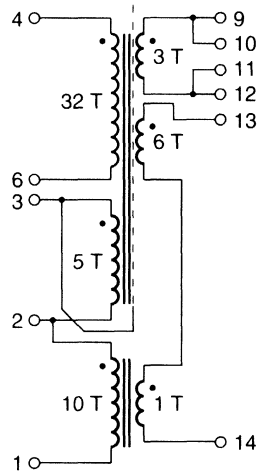


CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	+5 V OUTPUT
14	+12 V OUTPUT

PI-428-061391

Figure 16. 5/12 V Transformer Schematic Diagram.



CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	DRAIN
9/10	SECONDARY-SIDE COMMON
11/12	N/C
13	+5 V OUTPUT
14	+15 V OUTPUT

PI-429-061391

Figure 17. 5/15 V Transformer Schematic Diagram.

Output Transformer T1002 (cont.)

The output voltage can be increased to 12 volts by increasing the secondary to 7 turns. The transformer will generate 1.8 volts/turn less a 0.6 volt diode drop yields 12 volts.

The output voltage can be increased to 15 volts by increasing the secondary to 8 turns and increasing the number of junctions in D3 to two. The two junctions for D3 increases the output to 1.96 volts/turn. A 0.6 volt diode drop will yield a 15 volt output.

Multiple Output Voltages

The number of output voltages can be increased by adding additional output turns and voltage taps. A 5 volt and 12 volt output can be achieved with a 7 turn winding with a tap at 3 turns as shown in Figure 16. Figure 17 shows how a 5 volt and 15 volt output can be achieved with a 6 turn winding and a 3 turn winding. This scheme creates two separate supplies, 5 V and 10.5 V, and connects them in series.

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C15 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C15 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1.

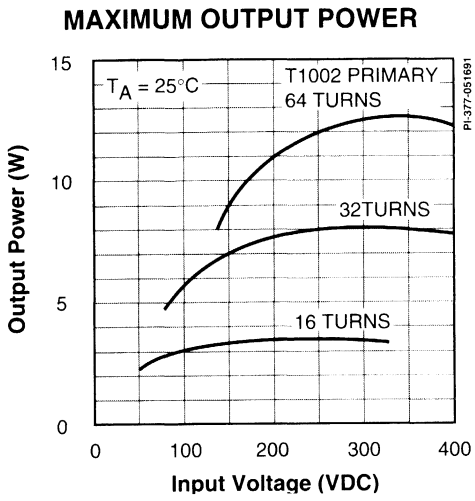


Figure 18.

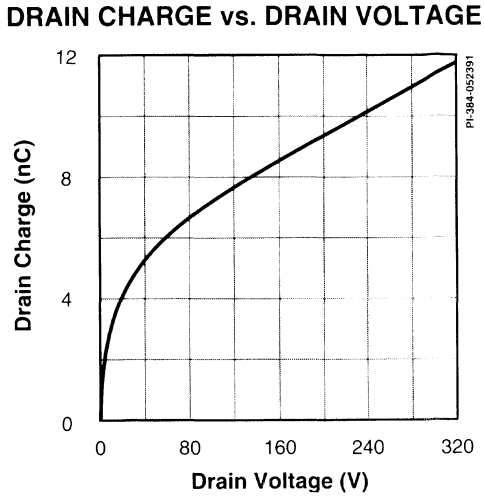


Figure 19.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package, the ambient temperature[5], and the peak switching transistor current limit circuit. The available output power as a function of input voltage for an 80°C temperature rise for the standard transformer T1002, and the performance with twice and half the normal number of primary turns (junction to ambient) is shown in Figure 18.

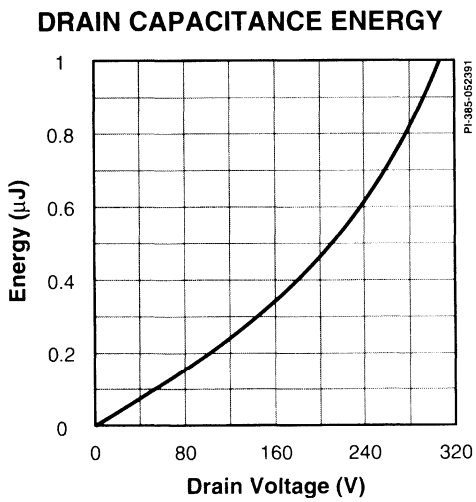


Figure 20.

Thermal Characteristics

The PWR-SMP210BNC is packaged in a 16-pin plastic power DIP package[6]. This package offers a lower thermal impedance as compared to a standard plastic DIP package. The thermal impedance from junction to ambient and from junction to case are 43°C/Watt and 6°C/Watt respectively. Soldered connections to the heat spreading "wings" (pins 4, 5, 12, and 13) provide a good thermal path while the DIP form factor maintains compatibility with automatic insertion equipment for low cost assembly. The thermal impedance from case to local ambient on a typical power supply board is 43-6 = 37°C/W. The local ambient temperature can be 10°C above ambient due to heating from other components on the printed circuit board.

The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and the transformer and damping network capacitances[7], and the losses in the pre-regulator when it is active. Figure 19 is the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 20. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this Figure to determine the total AC losses in the circuit.

Additional information on thermal management is available in AN-9.

CURRENT LIMIT CHARACTERISTIC

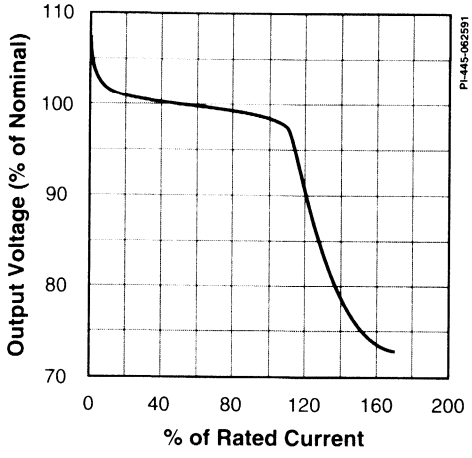


Figure 21.

Current Limit

Current limit is implemented by applying a current sense signal developed across R11 to a comparator input pin 6, $_{ILIMIT}$. The comparator triggers a latch which turns the power transistor off until the next clock cycle.

The voltage divider formed by R2 and R12 set the voltage across the current limit resistor R11 that will initiate the current limit function. The current limit circuit is a peak detection type of circuit. The circuit monitors the current flowing in the switching transistor. When the current exceeds the typical value of 280 mA for 250 ns the switching transistor is turned off for the rest of the oscillator cycle. The voltage across R12 at the moment of current limit threshold is 5.6 V - 0.34 V. The voltage across R11 when the current limit threshold is crossed can be calculated as follows:

$$V_{R11} = \left((V_S - V_{ILIMIT}) \times \frac{R2}{R12} \right) - V_{ILIMIT}$$

$$= \left((5.6 - 0.34) \times \frac{2.43k\Omega}{20.5k\Omega} \right) - 0.34 = 284mV$$

The effect on the output voltage can be seen in Figure 21. The shape of the current limit function is very close to a constant power curve[8]. This is because the circuit regulates the peak current in the transformer primary providing a constant energy delivery to the core during current limit, thus a constant power output in current limit.

Operating Frequency

The operating frequency of the PWR-EVAL5 is typically 250 kHz. A timing capacitor of 25 pF for the oscillator is internal to the PWR-SMP210BNC. The frequency of operation is adjustable and the printed circuit board has a location for an external frequency setting capacitor C11 connected to pin 8 of U1. The nominal operating frequency can be estimated with the following formula:

$$f = \frac{67.4\mu A}{\frac{2.2V}{25pF + C_{EXT}}}$$

Voltage Control Loop

The PWR-SMP210BNC has a voltage-mode control circuit[9]. The DC input to output voltage transfer function when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P} \right) \times \frac{D}{(1 - D)}$$

where D is equal to the duty cycle of the switching transistor[10]. The duty cycle is controlled by the output voltage error amplifier. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[11,12] is included in the documentation disk. T1, U1, R4, R5, C2 and C4 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The model for the operating point duty cycle transformation uses a transconductance generator and a voltage gain stage. The coefficients of the small signal pulse width modulator transfer-function generators are calculated by knowing the primary reflex voltage (output voltage plus rectifier forward drop times the transformer turns ratio), the duty cycle of the operating point of interest and the load resistance transformed to the primary of the transformer:

$$R = R_O \times \left(\frac{N_P}{N_S} \right)^2 = 5 \times \left(\frac{32}{3} \right)^2 = 569\Omega$$

The voltage generator gain:

$$E = \frac{-V}{D^2} = \frac{-59}{(0.269)^2} = -815$$

The current generator gain:

$$J = \frac{-V}{(1 - D)^2 \times R} = \frac{-59}{(1 - 0.269)^2 \times 569} = -0.194$$

3

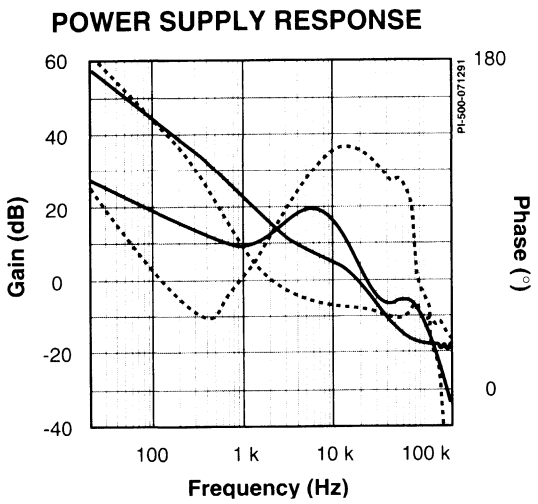


Figure 22.

The current generator is to provide the negative input impedance effect of a switching regulator and can be neglected if the resonant frequency of the EMI filter is much higher than the control loop frequencies of interest.

The measured open loop gain/phase response curve for 120 VRMS input, solid lines and 240 VRMS input, dashed lines are shown in Figure 22. The 120 VRMS input control loop has 72° phase margin, an open loop unity gain crossover frequency of 17 kHz and 18.8 dB gain margin at 170 kHz with a 5 W load. This provides 43 dB of gain at 120 Hz for power line ripple rejection. The 240 VRMS input control loop has 84° phase margin, an open loop unity gain crossover frequency of 2 kHz and 11.7 dB gain margin at 151 kHz with a 5 W load. This provides 43 dB of gain at 120 Hz for power line ripple rejection.

The output ripple voltage at the power line frequency can be estimated by knowing the open loop gain of the regulator, the transformer turns ratio and the operating duty cycle of the flyback switching regulator. The output peak to peak ripple voltage at the power line frequency can be calculated from the following equation:

$$V_{o(pp)} = \frac{V_{in(pp)} \times \frac{N_S}{N_P} \times \frac{D}{1-D}}{A_V} = \frac{20 \times \frac{3}{32} \times \frac{0.27}{1-0.27}}{178} = 3.9\text{mV}$$

The DC model for the error amplifier within the integrated circuit is shown in Figure 23. Figure 24, the error amplifier open-loop gain/phase response curve, shows that the amplifier is stable in the unity gain feedback configuration.

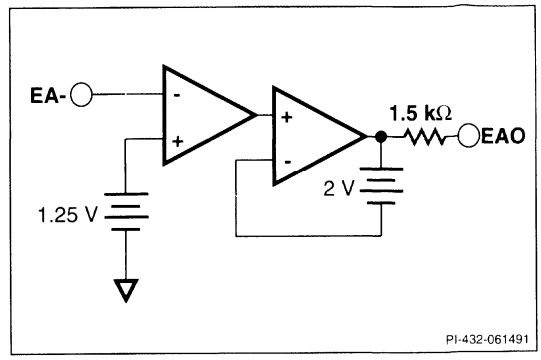


Figure 23. Error Amplifier Equivalent Circuit.

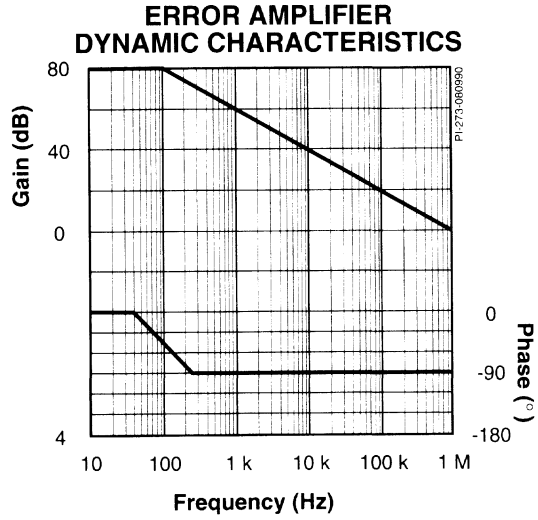


Figure 24.

Protection Features

Overtemperature

The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 135°C and keeps it off until the junction temperature decreases 45°C[13].

Test Mode

The I_{LIMIT} input (pin 6) controls the built in test logic of the integrated circuit. The built-in test logic turns on the power transistor continuously when the voltage on pin 6 is equal to the pin 7 voltage (5.6 volts) +/- 1.5 V Do not put the circuit in test mode while operating in a power supply circuit as this could destroy the PWR-SMP210.

Control Circuit Undervoltage Protection

The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is typically 5 volts on pin 7.

Input Filtering and Rectification

BR1 and C1 perform the input rectification and filtering function. The rectifier bridge should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage rating on C1 is equal to the peak value of the maximum rectified input voltage, 200 V for 115 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitor, C1, can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage the power supply will provide a regulated output voltage at maximum power, and the minimum AC input voltage[14]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 when the input bridge diodes stop conducting, and V_2 is the voltage on C1 when the input bridge diodes start conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the input capacitor value.

Input Surge Current

When line voltage is applied to the power supply a surge of current flows in the input of the power supply to charge the input storage capacitor C1[15]. The magnitude of current must be within the surge ratings of the power switch, fuse and input rectifiers. The surge current is limited by the resistance of the EMI filter. L3, the differential mode filter inductor contributes the majority of the EMI filter resistance of 8 Ω. This limits the peak surge current to 160 V/8 Ω = 20 A.

3

EMI Considerations

This power supply was designed to meet worldwide EMI (DIN VDE 0805/05.90) and safety (UL1950 and IEC950) specifications. Figure 25 is a plot of the conducted EMI relative to the FCC specification limits.

Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L3 and C6 filter differential mode conducted emissions.

Common Mode Filter
L2, L4, C7, C8, C12, and C17 filter common mode conducted emission currents[16]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C12 couples high-frequency noise back to the system chassis ground. C7, C8, and C17 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP210. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L4 in series with the ground lead of the power connector is a "lossy" bead and is equivalent to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

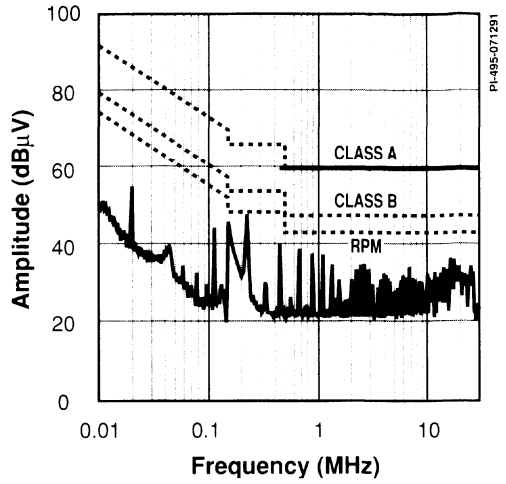


Figure 25. EMI Plot of the PWR-EVAL5.

Safety Agency Requirements

The PWR-EVAL5 is being submitted to TUV Rhein Land for evaluation to the IEC 950.

Additional information on safety and layout-related issues is available in DA-2.

Documentation Disks

The PWR-EVAL5 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL5 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README5.BAT	(This file) contains a summary and last minute information on PWR-EVAL5
PWB1002B.APR	Aperture file with assigned D-codes
EVAL5.BOM	Bill of Materials file
EVAL5ASY.DWG	Assembly drawing file
FAB1002B.DWG	Fabrication drawing for the PC board
1002BCL.G23	Copper layers gerber file
1002BSM.G23	Solder mask layers gerber file
1002BSKP.G23	Silkscreen and padmaster gerber file
EVAL5.LIB	Library file of the part symbols used in both schematics
PWB1002B.NCD	NC drill file for computerized drilling of the PCB
EVAL5.SCH	Schematic file of PWR-EVAL5
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES5.TXT	Functional description of the power supply circuitry used in PWR-EVAL5
ICDESC2.TXT	Functional description of the PWR-SMP210 integrated circuit used in PWR-EVAL5
EVL5COST.TXT	Estimated parts cost
T1002 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD 286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README5.BAT and the EVAL5.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP210.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

References

1 Leman, Brooks R. "Implementing Off-line, Isolated Power Supplies with a New Integrated MOSFET Switch/Controller Technology" Proceedings HFPC, May 1990, pp. 124-132.

2 Wilson Jr.,Thomas "Cross Regulation in an Energy-Storage DC-to-DC Converter with Two Regulated Outputs" PESC 77 Record, pp. 190-199

3 Kamm, Edith "New Military EMI Specifications Affecting the Input Circuit Architecture of AC to DC Converters" Proceedings, Eighth National Solid-State Power Electronics Conference (Powercon 8), April 1981, C.3.1-C.3.11

4 Leman, Brooks R., U.S. Patent Number 5,008,794

5 Davis, Paul A. "Thermal Packaging Concepts in Power Supply Design" HFPC 89 Proceedings, May 1989, pp. 446-458

6 Power Integrations Data Book, July 1991.

7 Keller, R., Leman, B. "New Integrated Technology Combines 800 V High-Speed Power MOSFET Switch with Pulse Width Modulation Control Circuitry for Power System Applications" Proceedings, High Frequency Power Conversion International June 1991, p. 61

8 Harada, K., Ninomiya, T., Nabeshima, T. "On the Precise Regulation of Multiple Outputs in a DC-DC Converter with an Energy-storage Reactor" IEEE Power Electronics Specialists Conference Record, 1979, p. 162

9 Middlebrook, R.D. "Power Electronics: Topologies, Modeling and Measurement" Proceedings of the IEEE International Symposium on Circuits and Systems, 1981 Record, April 27-29 1981

10 Severns, R.P., Gordon, E. Modern DC-DC Switchmode Power Converter Circuits Van Nostrand Reinhold Company, p 231

11 Middlebrook, R.D., Cuk, Slobodan, "Modeling and Analysis Methods for DC-to-DC Switching Converters" Proceedings of the IEEE International Semiconductor Power Converter Conference, 1977 Record, pp. 90-111

12 Keller, Richard, "The Off-Line Converter as a Closed Loop System: Loop Design, Measurement and Analysis" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, A2.1-A2.9

13 Thermal Shutdown Application notes: National Semiconductor AN-82, AN-103

14 Tartar, Ralph E., Principles of Solid-state Power Conversion Howard W. Sams & Co., Inc., 1985, p. 232

15 Hirshberg, Walter "Optimizing Line Inrush Design in Off-Line Converters" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, E3.1-E3.7

16 Nave, Mark J. "Measuring, Suppressing, and Filtering Common Mode Emissions in Switch-Mode Power Supplies" HFPC 89 Proceedings, May 1989, pp. 285-293

PWR-EVAL6

PWR-INT200/201/202 Board

Bare Printed Circuit Board
Multi-phase Half Bridge Layout

POWER INTEGRATIONS, INC.

Product Highlights

User-configurable Circuit Board

- 3 half bridge layouts can be used independently, or for full bridge or 3-phase applications
- Accomodates application-specific external circuitry
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits

- Input undervoltage lockout
- Simultaneous conduction lockout (when using PWR-INT200)
- Assymetric drive currents and built-in assymetric delays minimize the risk of shoot-through
- Schmitt-triggered inputs and unique low-to-high side communication technique maximize noise immunity

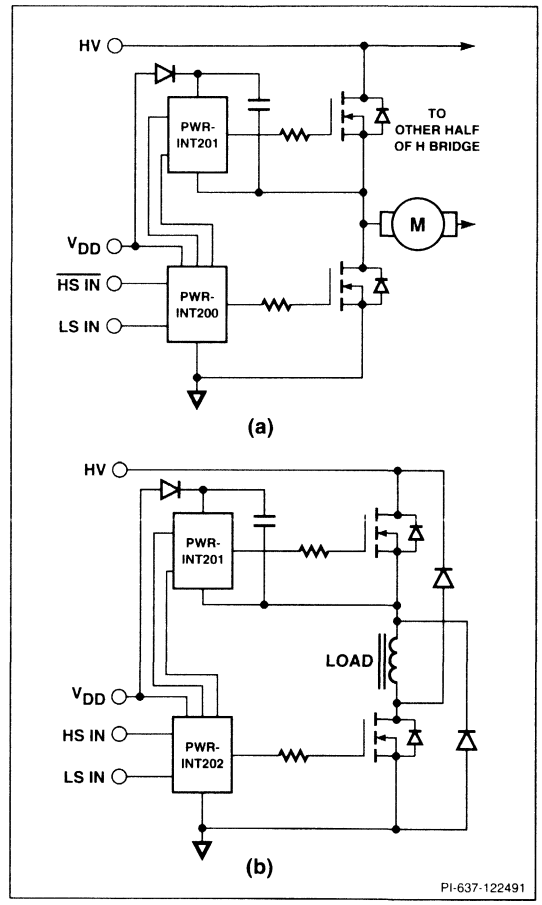


Figure 1. Typical Application Circuits.

Description

The PWR-EVAL6 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-INT200 and PWR-INT202 low-side MOSFET drivers, and the PWR-INT201 high-side MOSFET driver.

The PWR-INT200 or PWR-INT202 low-side drivers, when used in conjunction with the PWR-INT201 high-side driver, provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads.

Applications include motor drives, electronic ballasts, and uninterruptible power supplies. These parts can also be used to implement full- bridge and multi-phase configurations.

The PWR-EVAL6 evaluation board comes unpopulated, and can be assembled to evaluate half bridge, full bridge, or 3-phase applications.

ORDERING INFORMATION	
PART NUMBER	OUTPUT CONFIGURATION
PWR-EVAL6	3 SINGLE PHASE OUTPUTS

EVALUATION BOARD FEATURES

This demonstration board is designed to simplify evaluation of the PWR-INT200/201/202 half bridge driver family. Half bridge, full bridge, and three phase circuit configurations can all be easily realized using this board. Inputs to the board are power (high-voltage and low-voltage bias) and 5V CMOS control signals. Loads can be connected to any of the three phases and to either high voltage rail.

The demonstration board has been designed to implement each of the circuit techniques discussed in application note AN-10: Function and Application of the PWR-INT200-202. Refer to AN-10 for guidelines on selecting specific component values for each of the following circuit techniques:

- Input series gate resistors
- Asymmetric gate drive impedance networks
- Driver output clamping
- Minimizing effects of parasitic series inductance
- Input signal conditioning

Each of these circuits can be effectively disabled by either leaving the component positions blank or installing appropriate jumpers. A jumper table is given with each circuit diagram which properly configures the evaluation board.

Other features designed to facilitate breadboarding include:

- On-board fuse for the high-voltage bus
- Pad spacings to accept TO-220, TO-218, and TO-247 power transistor packages
- On-board 5 V linear regulator for signal strapping and pullup

Refer to Figures 8 and 9 at the end of this document for a complete component placement and schematic diagrams.

BASIC HALF BRIDGE OPERATION

One phase of a simple three phase bridge circuit is shown in Figure 2. This circuit easily interfaces between a motor controller and the three phases of the load.

SWITCHED RELUCTANCE OPERATION

A simple switched reluctance three phase circuit is shown in Figure 3. Note that the source of a high side transistor is no longer connected to the drain of a low side transistor. Note also the diodes which commutate the winding current when both devices in each leg are turned off.

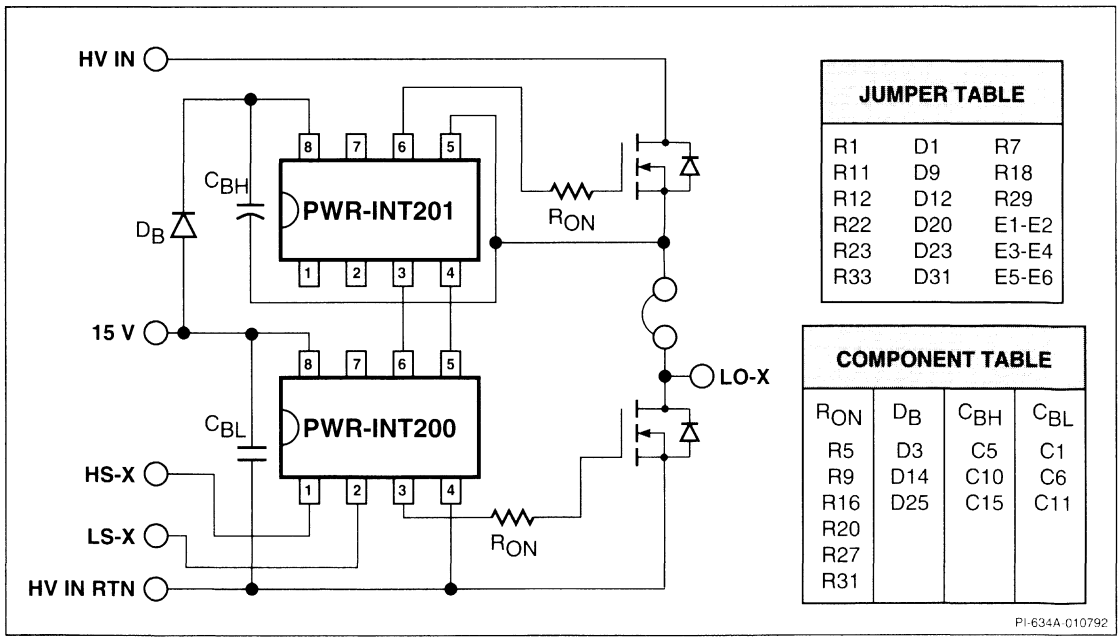


Figure 2. One Phase Example of a 3-phase Half Bridge Drive Circuit.

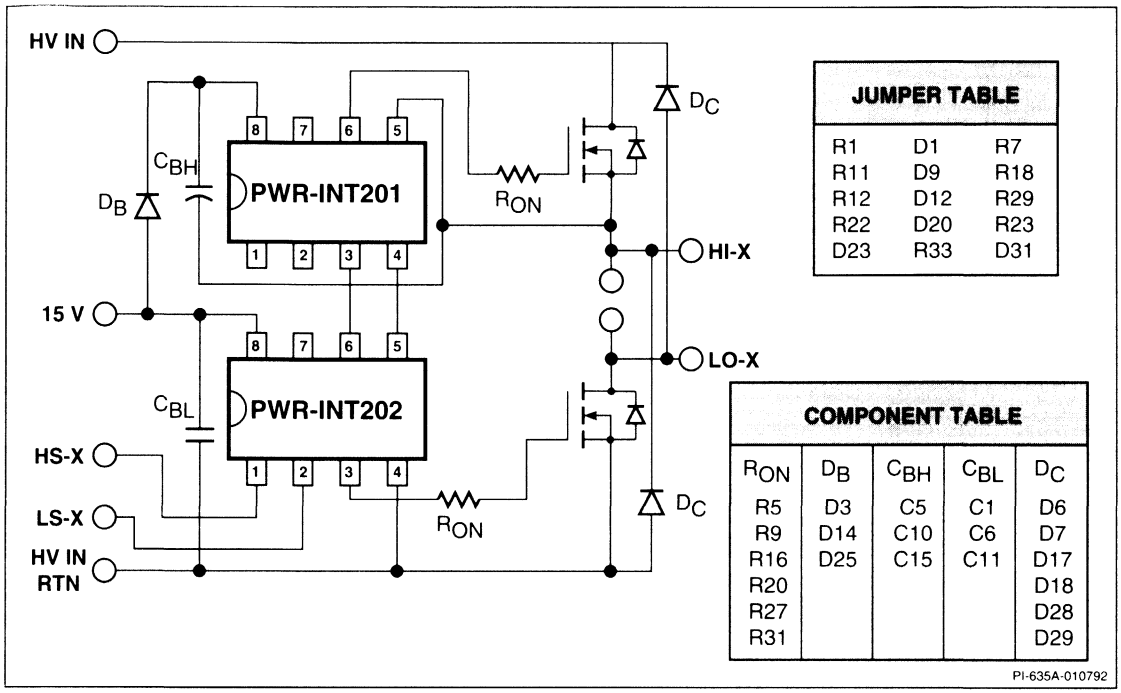


Figure 3. One Phase Example of a Switched Reluctance Drive Circuit.

ASYMMETRIC GATE DRIVE NETWORKS

The asymmetric gate drive circuit shown in Figure 4 turns on the power MOSFET switch through resistance Ron while turning off through the lower effective value of RonllRoff. This technique provides smaller turn off delays than the single resistor circuit described above.

DRIVER OUTPUT CLAMPING

Schottky diodes can be added to the driver output as shown in Figure 5 for some high speed applications. The diodes provide a path for noise currents to flow immediately following transitions of the power MOSFET switch.

INDUCTIVE OVERSHOOT PROTECTION

The circuits shown in Figure 6 are useful for applications where the AC voltage overshoots below ground. Resistor Rs prevents the bootstrap capacitor from overcharging while the blocking diodes prevent HSD1 and HSD2 from being pulled below ground.

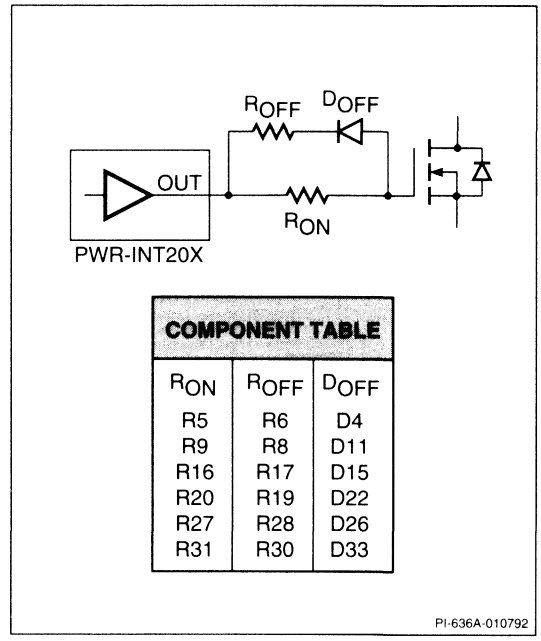
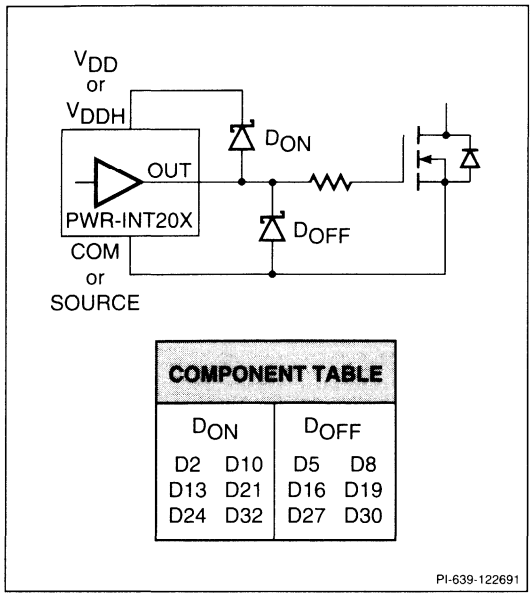
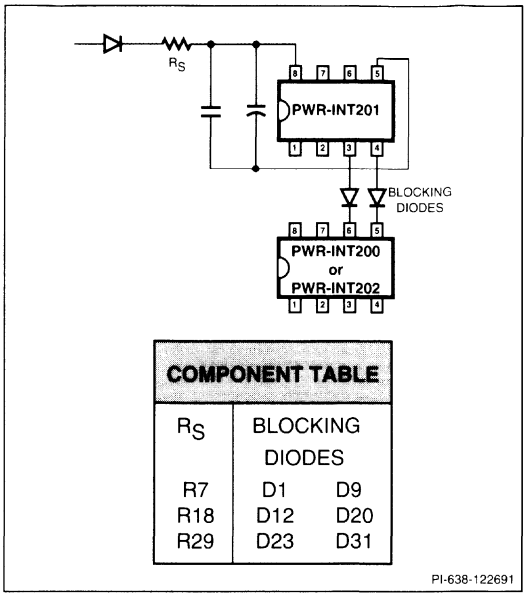


Figure 4. Asymmetric Gate Drive Components.



COMPONENT TABLE	
D_{ON}	D_{OFF}
D2 D10	D5 D8
D13 D21	D16 D19
D24 D32	D27 D30

Figure 5. Driver Output Clamping Components.



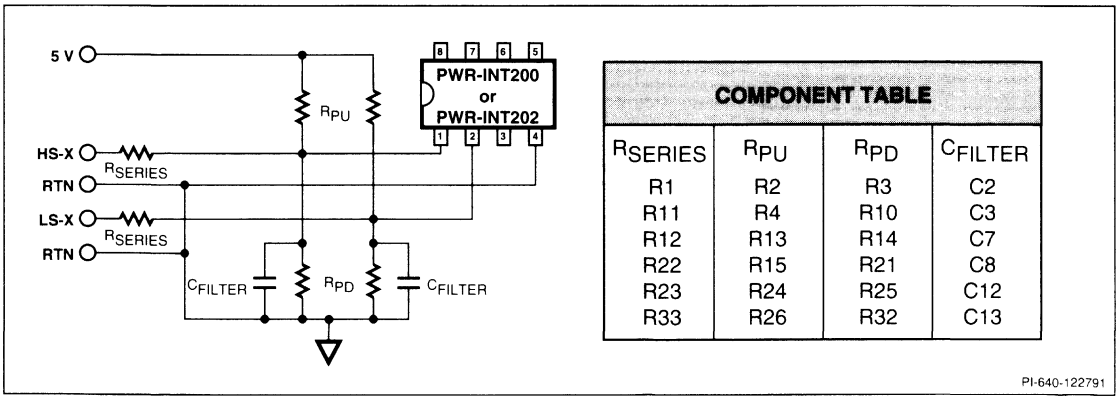
COMPONENT TABLE	
R_S	BLOCKING DIODES
R7	D1 D9
R18	D12 D20
R29	D23 D31

Figure 6. Inductive Overshoot Protection Components.

INPUT SIGNAL CONDITIONING

This circuitry shown in Figure 7 consists of a series, pullup, and pulldown resistor. A filter capacitor is also included. Many different combinations of these components can be used depending on the logic system outputs in the application. Some examples are:

- Open collector logic outputs would require the pullup resistor.
- 10 to 15 Volt logic signals would require a divider formed by the series and pull down resistors.
- Long wiring between the controller and driver could use the pullup and pulldown resistors as termination impedances.



COMPONENT TABLE			
R_{SERIES}	R_{PU}	R_{PD}	C_{FILTER}
R1	R2	R3	C2
R11	R4	R10	C3
R12	R13	R14	C7
R22	R15	R21	C8
R23	R24	R25	C12
R33	R26	R32	C13

Figure 7. Input Signal Conditioning Components.

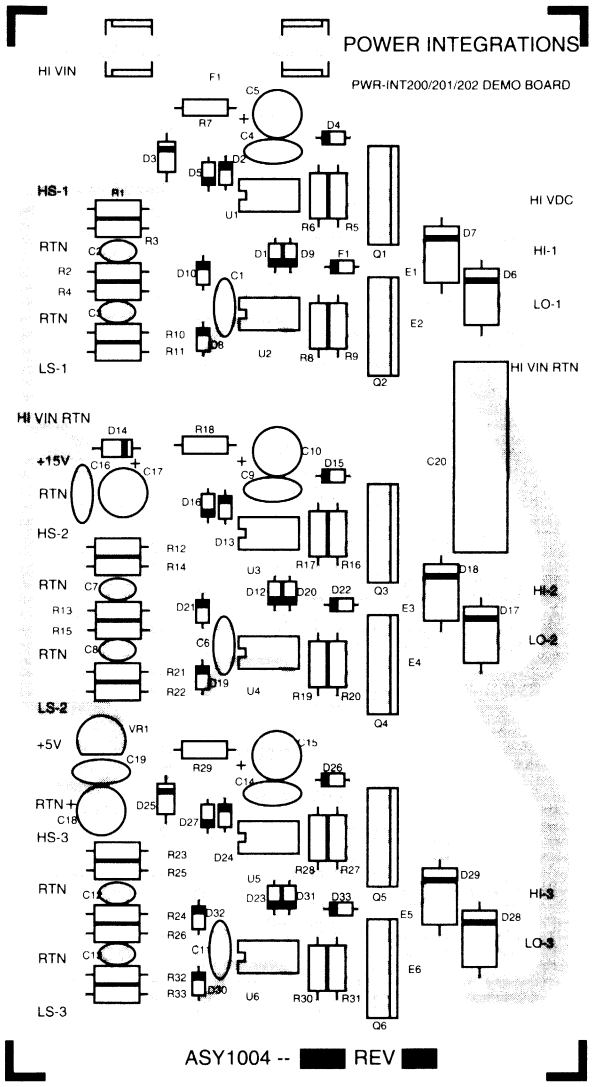


Figure 8. Component Legend of the PWR-EVAL5.

MISCELLANEOUS FEATURES

The following features are shown on the component placement drawing in Figure 8. The evaluation board was designed to accomodate T0-220, TO-218, and TO-247 power MOSFET packages.

Each bootstrap capacitor location has a ceramic capacitor in parallel with an aluminum electrolytic capacitor such that either can be used.

A fuse (F1) location and high voltage bypass capacitor (C20) location are provided.

On board 5 V V_{CC} for the logic inputs can be provided directly from the 15 V V_{DD} by installing a 78L05 linear regulator (VR1).

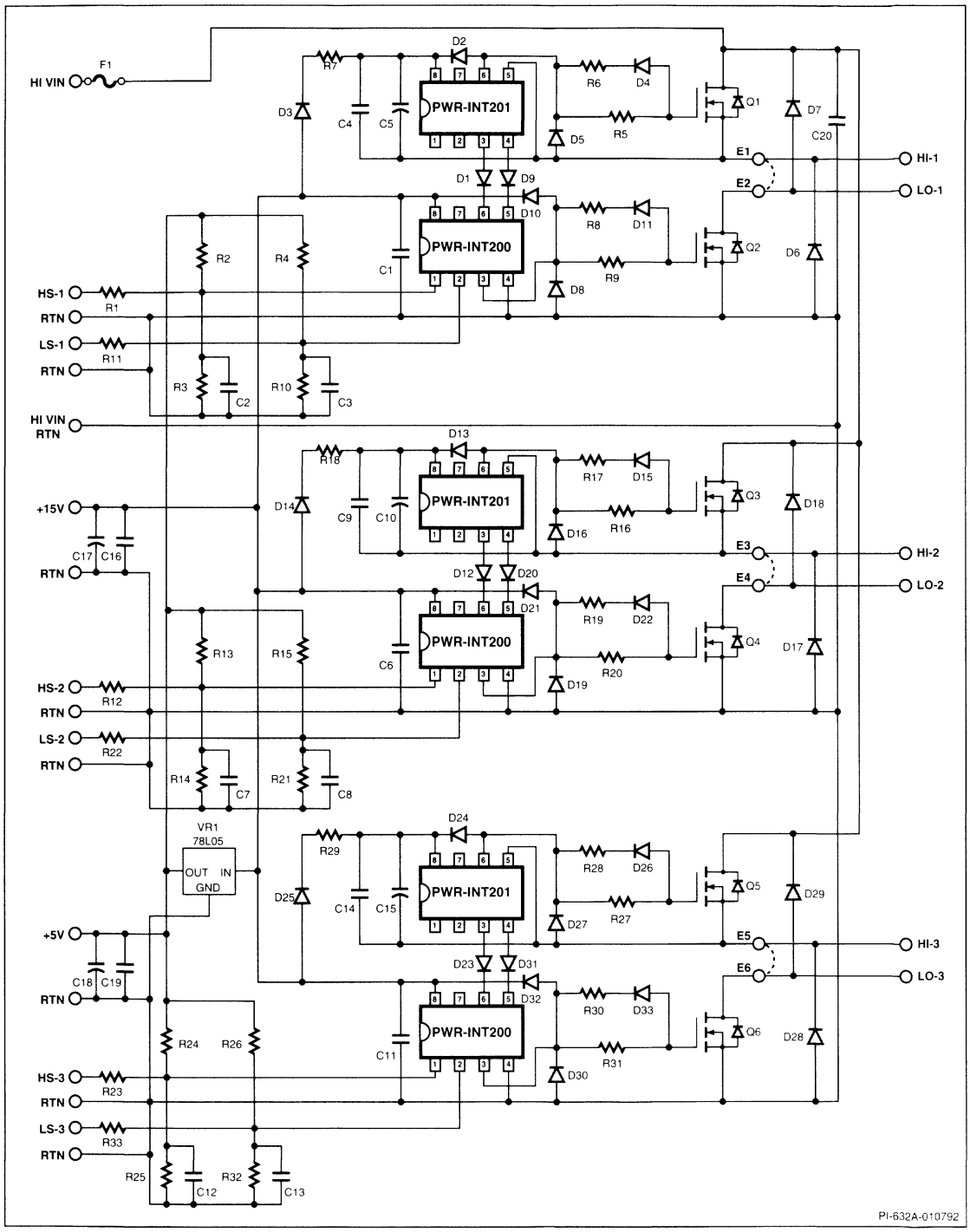


Figure 9. Schematic Diagram of the PWR-EVAL6 Circuit, Including all External Component Options.

PWR-EVAL7

PWR-SMP260 Evaluation Board

110/220 VAC Input
Isolated 5/12 V, 30 W (Total) Output

POWER INTEGRATIONS, INC.®

Product Highlights

Isolated 5 V Output from 110/220 VAC Input

- Up to 30 watts of output power can be supplied
- Isolation is provided by transformer designed to UL/VDE specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits

- Input undervoltage lockout
- External current limit
- Thermal shutdown
- Soft-start
- Overload shutdown/auto-restart

Designed to Meet Regulatory Standards

- Layout designed to meet UL/CSA/VDE requirements
- Meets DIN VDE 0805/05.90 Level B

Description

The PWR-EVAL7 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP260WTC power supply IC.

The PWR-SMP260, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a current-mode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP260 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP260 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL7 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

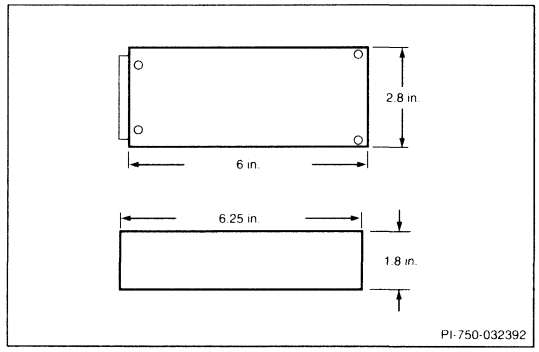


Figure 1. Evaluation Board Overall Physical Dimensions.

PARAMETER	LIMITS
Input Voltage Range	85 to 265 VAC
Input Frequency Range	47 to 440 Hz
5 V Output Voltage Range Load Current Range	 4.5 to 5.5 VDC 0 to 3 A
12 V Output Voltage Range Load Current Range	 10.8 to 13.2 VDC 0 to 2 A
Temperature Range	0 to 70°C
Efficiency	> 77%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	**OPERATING VOLTAGE**
PWR-EVAL7	110/220 VAC INPUT 5/12 VDC OUTPUT @ 30 W

3

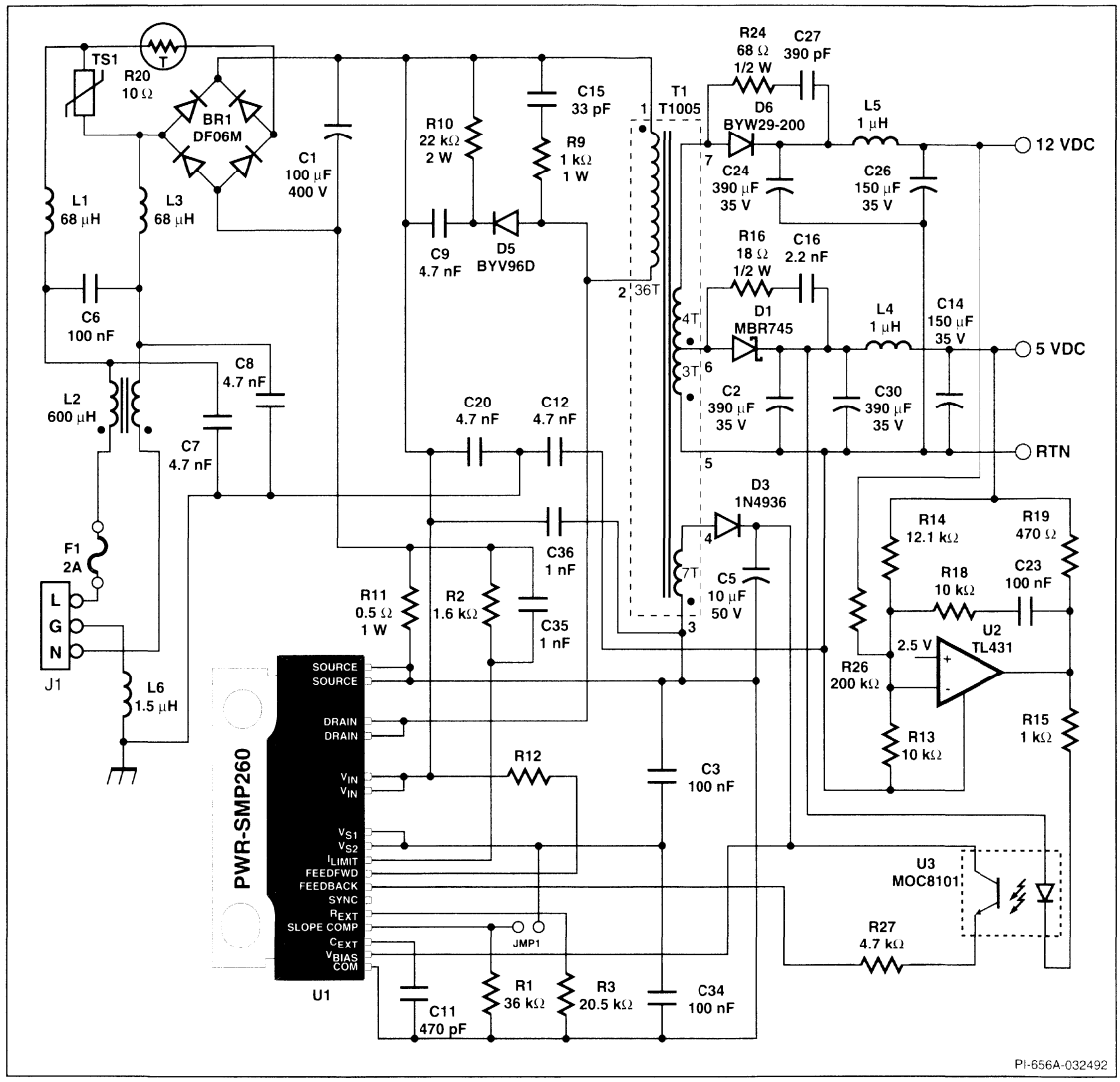


Figure 3. Schematic Diagram of the PWR-EVAL7 Power Supply.

General Circuit Description

The PWR-EVAL7 is an isolated Buck-Boost (flyback) switching power supply[1] topology. The power supply is implemented using the PWR-SMP260WTC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1005 standard transformer (see DA-3), will produce a dual output 30 watt power supply that will operate from 85 to 265 VAC input voltage. The PWR-EVAL7 has a fully regulated 5 V output and a semi-regulated 12 V auxiliary output. The output voltages are selected by the turns ratios of the T1 output windings and the voltage divider formed by resistors R13, R14, and R26.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	100 µF, 400 V	LGQ2G101MHSA	Nichicon
C2, C24, C30	390 µF, 35 V	UPL1V391MPH	Nichicon
C3, C23, C34	100 nF, 50 V	K104Z20Z5UFVBWN	Philips
C5	10 µF, 50 V	UVZ1H100MDH	Nichicon
C6	100 nF, 250 VAC	F1772-410-2000	Roederstein
C7, C8, C12, C20	4.7 nF, 250VAC	F1710-247-1000	Roederstein
C9	4.7 nF, 1 kV	D472M47Z5UNAAEM	Philips
C11	470 pF, 50 V	K471J15C0GFVBWA	Philips
C14, C26	150 µF, 35 V	UPL1V151MPH	Nichicon
C15	33 pF, 1 kV	D330K29S2LNAAAL	Philips
C16	2.2 nF	D22M39Z5UNAAEM	Philips
C27	390 pF, 1 kV	D391K20Z5FNAAEM	Philips
C36	1 nF, 1 kV	D102P29Z5UNAAEM	Philips
C35	1 nF, 50 V	K102M15X7RFVBWA	Philips
BR1		DF06M	General Instruments
D1		MBR745	Motorola
D3		1N4936	Motorola
D5		BYV96D	Philips
D6		BYW29-200	Philips
F1	2 A , 250 VAC	230.002	Littelfuse
L1, L3	68 µH	SN8D-500	Tokin
L2	600 µH	SU10V-20006	Tokin
L4, L5	1 µH	RL-1160-1.0	Renco
L6	BEAD	2673200201	Fair-Rite
R1	36 kΩ	5043CX36K00J	Philips
R2	1.6 kΩ	5043CX1K600J	Philips
R3	20.5 kΩ, 1%	5043EM20K50F	Philips
R10	22 kΩ, 2 W	MO-2 223J	Koa/Speer
R11	500 mΩ, 1 W	RSS-1 0R5J	Koa/Speer
R13	10 kΩ, 1%	5043EM10K00F	Philips
R14	12.1 kΩ, 1%	5043EM12K10F	Philips
R15	1 kΩ	5043CX1K000J	Philips
R16	18 Ω, 1/2 W	5053CX18R00J	Philips
R18	10 kΩ	5043CX10K00J	Philips
R19	470 Ω	5043CX470R0J	Mepco
R20	10 Ω - Thermistor	SG220	Ketema
R24	68, 1/2 W	5053CX68R00J	Philips
R26	200 kΩ, 1%	5043EM200K0F	Philips
R27	4.7 kΩ	5043CX004K7J	Philips
TS1		V275LA20A	Harris
U1		PWR-SMP260WTC	Power Integrations
U2		TL431CLP	Motorola
U3		MOC8101	Motorola
T1		T1005	Custom*
HS1		6263	Thermalloy
HS2,HS3		6225	Thermalloy
JMP1		22 AWG	Bus Wire
J1	Plug Socket	EAC-303	Switchcraft
	PC Board	ASSY 1007-A	Custom**

Figure 4. Parts List for the PWR-EVAL7

Component Listing (cont.)

Reference	Value	Part Number	Typical Manufacturer

Custom Components:

* Qualified manufacturers are:

AT&T Microelectronics	(800) 372-2447	FAX: (214) 284-8282
Datatronics	(714) 928-7731	FAX: (714) 928-7701
Delta (Taiwan)	(02) 7164822	FAX: (02) 7169764
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin (Japan)	(03) 402-6166	FAX: (03) 497-9756

** Manufacturer is:

CBR Circuits
116 Minnis Court
Milpitas, CA 95035
(408) 946-3446

Figure 4. Parts List for the PWR-EVAL7

The circuit groups in the schematic Figure 3 are as follows. L1, L2, L3, L6, C6, C7, C8, C12, and C20 form the EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. D5, C9 and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the leakage inductance ringing voltage. The damping network improves the EMI performance of the supply. R2, R11, R14, R18, R26, C2, C14, C23, C24, C26, C30, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP260. C11 sets the switching frequency of the power supply. C3, C5,C34, C35, and C36 are bypass capacitors. C3 supplies the pulsed current required to charge the gate of the output power FET when it is turned on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. R2 and R11 form the cycle-by cycle current limit and current mode control circuitry. R11 senses the primary current, and R2 is used to set the current sense comparator reference voltage. R1 can be used to set the amount of slope compensation current flowing in the current-mode control circuit.. R12 is an optional

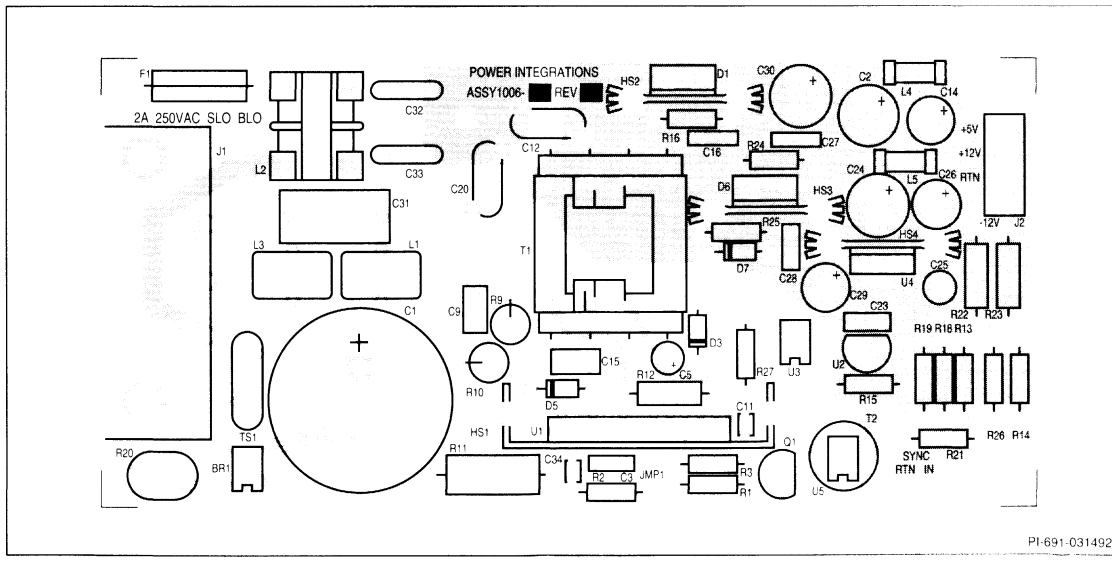


Figure 5. Component Legend of the PWR-EVAL7.

feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. D1, C2, C14, C30, and L6 rectify and filter the 5 V output. R16 and C16 damp the ringing caused by the reverse recovery of D1. D6, C24, C26, and L6 rectify and filter the 12 V output. R24 and C27 damp the ringing caused by the reverse recovery of D6. U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13, R14 and R26 form a voltage divider that sets the output voltages of the supply. R27 limits the AC current coupled from the V_{BIAS} supply through optocoupler U3.

The PWR-EVAL7 printed circuit board has circuit traces for several optional features which can be implemented by adding additional components. These include a linear-regulated -12V auxiliary output, transformer coupled external frequency synchonization, and an optically-coupled remote inhibit function.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 were measured by applying a DC input voltage to the PWR-EVAL7.

Load Regulation (Figures 6 and 7) - The amount of output voltage change for a change in output current is referred to as load regulation. The 5 V output changes less than 2% for a 10% to 100% load current range. The 12 V output changes less than 7.5% for a 10% to 100% load change. Below 10% of rated load, the 12 V output rises due to the leakage inductance between the secondaries of the transformer[2]. This rise becomes progressively more severe as the 5 V load is increased. To help combat this trend, R26 was added to the error amp circuit. This resistor samples a portion of the 12 V output voltage and adds it to the 5 V voltage divider. Thus, a rise in the 12 V output will cause the control circuit to scale back both the 5 V and 12 V outputs slightly. This improves the 12 V regulation, but deteriorates the 5 V regulation by about 1%. The 12 V regulation can be further tightened by decreasing the value of R26, at the expense of 5 V regulation. Decreasing R26 will also decrease the nominal 5 V output voltage. This value can be trimmed by increasing the value of R14, or by reducing the value of R13. If extremely tight regulation is required on both outputs, a post-regulator can be added to the 12 V output, making the two outputs essentially independent of one another. The disadvantages of this approach are increased parts count and reduced efficiency.

Line Regulation - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage from 100 to 400 VDC input, for both outputs, is 0.5% for an input voltage change of 100 V(rms) or 50 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first-cut transformer design procedure. Efficiency at full load and nominal line voltage is 78%. Full load is defined as a 2.5 A load on the 5 V output and a 1.5 A load on the 12 V output, for a total output power of 30.5 W. The ratio of 5 V power to 12 V power was held constant for the load efficiency curve.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typcial output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[3]. The power factor of the PWR-EVAL7 with a 30W load is approximately 0.6 at a input voltage of 115VAC.

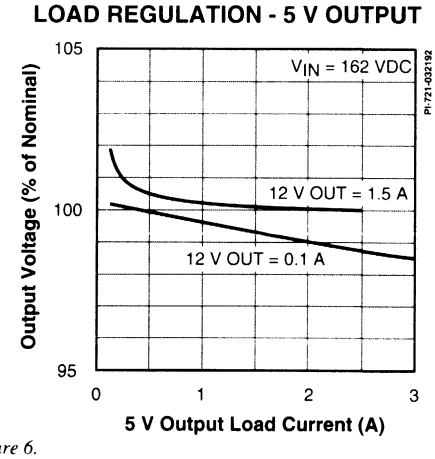


Figure 6.

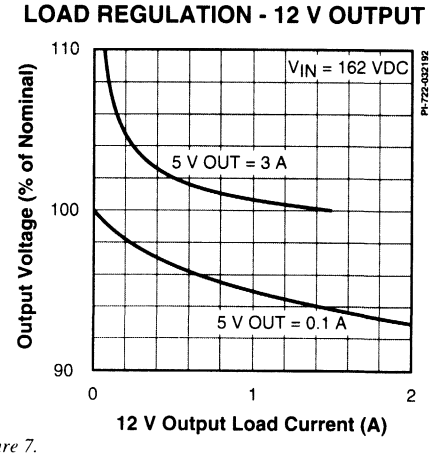


Figure 7.

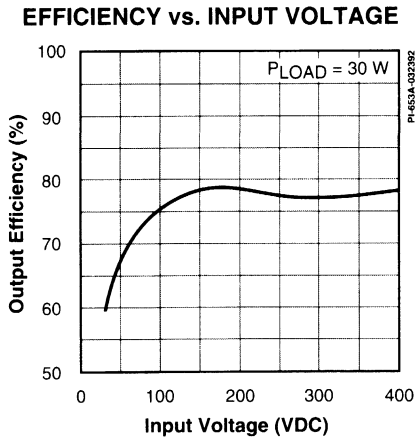


Figure 8.

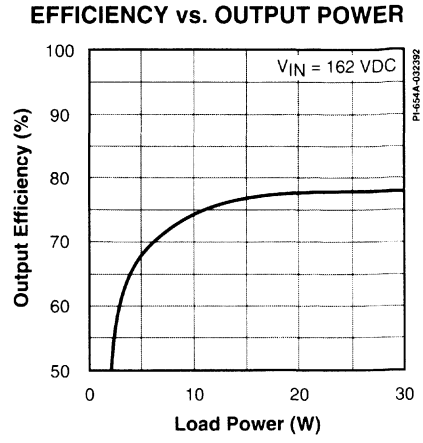


Figure 9.

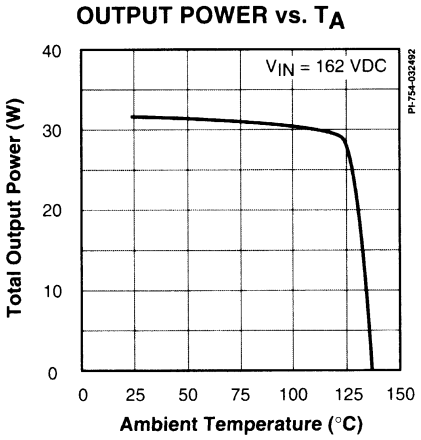


Figure 10.

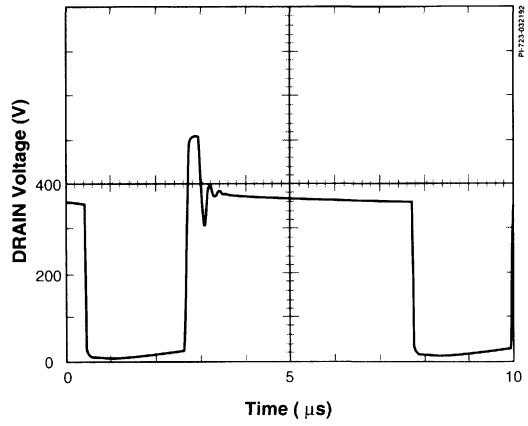


Figure 11. Drain-source Voltage of the PWR-SMP260.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum, the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a BYW29-200 diode. Figure 13(c) is the anode of D2 when D2 is a MUR820 diode. The BYW29-200 is rated at 200 V with a reverse recovery time of less than 25 ns. The MUR820 is rated at the same voltage with a reverse recovery time of 60 ns. The BYW29-200 exhibits a recovery time of approximately 26 ns in the circuit, providing good functionality. However, the MUR820 exhibits a 48 ns recovery time in the circuit. This length of recovery time does not work well in the circuit, as evidenced by the large value of undershoot on the voltage waveform.

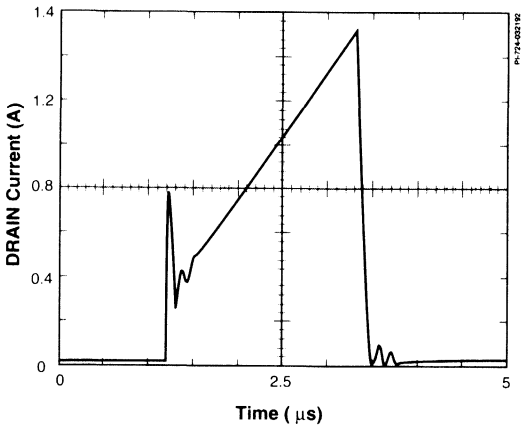


Figure 12. Drain Current of the PWR-SMP260.

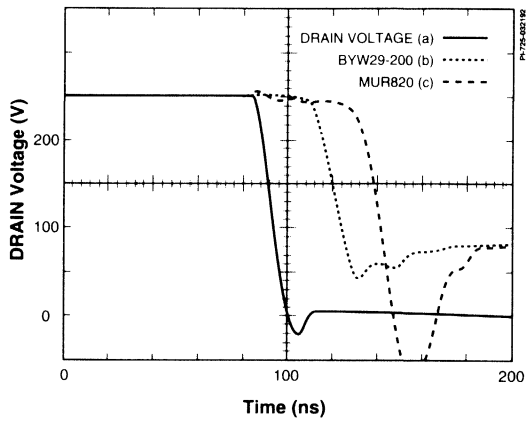


Figure 13. Recovery Times of Output Rectifier Diodes.

Bias Supplies

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. This regulator maintains the voltage on pins 10 and 11 at approximately 6 V. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the bias winding and filter provides bias current and turns off the pre-regulator when the power supply is operating.

Minimum Load

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. A shunt regulator is activated when the summing junction current falls below 12% of full scale. The shunt regulator will increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale. Figure 14 shows the load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The control loop gain path is shown in Figure 15. The gain of the minimum load regulator has been matched to the gain of the current mode switching regulator. This allows the control loop dynamics to remain the same whether the minimum load circuit is active or not active. This helps prevent degradation of the load transient response at light load.

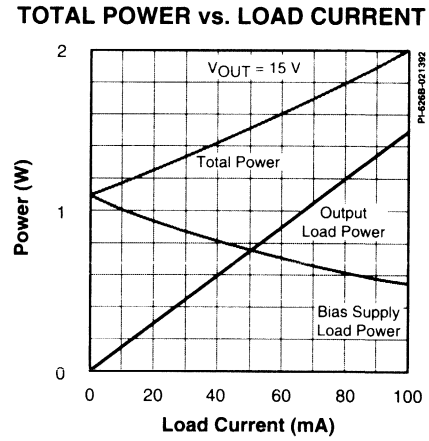


Figure 14. Minimum Load Transfer Characteristic.

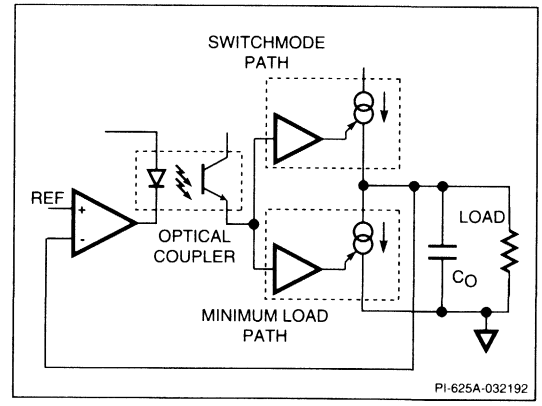


Figure 15. Control Loop Gain Path.

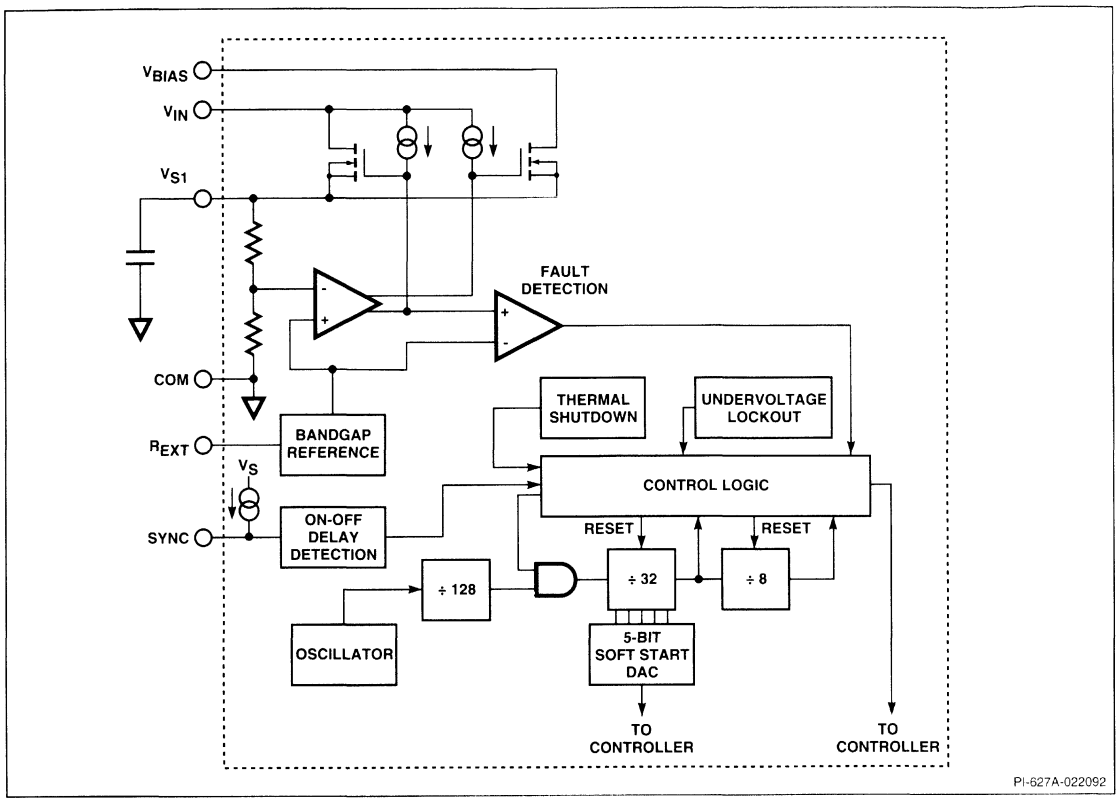


Figure 16. Soft-start section Functional Block Diagram.

Soft-Start

The soft-start function allows the power supply to start up in a controlled fashion. Flyback power supplies without soft-start will drive a large current into the output capacitors and load upon start-up, causing a peak power stress many times higher than the normal operating level. This power surge can unduly stress the power switch and output rectifiers, and also cause nuisance shutdown failures when the starting surge trips the overcurrent protection circuitry. Slowly increasing I_{LIMIT} will slowly increase the output current and output voltage. This characteristic will significantly reduce the peak power stress on the output rectifier and improve the demonstrated reliability of the power supply.

The PWR-SMP260 soft start circuit is shown in Figure 16. Soft-start is initiated when V_{S1} is in regulation. The soft-start time is controlled by the oscillator frequency. The first twelve bits of a fifteen-bit counter set the soft-start time of 4,096 power supply equivalent cycles. I_{LIMIT} is controlled by a five-bit digital to analog converter decoding the eithth through the twelveth bit of the counter chain. I_{LIMIT} will increase from zero to full-scale in 4096 cycles of the power supply. Note that the change in oscillator frequency for 50% duty cycle mode will not affect this timing. A digital implementation of soft-start was used because it is more stable and reliable, and requires no external timing capacitor.

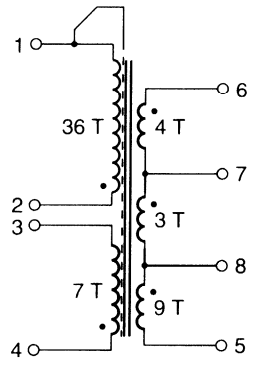
Upon completion of the soft-start time, the fault detection function is enabled. The fault detector monitors V_{BIAS}, which is related to the output voltage of the power supply. If a fault is not detected at the end of soft-start, the counting action of the counter chain is inhibited and the count is held at that point awaiting a fault. If an output overload occurs, the current limit will cause the output voltage (and consequently, V_{BIAS}) to decrease. If V_{BIAS} falls below the fault detector level, the power supply will be turned off, limiting the current delivered to the overload. The soft-start counter chain will then be enabled, keeping the power supply turned off for a measured period of time before allowing another restart attempt. The fault detection circuit will check to determime if the output overload has been removed after the automatic restart time. The last three bits of a fifteen bit counter set the automatic restart time of 28,672 power supply equivalent cycles.

One objective of the soft-start circuit is to limit the current delivered to the output capacitors. However, during start-up, the voltage on the output capacitors must be increased to the V_{BIAS} fault threshold before the end of the soft-start time or a fault will be detected and the power supply will be turned off, discharging the output capacitors. The effect on the power supply design is that the amount of capacitive stored energy in the output filters must be limited. The amount of capacitive stored energy is a function of the power level of the power supply, the V_{BIAS}-to-output turns ratio, and the power supply frequency.

Power-up is the time when most power supplies fail. The soft-start function reduces all of the power supply component peak stresses during the power up sequence. This will produce a power supply with a superior demonstrated reliability.

Output Voltage

The main (5 V) output is controlled by the feedback error amplifier circuit consisting of U2, U3, R13, R14, R15, R18, R19, R26 and C23. The 5 V output is scaled down by R13 and R14 and compared to a 2.5 V reference within U2. Any difference between the sampled 5 V output and the reference generates an error signal which is transmitted to the FEEDBACK pin (pin 7) of PWR-SMP260 through optocoupler U3. FEEDBACK is used by the control circuit to modify the duty cycle of the internal power switch, which in turn controls the output voltage of the supply. This technique enables the regulation on the 5 V output to be very precise. The 12 V output voltage is semi-regulated, and the regulation quality depends on several factors: output turns ratio, D6 forward voltage drop, the 5 V set point , and the value of R26.



CORE/BOBBIN #
FQK2522-T11-255-2500B2

PIN	FUNCTION
1	HIGH-VOLTAGE DC BUS
2	PWR-SMP DRAIN
3	PRIMARY-SIDE COMMON
4	V_{BIAS}
5	-12 V OUTPUT
6	+12 V OUTPUT
7	+5 V OUTPUT
8	RETURN

PI-726-032192

Figure 17. T1005 Schematic Diagram.

Output Transformer T1005

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies. T1005 is being submitted to TUV Rheinland for safety review in 240 VAC applications. The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Magnetics Design

The standard transformer schematic is shown in Figure 17. This design has a primary winding with 36 turns of 27 AWG magnet wire and a bias winding of 7 turns of 27 AWG magnet wire. The shield is 0.002" thick copper foil. The three output windings consist of three turns of 0.004" thick copper foil for the 5 V output, four turns of 21 AWG magnet wire for the 12 V output, and nine turns of 27 AWG magnet wire for the optional -12 V output. The transformer is margin wound to meet the voltage breakdown and safety requirements of Underwriters Laboratories and VDE. The nominal primary inductance is 330 µH. The maximum leakage inductance measured on the primary is 15 µH. Approximately 80% of the total leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 1 MHz. The resistance of the primary winding is 540 mΩ. The resistance of the 5 V secondary winding is 5 mΩ, and the resistance of the feedback winding is 370 mΩ.

Output Transformer T1005 (cont.)

The core is a LP22/13-style core. The core material is TDK "PC40" material or Tokin "2500B2". The A_L value is 255 nH/T^2.

The power transformer AC flux density at 30 watts and 130 kHz is 1325 gauss.

The primary saturation current at 100°C, 3800 gauss, is 2.8 amperes.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The minimum permissible inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.45}{2 \times 1.3 \times 10^5 \times (1.54 - 0.876)} = 248\mu H$$

where the peak switch current is less than the specification sheet typical current with V_{DS} of 10 V and the minimum current limit current. The maximum recommended value of peak switch current for continuous operation is 2.5 A. The primary inductance calculations for the PWR-SMP260 with 30 watts output show an inductance of 248 µH. The efficiency of the PWR-SMP260 at 30 watts and 100 VDC is 76%. The input power will be 39.4 W (30 W divided by 0.76). The average input current at 100 VDC will be 0.394 A (39.4 W divided by 100 V). The average on time current with a 45% duty cycle is 0.876 A (0.394 A divided by 0.45). The minimum permissible primary inductance L_P equals 248 µH. The nominal primary inductance of the T1005 is 330 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds/turn = 0).

$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.45}{(1 - 0.45)} \times \frac{115 - 5}{5 + 0.5} = 16.4$$

Other Output Voltages

The standard transformer as shown in Figure 17 can be modified for output voltages other than 5 and 12 volts. This is achieved by changing the secondary winding turns ratios. For example, the 12 V output can be changed to 15 V by changing the total turns in that winding from 7 to 9. The output voltage can be fine-tuned by adjusting the R13, R14 voltage divider. Traces for an additional linear regulated negative auxiliary output are included on the PWR-EVAL7 printed circuit board. The T1005 standard power transformer comes with an additional auxiliary winding capable of 15 V and 0.5 A. With the addition of a few components, a fully-regulated -12 V, 0.5 A output can be added to the supply. The schematic for this optional output is shown in Figure 18.

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C15 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C15 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1 and the series resistor R9.

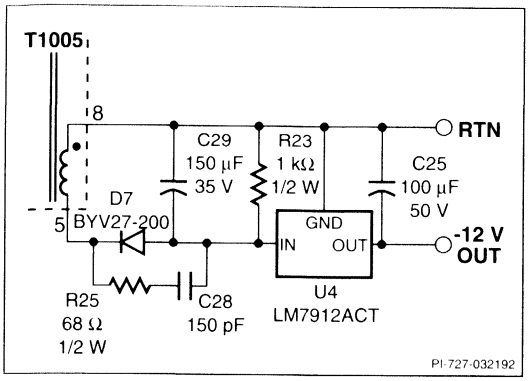


Figure 18. Optional -12 V Output Schematic Diagram.

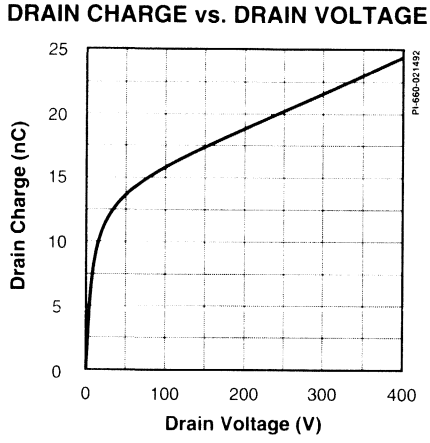


Figure 19.

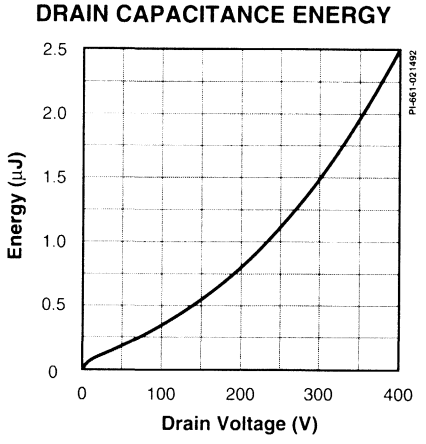


Figure 20.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package and heat sink, the ambient temperature[4], and the peak switching transistor current limit circuit.

Thermal Characteristics

The PWR-SMP260WTC is packaged in a 23-pin power SIP package[5]. The thermal impedance from junction to ambient and from junction to case are 41°C/Watt and 7.2°C/Watt respectively. In order to exploit the full power capability of this package, an external heat sink is required. The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and transformer and damping network capacitances[6], and the losses in the pre-regulator when it is active. Figure 19 gives the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 20. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this figure to determine the total AC losses in the circuit. Additional information on thermal management is available in AN-9.

Current Limit

Since the PWR-SMP260 control IC utilizes current mode control, cycle by cycle current limit protection occurrs as a natural consequence of the design, and requires no additional circuitry. Maximum peak current is set by the values of R2 and R11. R11, in conjunction with a 480 uA current source internal to U1, sets the maximum reference voltage for the current comparator. Peak primary current is sensed by R11. Maximum peak current is determined by the equation:

$$I_{pk} = \frac{R2}{R11} \times (480\mu A - 2 \times I_{FF})$$

where I_{FF} is the feedforward compensation current. As supplied, the PWR-EVAL7 does not use feedforward compensation, so the I_{FF} term will normally be zero. However, if feedforward is used, the I_{FF} term should be taken into account when selecting R2 and R11. When choosing values for R2 and R11, two factors should be considered. The current comparator reference voltage set by R2 should be reasonably large to provide noise immunity. However, if it is set too high, power dissipation across R11 will be excessive at the current limt point. The value of R2 used in the EVAL7 demonstration circuit (1.6 kΩ) sets the maximum current compararator reference to 770 mV. Since R11 is set at

3

500 mΩ, the maximum peak current is set at 1.54 A. Given the waveshape and duty cycle of the primary current, the maximum RMS current through R11 is about 800 mA, which yields a power dissipation of 300 mW at the current limit point, which is adequate derating for R11 at the current limit point.

The PWR-SMP260 control circuit blanks the first 100-200 ns of the signal from the current sense resistor. This feature helps to eliminate spurious termination of the switching cycle caused by output rectifier reverse recovery spikes. In conventional current-mode circuits this leading edge spike is usually suppressed by filtering the current sense signal. This can add substantially to the delay time in the current feedback loop, which increases the minimum on time of the switching cycle. This can cause problems at high line and during fault conditions, especially at a high operating frequency. The PWR-SMP260 does not require passive filtering for the blanking function, and the overall speed of the current sense loop is not affected.

The effect of current limit on the output voltage can be seen in Figure 21. The shape of the current limit function is fairly close to a constant power curve. This is because the circuit regulates the peak current in the transformer primary, providing a constant energy delivery to the core during current limit. Since the power supply operates at a constant frequency, constant power is delivered in current limit.

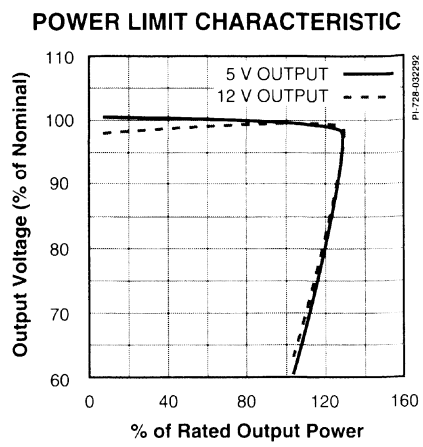


Figure 21.

Operating Frequency

The operating frequency of the PWR-EVAL7 is typically 130 kHz. The frequency of operation is adjustable by varying the timing capacitor C11 connected to pin 3 of U1. The nominal output operating frequency can be estimated with the following formula:

$$f = \frac{127 \times 10^{-6}}{C_{EXT}(\text{in pF})}$$

Where f is the frequency expressed in kilohertz, and C_{EXT} is expressed in pF. Note that the oscillator of the PWR-SMP260 will run twice as fast as the output due to the internal frequency divider in the 50% maximum duty cycle mode. If the 90% duty cycle mode is selected, the internal frequency divider is disabled, and the output frequency will be identical to the oscillator frequency. The nominal oscillator frequency with C_{EXT} = 470 pF is 270 kHz. The PWR-EVAL7 printed circuit board includes circuit traces for a transformer-coupled synchronization option. This circuit, when populated, allows the frequency of the power supply to be synchronized to a external TTL-level source. The schematic diagram for this option is shown in Figure **22**. The secondary turns should be wound on one-third of the circumfrence of the toroid. The primary turns should then be spaced evenly around the entire circumfrence. "Start" and "finish" of the primary should be on opposite sides of the core from the "start" and "finish" of the secondary.

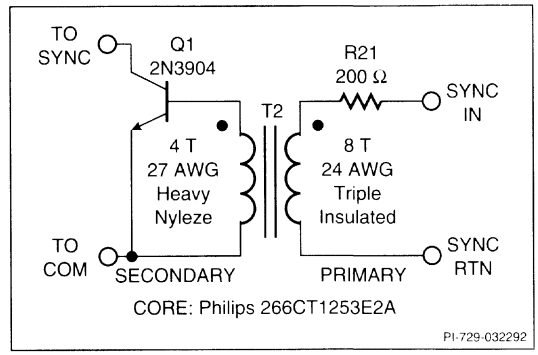


Figure 22. Optional External Synchronization Circuit.

A transfomer approach was chosen over an optically-coupled approach because affordable optocouplers lack the required speed to run properly at the operating frequency of the PWR-EVAL7. In practice, the nominal operating frequency of the oscillator should be set about 10% below the synchronizing frequency to allow the oscillator to lock in properly to the external source. Pulse width of the synchronizing signal should be at least 100 ns to allow the synchronizing transformer and transistor time to turn on. Pulse width into Pin 6 of U1 should be limited to 1 µs or less to avoid activating the ON/OFF function of the IC. The ON/OFF function will shut down the output and trigger the soft start sequence. Transistor Q1 has a storage and fall time of about 500 ns as used in the synchronizing circuit. This time should be considered when determining the maximum pulse width for the synchronization signal.

Remote Inhibit

The SYNC pin of the PWR-SMP260 can also be used to implement a remote inhibit function. If Pin 6 is pulled down to analog common for more than 10 µs, the power supply will shut down. If this pin is held down, the power supply will remain off indefinitely. Releasing Pin 6 allows the controller to initiate a soft-start cycle and restart the supply. Circuit traces are provided on the PWR-EVAL7 to allow implementation of an optically-coupled remote inhibit circuit. Isolation of the inhibit circuit is required because the control IC is on the primary side of the power supply. A schematic diagram for the inhibit circuit is provided in Figure **23**. The inhibit circuit is activated by a TTL-level "high" signal.

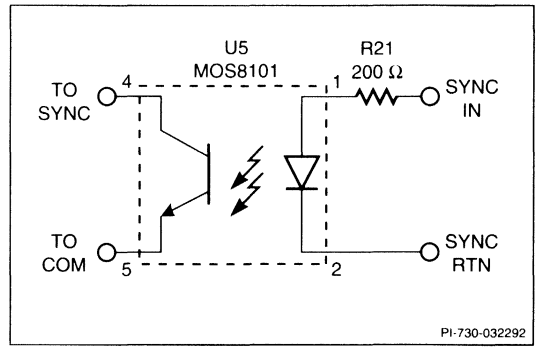


Figure 23. Optional External Inhibit Circuit.

Maximum Duty Cycle Select

The PWR-EVAL7 is configured for a maximum duty cycle of 50%. In most circumstances, this is an optimum value for use in a universal input flyback power supply, allowing sufficient dynamic range to comfortably cover the entire input voltage swing. Also, limiting the input duty cycle range allows the use of current-mode control without the danger of current-mode oscillation. To select a 50% maximum duty cycle, SLOPE COMP (pin 4) of the PWR-SMP260 is tied to V_{S1}/V_{S2} (Pins 10 and 11).

If a wider duty cycle range is required, SLOPE COMP can be connected through a resistor to COM. This sets the maximum duty cycle to 90%, and the value of the resistor sets the amount of slope compensation provided. This modification can be done by removing JMP1 and inserting resistor R1. If the wide duty cycle option is selected, slope compensation should be employed to prevent current-mode oscillation. The amount of slope compensation is determined by R1, and is inversely proportional to its value. The installed value of R1 is 36 kΩ. The range of values for R1 can be from 7 to 36 kΩ. Refer to AN-11 for a more detailed description of current mode control theory and criteria for selecting current mode compensation components.

Control Loop

The PWR-SMP260WTC utilizes current-mode control[7]. Current mode control uses the signal from the output voltage error amplifier to set the threshold of a comparator which monitors the peak current in the primary power switch. This comparator turns off the output switch when the peak current exceeds the level set by the error amplifier. The error amplifier signal is used to program the cycle-by-cycle peak current in the primary switch. This has several advantages in terms of power supply operation. First, since the peak primary switch current is controlled by the error amplifier, current limit protection is inherently provided. Additionally, since a peak current level is programmed by the error signal instead of a fixed duty cycle, open loop correction for input ripple is obtained, greatly reducing the demand on the output error amplifier. Lastly, current mode control transforms the power supply into a controlled current source. This effectively eliminates one of the poles in the output filter transfer function, making the power supply easier to stabilize. The PWR-EVAL7 uses the PWR-SMP260 control circuit to construct a current-mode controlled flyback power supply designed to operate in the continuous current mode. The DC input to output voltage transfer function for a flyback supply when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[8]. The duty cycle is controlled by the output voltage error amplifier, which sets the cycle by cycle peak current in the primary power switch. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[9,10,11] is included in the documentation disk. T1, U1, U2, U3, R2, R11, R13, R14, R15, R18, R26, C2, C14, C23, C24, C26, and C30 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The coefficients of the small-signal pulse width modulator transfer function generators are calculated by knowing the transformer inductance, the duty cycle of the operating point of interest, the switching period, the current sense resistor, and the on-time slope of the current sense waveform.

The input voltage feedforward gain is:

$$k_f = \frac{-D \times T_S \times R_i}{L} \times \left(1 - \frac{D}{2}\right)$$

The output voltage feedback gain is:

$$k_r = \frac{(1-D)^2 \times T_S \times R_i}{2L}$$

The modulator gain is:

$$F_m = \frac{1}{(S_n + S_e) \times T_S}$$

D is the duty cycle at the operating voltage of intrest. T_S is the switching time, which is equal to the reciprocal of the operating frequency. L is the primary inductance of the power transformer, and R_i is the value of the current sense resistor. S_n is the slope of the inductor current waveform, equal to L/V_{in}, where V_{in} is the voltage across the transformer primary during the on time of the switching cycle. S_e is the slope of the slope compensation ramp. If no slope compensation is used, this value is zero. The measured open loop gain/phase response curve for 120 V_{RMS} input (solid lines) and 240 V_{RMS} input (dashed lines) are shown in Figure 24. The 120 V_{RMS} input control loop has 76° phase margin, an open loop unity gain crossover frequency of 1.4 kHz, and 21 dB gain margin at 10 kHz with a 30 W load. The 2430 V_{RMS} input control loop has 50° phase margin, an open loop unity gain crossover frequency of 3.1 kHz, and 15 dB gain margin at 10 kHz with a 30 W load.

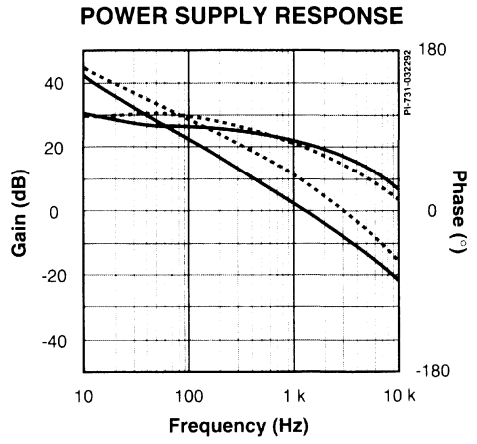


Figure 24.

The output load transient response can also be used to provide an indication of power supply control loop stability. Because this test exercises the loop in the large signal domain by forcing it to slew, it is useful in uncovering areas of marginal or conditional stability. Figure 25 gives the load transient response of the 5 V output of the PWR-EVAL7 for a 75%-100%-75% repetitive load step. The 12 V output was loaded at 1.5 A, and the input voltage was set to 162 VDC. The initial transient recovers in about 100 µs for a 25% load step. The pedestal portion of the waveform is due to the finite load regulation of the 5 V output. The slight ringing is due to the second LC output filter on the 5 V output.

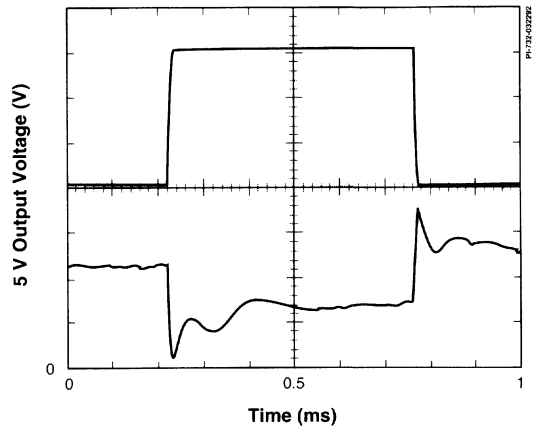


Figure 25. Transient Response.

Protection Features

Overtemperature

The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 140°C and keeps it off until the junction temperature decreases 45°C[12].

Test Mode

The I_{LIMIT} input (pin 9) controls the built-in test logic of the integrated circuit. The test logic turns on the power transistor continuously when the voltage on pin 9 is equal to the pin 10 & 11 voltage (5.8 V) ±1.5 V. Do not put the PWR-EVAL7 into test mode while operating in a power supply circuit as this could destroy the PWR-SMP260.

Control Circuit Undervoltage Protection

The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is the regulation voltage of the V_S regulator.

Input Filtering and Rectification

BR1 and C1 perform the input rectification and filtering function. The rectifier bridge should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage rating on C1 is equal to the peak value of the maximum rectified input voltage, 200 V for 120 VAC and 400 V for 240 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitor C1 can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage provided to a regulated output voltage at maximum power, and the minimum AC input voltage[13]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 when the input bridge stops conducting, and V_2 is the voltage on C1 when the input bridge starts conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the minimum input capacitor value for both 120 VAC and universal input voltage ranges.

Input Surge Current

When mains voltage is applied to the power supply, a surge of current flows into the input to charge the input storage capacitor C1[14]. The magnitude of current must be within the surge ratings of the power switch, fuse, EMI filter, and input rectifiers. The surge current is limited by the resistance of the input surge limiting thermistor R20. This device is a negative temperature coefficient thermistor with a room temperature resistance value of 10 Ω. The thermistor initially presents this value of resistance to the AC line when the power supply is first turned on, limiting the input inrush current to a maximum value of 37 A. After limiting the initial surge current, the thermistor heats up and assumes a low value of resistance, allowing the supply to operate without undue power loss.

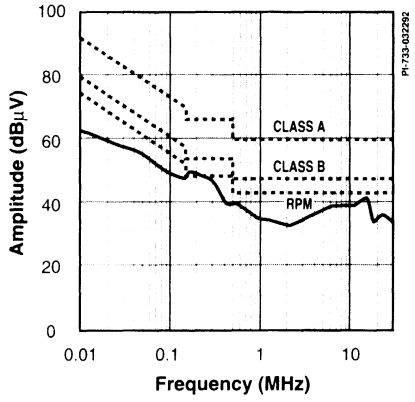


Figure 26. EMI Plot of the PWR-EVAL7.

EMI Considerations

This power supply was designed to meet worldwide EMI (DIN VDE 0805/05.90) and safety (UL1950 and IEC950) specifications. Figure 26 is a plot of the maximum conducted EMI relative to the VDE specification limits. Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L1, L3, and C6 filter differential-mode conducted emissions.

Common Mode Filter
L2, L6, C7, C8, C12, and C20 filter common-mode conducted emission currents[15]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C20 couples high-frequency noise back to the system chassis ground. C7, C8, and C12 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP260. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L6 in series with the ground lead of the power connector is a "lossy" bead and is equal to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

Safety Agency Requirements

The PWR-EVAL7 has been submitted to TUV Rhein Land for evaluation per IEC 950.

Additional information on safety and layout-related issues is available in DA-2.

Documentation Disks

The PWR-EVAL7 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL7 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README7.BAT	(This file) contains a summary and last minute information on PWR-EVAL7
PWB1006B.APR	Aperture file with assigned D-codes
EVAL7.BOM	Bill of Materials file
EVAL7ASY.DWG	Assembly drawing file
FAB1006B.DWG	Fabrication drawing for the PC board
1006BCL.G23	Copper layers gerber file
1006BSM.G23	Solder mask layers gerber file
1006BSKP.G23	Silkscreen and padmaster gerber file
EVAL7.LIB	Library file of the part symbols used in both schematics
PWB1006B.NCD	NC drill file for computerized drilling of the PCB
EVAL7.SCH	Schematic file of PWR-EVAL7
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES7.TXT	Functional description of the power supply circuitry used in PWR-EVAL7
ICDESC2.TXT	Functional description of the PWR-SMP260 integrated circuit used in PWR-EVAL7
EVL7COST.TXT	Estimated parts cost
T1005 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD 286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README7.BAT and the EVAL7.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP260.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

References

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3 Kamm, Edith "New Military EMI Specifications Affecting the Input Circuit Architecture of AC to DC Converters" Proceedings, Eighth National Solid-State Power Electronics Conference (Powercon 8), April 1981, C.3.1-C.3.11

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11 Ridley, R.B. "A New, Continuous-Time Model for Current-Mode Control", Modeling, Analysis, and Design of PWM Converters , Dr. Fred C. Lee, ed., Virginia Power Electronics Center, 1990, pp 321-331

12 Thermal Shutdown Application notes: National Semiconductor AN-82, AN-103

13 Tartar, Ralph E., Principles of Solid-state Power Conversion Howard W. Sams & Co., Inc., 1985, p. 232

14 Hirshberg, Walter "Optimizing Line Inrush Design in Off-Line Converters" Proceedings, Fifth National Solid-State Power Conversion Conference (Powercon 5), May 1978, E3.1-E3.7

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PWR-EVAL8

PWR-SMP240 Evaluation Board

110/220 VAC Input
Isolated 5/12 V, 20 W (Total) Output

POWER INTEGRATIONS, INC.®

Product Highlights

Isolated 5 V Output from 110/220 VAC Input
- Up to 20 watts of output power can be supplied
- Isolation is provided by transformer designed to UL/VDE specifications
- Layout has been designed for ease of evaluation and testing

Built-in Self-protection Circuits
- Input undervoltage lockout
- External current limit
- Thermal shutdown
- Soft-start
- Overload shutdown/auto-restart

Designed to Meet Regulatory Standards
- Layout designed to meet UL/CSA/VDE requirements
- Meets DIN VDE 0805/05.90 Level B

Description

The PWR-EVAL8 board has been designed to demonstrate circuit layout guidelines and to allow easy evaluation of the performance for the PWR-SMP240WTC power supply IC.

The PWR-SMP240, intended for off-line isolated power supply applications, combines a high-voltage power MOSFET switch, a current-mode power system controller, and an off-line bias regulator in a monolithic integrated circuit. High frequency operation reduces total power supply size. The PWR-SMP240 uses the integrated high-voltage pre-regulator to self-bias during power supply start-up.

The other key component of the design is the high-frequency output transformer. This item is available from several magnetics suppliers who are listed in this document. All other components used on the evaluation board are industry-standard devices.

Applications for the PWR-SMP240 include bias and keep-alive supplies, battery chargers, and small internal supplies for portable products in the commercial/industrial marketplace.

The PWR-EVAL8 evaluation board comes fully assembled and tested. Included with the board are 3.5 inch and 5.25 inch floppy disks containing Gerber file data of the printed circuit board for use with most photo plotting equipment.

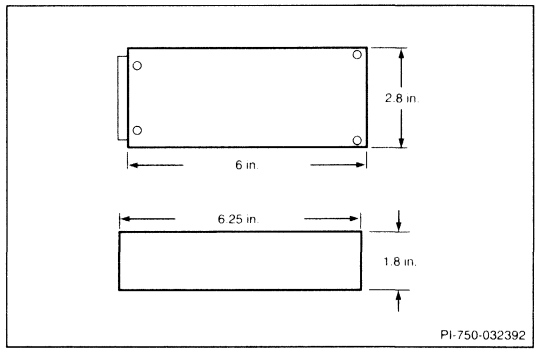

Figure 1. Evaluation Board Overall Physical Dimensions.

PARAMETER	LIMITS
Input Voltage Range	85 to 265 VAC
Input Frequency Range	47 to 440 Hz
5 V Output Voltage Range Load Current Range	 4.5 to 5.5 VDC 0 to 2 A
12 V Output Voltage Range Load Current Range	 10.8 to 13.2 VDC 0 to 1.2 A
Temperature Range	0 to 70°C
Efficiency	> 77%

Figure 2. Table of Key Electrical Parameters.

ORDERING INFORMATION	
PART NUMBER	OPERATING VOLTAGE
PWR-EVAL8	110/220 VAC INPUT 5/12 VDC OUTPUT @ 20 W

3

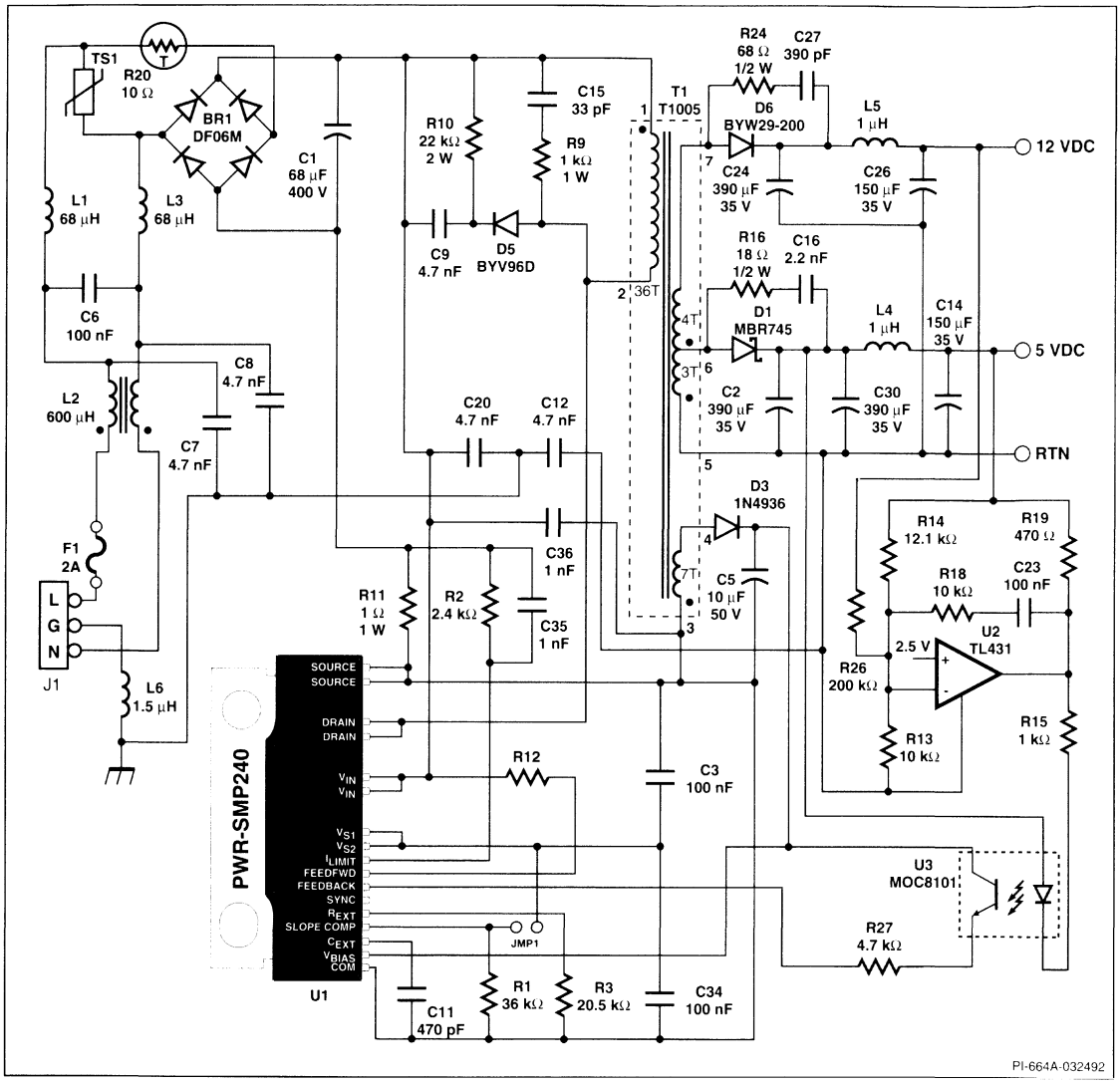

Figure 3. Schematic Diagram of the PWR-EVAL8 Power Supply.

General Circuit Description

The PWR-EVAL8 is an isolated Buck-Boost (flyback) switching power supply[1] topology. The power supply is implemented using the PWR-SMP240WTC integrated circuit. The power supply circuit operates by alternately storing energy in the transformer core and releasing it to the output.

The flyback power supply circuit shown in Figure 3, when operated with the T1005 standard transformer (see DA-3), will produce a dual output 20 watt power supply that will operate from 85 to 265 VAC input voltage. The PWR-EVAL8 has a fully regulated 5 V output and a semi-regulated 12 V auxiliary output. The output voltages are selected by the turns ratios of the T1 output windings and the voltage divider formed by resistors R13, R14, and R26.

Component Listing

Reference	Value	Part Number	Typical Manufacturer
C1	68 µF, 400 V	LGQ2G680MHSZ	Nichicon
C2, C24, C30	390 µF, 35 V	UPL1V391MPH	Nichicon
C3, C23, C34	100 nF, 50 V	K104Z20Z5UFVBWN	Philips
C5	10 µF, 50 V	UVZ1H100MDH	Nichicon
C6	100 nF, 250 VAC	F1772-410-2000	Roederstein
C7, C8, C12, C20	4.7 nF, 250VAC	F1710-247-1000	Roederstein
C9	4.7 nF, 1 kV	D472M47Z5UNAAEM	Philips
C11	470 pF, 50 V	K471J15C0GFVBWA	Philips
C14, C26	150 µF, 35 V	UPL1V151MPH	Nichicon
C15	33 pF, 1 kV	D330K29S2LNAAAL	Philips
C16	2.2 nF	D22M39Z5UNAAEM	Philips
C27	390 pF, 1 kV	D391K20Z5FNAAEM	Philips
C36	1 nF, 1 kV	D102P29Z5UNAAEM	Philips
C35	1 nF, 50 V	K102M15X7RFVBWA	Philips
BR1		DF06M	General Instruments
D1		MBR745	Motorola
D3		1N4936	Motorola
D5		BYV96D	Philips
D6		BYW29-200	Philips
F1	2 A , 250 VAC	230.002	Littelfuse
L1, L3	68 µH	SN8D-500	Tokin
L2	600 µH	SU10V-20006	Tokin
L4, L5	1 µH	RL-1160-1.0	Renco
L6	BEAD	2673200201	Fair-Rite
R1	36 kΩ	5043CX36K00J	Philips
R2	2.4 kΩ	5043CX2K400J	Philips
R3	20.5 kΩ, 1%	5043EM20K50F	Philips
R10	22 kΩ, 2 W	MO-2 223J	Koa/Speer
R11	1 Ω, 1 W	RSS-1 1ROJ	Koa/Speer
R13	10 kΩ, 1%	5043EM10K00F	Philips
R14	12.1 kΩ, 1%	5043EM12K10F	Philips
R15	1 kΩ	5043CX1K000J	Philips
R16	18 Ω, 1/2 W	5053CX18R00J	Philips
R18	10 kΩ	5043CX10K00J	Philips
R19	470 Ω	5043CX470R0J	Mepco
R20	10 Ω - Thermistor	SG220	Ketema
R24	68, 1/2 W	5053CX68R00J	Philips
R26	200 kΩ, 1%	5043EM200K0F	Philips
R27	4.7 kΩ	5043CX004K7J	Philips
TS1		V275LA20A	Harris
U1		PWR-SMP240WTC	Power Integrations
U2		TL431CLP	Motorola
U3		MOC8101	Motorola
T1		T1005	Custom*
HS1		6263	Thermalloy
HS2,HS3		6225	Thermalloy
JMP1		22 AWG	Bus Wire
J1	Plug Socket	EAC-303	Switchcraft
	PC Board	ASSY 1007-A	Custom**

Figure 4. Parts List for the PWR-EVAL8

Component Listing (cont.)

Reference	Value	Part Number	Typical Manufacturer

Custom Components:

* Qualified manufacturers are:

AT&T Microelectronics	(800) 372-2447	FAX: (214) 284-8282
Datatronics	(714) 928-7731	FAX: (714) 928-7701
Delta (Taiwan)	(02) 7164822	FAX: (02) 7169764
Inductor Supply	(714) 978-2277	FAX: (714) 978-2411
Renco Electronics	(800) 645-5828	FAX: (516) 586-5562
Tokin (Japan)	(03) 402-6166	FAX: (03) 497-9756

** Manufacturer is:

CBR Circuits
116 Minnis Court
Milpitas, CA 95035
(408) 946-3446

Figure 4. Parts List for the PWR-EVAL8

The circuit groups in the schematic Figure 3 are as follows. L1, L2, L3, L6, C6, C7, C8, C12, and C20 form the EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold up time. D5, C9 and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the leakage inductance ringing voltage. The damping network improves the EMI performance of the supply. R2, R11, R14, R18, R26, C2, C14, C23, C24, C26, C30, and T1 determine the control loop frequency response. R3 sets the current sources within the PWR-SMP240. C11 sets the switching frequency of the power supply. C3, C5,C34, C35, and C36 are bypass capacitors. C3 supplies the pulsed current required to charge the gate of the output power FET when it is turned on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. R2 and R11 form the cycle-by cycle current limit and current mode control circuitry. R11 senses the primary current, and R2 is used to set the current sense comparator reference voltage. R1 can be used to set the amount of slope compensation current flowing in the current-mode control circuit.. R12 is an optional

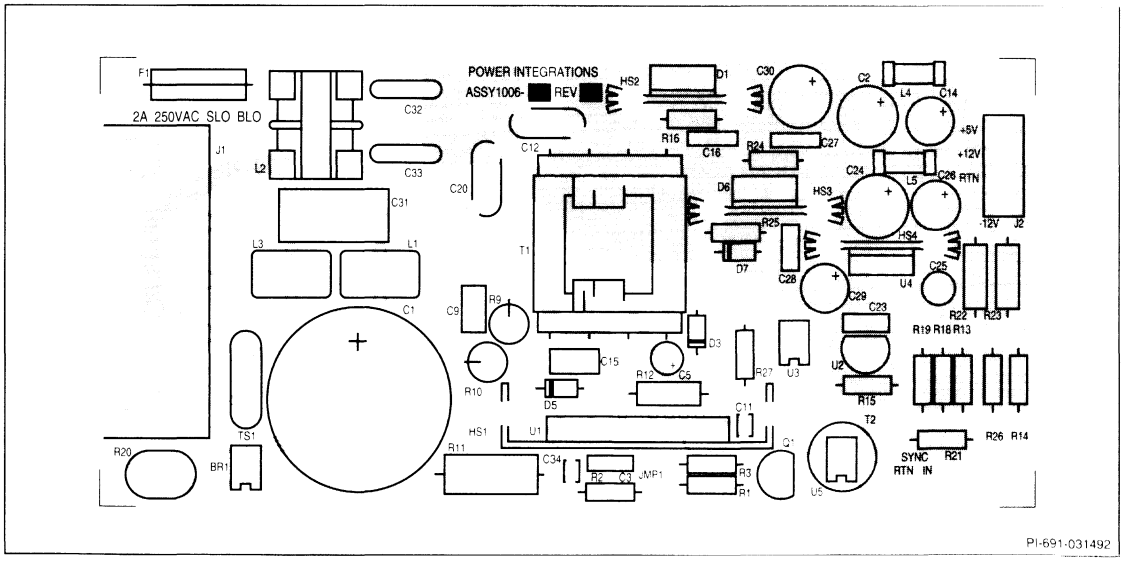

Figure 5. Component Legend of the PWR-EVAL8.

feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. D1, C2, C14, C30, and L6 rectify and filter the 5 V output. R16 and C16 damp the ringing caused by the reverse recovery of D1. D6, C24, C26, and L6 rectify and filter the 12 V output. R24 and C27 damp the ringing caused by the reverse recovery of D6. U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13, R14 and R26 form a voltage divider that sets the output voltages of the supply. R27 limits the AC current coupled from the V_{BIAS} supply through optocoupler U3.

The PWR-EVAL8 printed circuit board has circuit traces for several optional features which can be implemented by adding additional components. These include a linear-regulated -12V auxiliary output, transformer coupled external frequency synchonization, and an optically-coupled remote inhibit function.

Input and Output Characteristics

Figure 2 gives the basic DC performance characteristics of the power supply. The circuit performance data shown in Figures 6-10 were measured by applying a DC input voltage to the PWR-EVAL8.

Load Regulation (Figures 6 and 7) - The amount of output voltage change for a change in output current is referred to as load regulation. The 5 V output changes less than 2% for a 10% to 100% load current range. The 12 V output changes less than 7.5% for a 10% to 100% load change. Below 10% of rated load, the 12 V output rises due to the leakage inductance between the secondaries of the transformer[12]. This rise becomes progressively more severe as the 5 V load is increased. To help combat this trend, R26 was added to the error amp circuit. This resistor samples a portion of the 12 V output voltage and adds it to the 5 V voltage divider. Thus, a rise in the 12 V output will cause the control circuit to scale back both the 5 V and 12 V outputs slightly. This improves the 12 V regulation, but deteriorates the 5 V regulation by about 1%. The 12 V regulation can be further tightened by decreasing the value of R26, at the expense of 5 V regulation. Decreasing R26 will also decrease the nominal 5 V output voltage. This value can be trimmed by increasing the value of R14, or by reducing the value of R13. If extremely tight regulation is required on both outputs, a post-regulator can be added to the 12 V output, making the two outputs essentially independent of one another. The disadvantages of this approach are increased parts count and reduced efficiency.

Line Regulation - The change of output voltage for a change in input voltage is called line regulation. The maximum change in output voltage from 100 to 400 VDC input, for both outputs, is 0.5% for an input voltage change of 100 V(rms) or 50 ppm/V(rms).

Load and Line Efficiency (Figures 8 and 9) - Efficiency is the ratio of output power to input power. These graphs show how the efficiency changes with load current and input voltage. This data is used in the first-cut transformer design procedure. Efficiency at full load and nominal line voltage is 78%. Full load is defined as a 1.6 A load on the 5 V output and a 1.0 A load on the 12 V output, for a total output power of 20 W. The ratio of 5 V power to 12 V power was held constant for the load efficiency curve.

Temperature Performance (Figure 10) - The output power deliverable to the load decreases as the ambient temperature increases. This graph gives the typcial output power capability with a nominal input voltage.

Power Factor - Power Factor is the ratio of input power watts to the product of input voltage and input current[13]. The power factor of the PWR-EVAL8 with a 20 W load is approximately 0.6 at a input voltage of 115VAC.

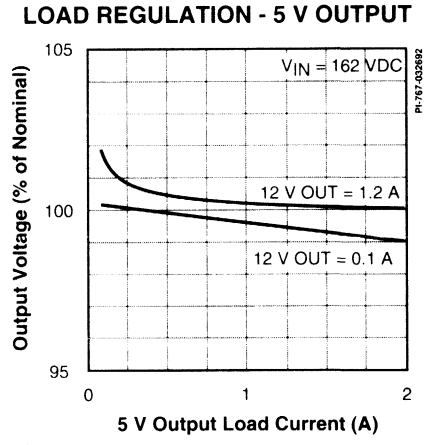

Figure 6.

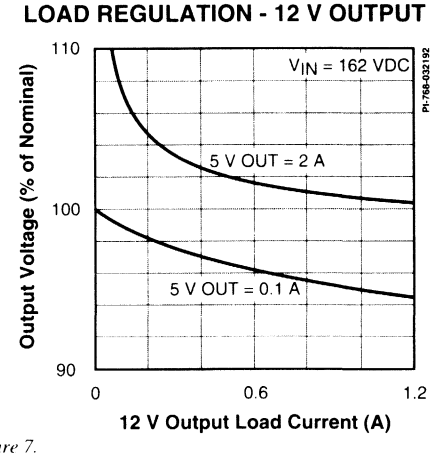

Figure 7.

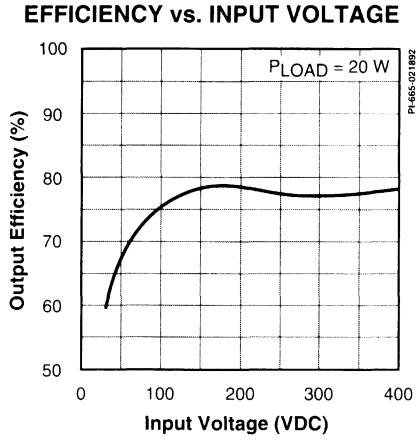

Figure 8.

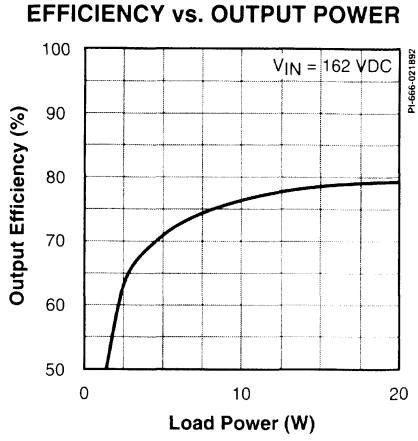

Figure 9.

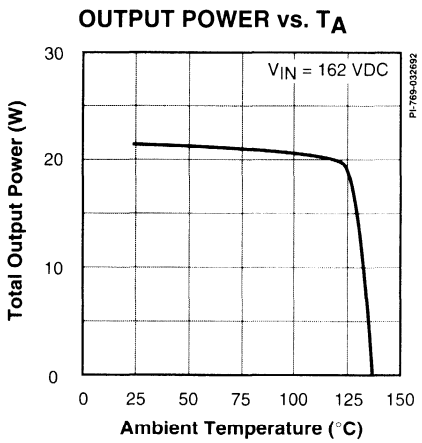

Figure 10.

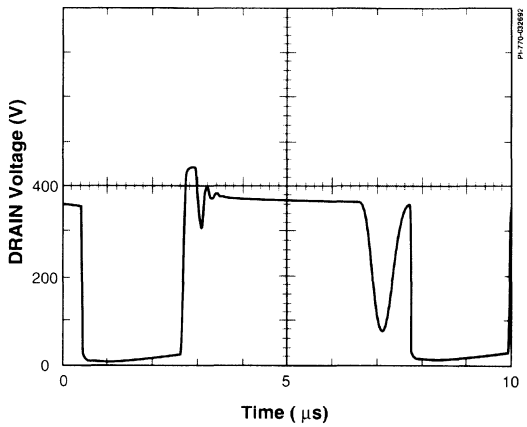

Figure 11. Drain-source Voltage of the PWR-SMP240.

Circuit Operation and Waveforms

The drain-source voltage and current waveforms are shown in Figures 11 and 12. The voltage waveform provides a wealth of information on how well the circuit is operating. The rise and fall times of the switch, the operating frequency, the effectiveness of the drain voltage clamping and damping networks can be observed. The minimum regulation voltage can be detected by observing the drain voltage waveform in conjunction with the input voltage. When the duty cycle of the switch reaches maximum, the minimum input voltage for regulation and output ripple has been reached. Note that this voltage is a strong function of output power. The effective storage time of the output rectifier can be determined by observing the delay between the falling edge of the drain waveform and the anode voltage on the output rectifier as shown in Figure 13.

Figure 13(a) is the drain waveform. Figure 13(b) is the anode of D2 when D2 is a BYW29-200 diode. Figure 13(c) is the anode of D2 when D2 is a MUR820 diode. The BYW29-200 is rated at 200 V with a reverse recovery time of less than 25 ns. The MUR820 is rated at the same voltage with a reverse recovery time of 60 ns. The BYW29-200 exhibits a recovery time of approximately 26 ns in the circuit, providing good functionality. However, the MUR820 exhibits a 48 ns recovery time in the circuit. This length of recovery time does not work well in the circuit, as evidenced by the large value of undershoot on the voltage waveform.

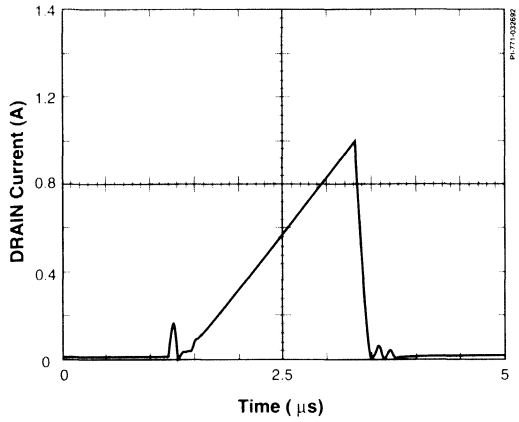

Figure 12. Drain Current of the PWR-SMP240.

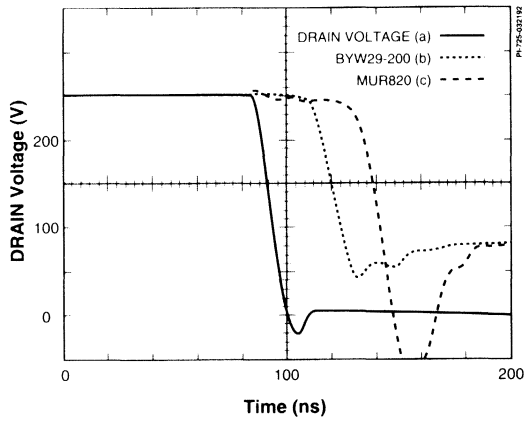

Figure 13. Recovery Times of Output Rectifier Diodes.

Bias Supplies

The pre-regulator, a high voltage linear regulator, provides the initial bias current when power is first applied. This regulator maintains the voltage on pins 10 and 11 at approximately 6 V. The bias regulator is turned off during normal operation to increase overall power supply efficiency and reduce power dissipation in the device. The voltage generated by the bias winding and filter provides bias current and turns off the pre-regulator when the power supply is operating.

Minimum Load

The PWR-SMP240 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. A shunt regulator is activated when the summing junction current falls below 12% of full scale. The shunt regulator will increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale. Figure 14 shows the load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The control loop gain path is shown in Figure 15. The gain of the minimum load regulator has been matched to the gain of the current mode switching regulator. This allows the control loop dynamics to remain the same whether the minimum load circuit is active or not active. This helps prevent degradation of the load transient response at light load.

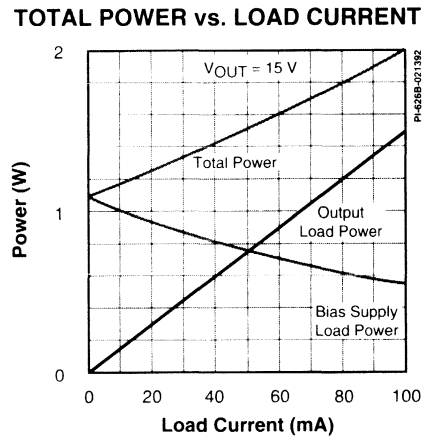

Figure 14. Minimum Load Transfer Characteristic.

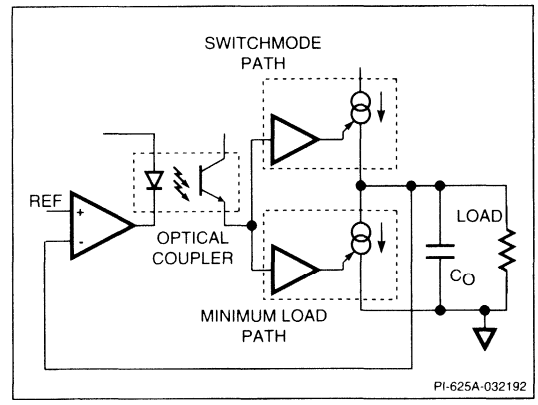

Figure 15. Control Loop Gain Path.

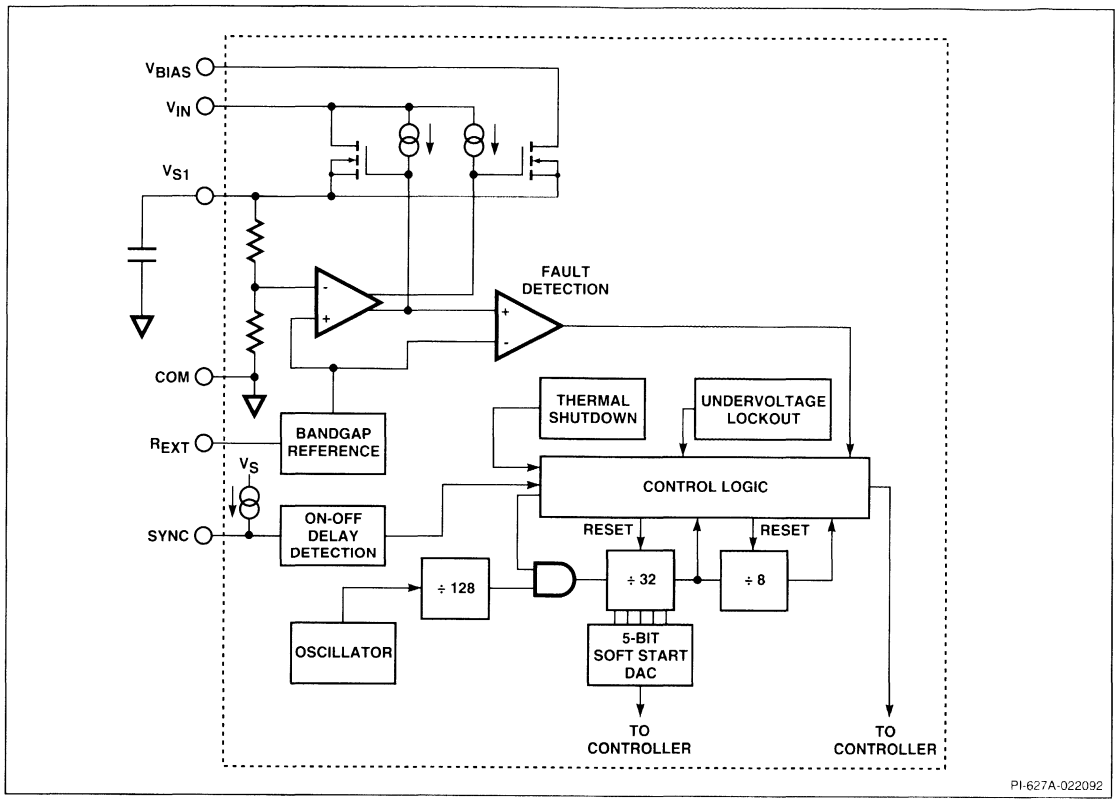

Figure 16. Soft-start section Functional Block Diagram.

Soft-Start

The soft-start function allows the power supply to start up in a controlled fashion. Flyback power supplies without soft-start will drive a large current into the output capacitors and load upon start-up, causing a peak power stress many times higher than the normal operating level. This power surge can unduly stress the power switch and output rectifiers, and also cause nuisance shutdown failures when the starting surge trips the overcurrent protection circuitry. Slowly increasing I_{LIMIT} will slowly increase the output current and output voltage. This characteristic will significantly reduce the peak power stress on the output rectifier and improve the demonstrated reliability of the power supply.

The PWR-SMP240 soft start circuit is shown in Figure 16. Soft-start is initiated when V_{S1} is in regulation. The soft-start time is controlled by the oscillator frequency. The first twelve bits of a fifteen-bit counter set the soft-start time of 4,096 power supply equivalent cycles. I_{LIMIT} is controlled by a five-bit digital to analog converter decoding the eithth through the twelveth bit of the counter chain. I_{LIMIT} will increase from zero to full-scale in 4096 cycles of the power supply. Note that the change in oscillator frequency for 50% duty cycle mode will not affect this timing. A digital implementation of soft-start was used because it is more stable and reliable, and requires no external timing capacitor.

Upon completion of the soft-start time, the fault detection function is enabled. The fault detector monitors V_{BIAS}, which is related to the output voltage of the power supply. If a fault is not detected at the end of soft-start, the counting action of the counter chain is inhibited and the count is held at that point awaiting a fault. If an output overload occurs, the current limit will cause the output voltage (and consequently, V_{BIAS}) to decrease. If V_{BIAS} falls below the fault detector level, the power supply will be turned off, limiting the current delivered to the overload. The soft-start counter chain will then be enabled, keeping the power supply turned off for a measured period of time before allowing another restart attempt. The fault detection circuit will check to determime if the output overload has been removed after the automatic restart time. The last three bits of a fifteen bit counter set the automatic restart time of 28,672 power supply equivalent cycles.

One objective of the soft-start circuit is to limit the current delivered to the output capacitors. However, during start-up, the voltage on the output capacitors must be increased to the V_{BIAS} fault threshold before the end of the soft-start time or a fault will be detected and the power supply will be turned off, discharging the output capacitors. The effect on the power supply design is that the amount of capacitive stored energy in the output filters must be limited. The amount of capacitive stored energy is a function of the power level of the power supply, the V_{BIAS}-to-output turns ratio, and the power supply frequency.

Power-up is the time when most power supplies fail. The soft-start function reduces all of the power supply component peak stresses during the power up sequence. This will produce a power supply with a superior demonstrated reliability.

Output Voltage

The main (5 V) output is controlled by the feedback error amplifier circuit consisting of U2, U3, R13, R14, R15, R18, R19, R26 and C23. The 5 V output is scaled down by R13 and R14 and compared to a 2.5 V reference within U2. Any difference between the sampled 5 V output and the reference generates an error signal which is transmitted to the FEEDBACK pin (pin 7) of PWR-SMP240 through optocoupler U3. FEEDBACK is used by the control circuit to modify the duty cycle of the internal power switch, which in turn controls the output voltage of the supply. This technique enables the regulation on the 5 V output to be very precise. The 12 V output voltage is semi-regulated, and the regulation quality depends on several factors: output turns ratio, D6 forward voltage drop, the 5 V set point , and the value of R26.

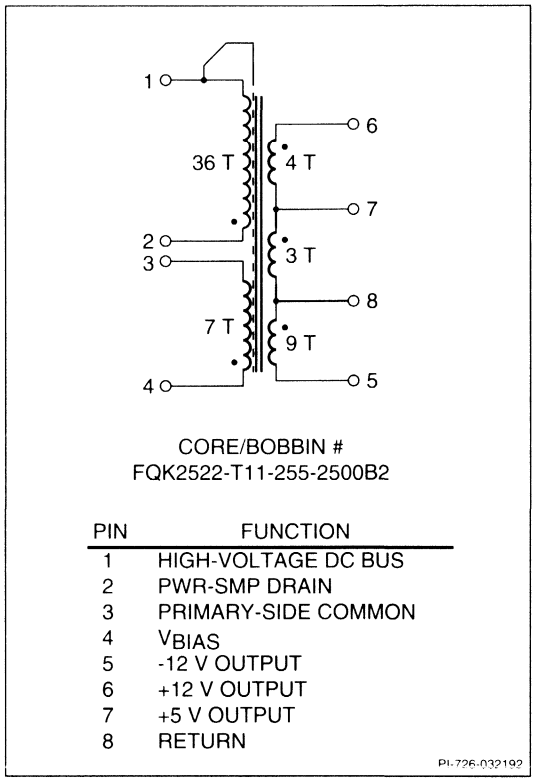

Figure 17. T1005 Schematic Diagram.

Output Transformer T1005

Transformer Specifications

Power Integrations has designed a series of power transformers for use with its products. The transformers are designed for small size and high frequency operation while meeting the requirements of applicable safety agencies. T1005 is being submitted to TUV Rheinland for safety review in 240 VAC applications. The list of manufacturers who have successfully passed the qualification process for standard transformers by Power Integrations is given in Figure 4. These vendors are aware of all of the unique requirements for design and manufacture of transformers for use with the PWR-SMP series of monolithic integrated circuits available from Power Integrations.

Magnetics Design

The standard transformer schematic is shown in Figure 17. This design has a primary winding with 36 turns of 27 AWG magnet wire and a bias winding of 7 turns of 27 AWG magnet wire. The shield is 0.002" thick copper foil. The three output windings consist of three turns of 0.004" thick copper foil for the 5 V output, four turns of 21 AWG magnet wire for the 12 V output, and nine turns of 27 AWG magnet wire for the optional -12 V output. The transformer is margin wound to meet the voltage breakdown and safety requirements of Underwriters Laboratories and VDE. The nominal primary inductance is 330 µH. The maximum leakage inductance measured on the primary is 15 µH. Approximately 80% of the total leakage inductance is due to the leakage inductance of the secondary winding.

The minimum acceptable resonant frequency is 1 MHz. The resistance of the primary winding is 540 mΩ. The resistance of the 5 V secondary winding is 5 mΩ, and the resistance of the feedback winding is 370 mΩ.

3

Output Transformer T1005 (cont.)

The core is a LP22/13-style core. The core material is TDK "PC40" material or Tokin "2500B2". The A_L value is 255 nH/T^2.

The power transformer AC flux density at 20 watts and 130 kHz is 1325 gauss.

The primary saturation current at 100°C, 3800 gauss, is 2.8 amperes.

First Try Transformer Design Example

The first estimation for the transformer design can be done with the help of the typical performance curves in the data sheet. The curves for efficiency are shown in Figures 8 and 9. Since many of the transformer design constraints occur at the minimum input voltage and maximum output power, this operating condition is where the transformer will be designed.

The primary inductance of the transformer can be obtained by the following procedure. First observe the typical efficiency of the demonstration power supply at the desired output power and input voltage from Figures 8 and 9. Calculate the input power by dividing the output power by the efficiency. Calculate the average input current by dividing the input power by the minimum DC input voltage on C1. Calculate the average current during the on time of the power switch by dividing the average input current by the maximum duty cycle for the frequency of operation from the data sheet. The minimum permissible inductance of the primary winding can be calculated by:

$$L_P = \frac{V_{in(min)} \times \text{Duty Cycle}}{2 \times f \times (I_{peak} - I_{avg})}$$

$$L_P = \frac{95 \times 0.45}{2 \times 1.3 \times 10^5 \times (1.15 - 0.584)} = 290\mu H$$

where the peak switch current is less than the specification sheet typical current with V_{DS} of 10 V and the minimum current limit current. The maximum recommended value of peak switch current for continuous operation is 1.5 A. The primary inductance calculations for the PWR-SMP240 with 20 watts output show an inductance of 290 µH. The efficiency of the PWR-SMP240 at 20 watts and 100 VDC is 76%. The input power will be 26.3 W (20 W divided by 0.76). The average input current at 100 VDC will be 0.263 A (26.3 W divided by 100 V). The average on time current with a 45% duty cycle is 0.584 A (0.263 A divided by 0.45). The minimum permissible primary inductance L_P equals 290 µH. The nominal primary inductance of the T1005 is 330 µH.

The primary-to-secondary turns ratio is dependent on the minimum DC input voltage, the average voltage drop across the conducting switching transistor, the average voltage across the conducting rectifier diode, the output voltage, and the maximum duty cycle. The turns ratio relationship is derived from the requirement that the sum of the voltage across a magnetic winding must equal zero over a period of operation (Sum of volts-seconds/turn = 0).

$$\frac{N_P}{N_S} = \frac{(V_{in} - V_{SW}) \times D \times t}{(V_O + V_d) \times (1 - D) \times t}$$

$$\frac{N_P}{N_S} = \frac{D}{(1 - D)} \times \frac{V_{in} - V_{SW}}{V_O + V_d}$$

$$\frac{N_P}{N_S} = \frac{0.45}{(1 - 0.45)} \times \frac{115 - 5}{5 + 0.5} = 16.4$$

Other Output Voltages

The standard transformer as shown in Figure 17 can be modified for output voltages other than 5 and 12 volts. This is achieved by changing the secondary winding turns ratios. For example, the 12 V output can be changed to 15 V by changing the total turns in that winding from 7 to 9. The output voltage can be fine-tuned by adjusting the R13, R14 voltage divider. Traces for an additional linear regulated negative auxiliary output are included on the PWR-EVAL8 printed circuit board. The T1005 standard power transformer comes with an additional auxiliary winding capable of 15 V and 0.5 A. With the addition of a few components, a fully-regulated -12 V, 0.5 A output can be added to the supply. The schematic for this optional output is shown in Figure 18.

Leakage Inductance Spike Voltage

The leakage inductance spike voltage seen on the primary winding when the power transistor turns off is proportional to the effective secondary leakage inductance of the transformer and the inductance of the output rectifier, capacitor loop and the current flowing in the primary winding when the switching transistor turns off. The ampere-turns stored in the primary winding when the transistor turns off will try to increase the current flowing in the output leakage inductance from zero to the stored ampere-turns in as short a time as possible. The voltage across the leakage inductance is limited by D5 and the voltage on C9, the primary peak voltage limiting network.

C15 and R9 form a damping network to reduce the ringing of the primary leakage inductance and capacitance. The value of C15 should be minimized as the energy stored in this capacitor is dissipated in the power switching transistor in U1 and the series resistor R9.

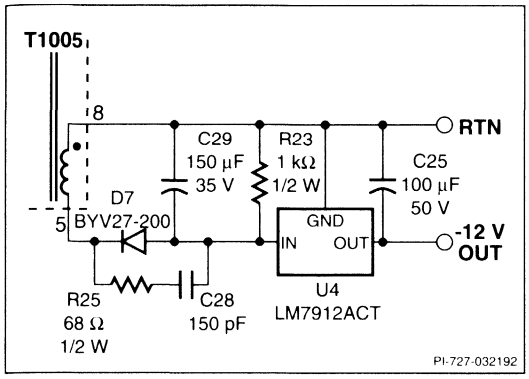

Figure 18. Optional -12 V Output Schematic Diagram.

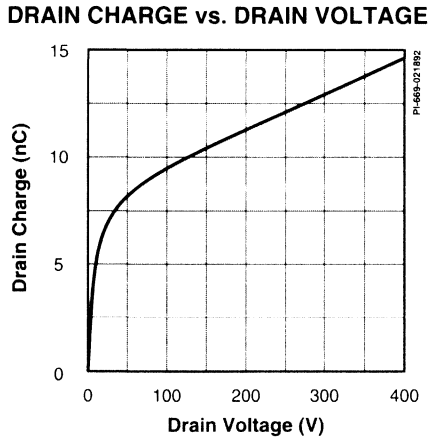

Figure 19.

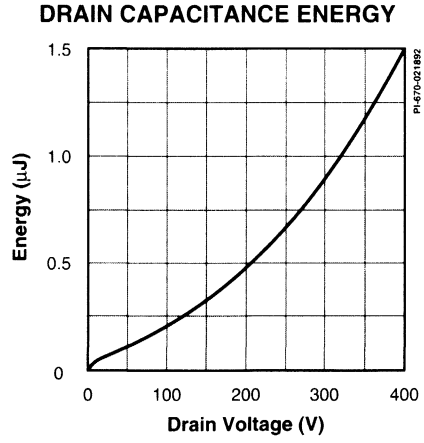

Figure 20.

Output Power Rating

The output power rating is limited by the thermal characteristics of the package and heat sink, the ambient temperature[4], and the peak switching transistor current limit circuit.

Thermal Characteristics

The PWR-SMP240WTC is packaged in a 23-pin power SIP package[5]. The thermal impedance from junction to ambient and from junction to case are 41°C/watt and 7.2°C/watt respectively. In order to exploit the full power capability of this package, an external heat sink is required. The major contributing factors to heat dissipation within the integrated circuit are the resistive losses due to the voltage drop across the output transistor, the switching losses in the output transistor due to the transistor stored charge and transformer and damping network capacitances[6], and the losses in the pre-regulator when it is active. Figure 19 gives the drain charge as a function of drain voltage. The integral of voltage with respect to charge gives the stored energy in the drain-source charge, which is charted in Figure 20. The energy curve is used to determine the AC losses in the transistor due to the stored charge. Losses are equal to the stored energy when the output switching transistor turns on multiplied by the operating frequency. The energy stored in the transformer and damping network capacitance must be added to this figure to determine the total AC losses in the circuit. Additional information on thermal management is available in AN-9.

Current Limit

Since the PWR-SMP240 control IC utilizes current mode control, cycle by cycle current limit protection occurrs as a natural consequence of the design, and requires no additional circuitry. Maximum peak current is set by the values of R2 and R11. R11, in conjunction with a 480 uA current source internal to U1, sets the maximum reference voltage for the current comparator. Peak primary current is sensed by R11. Maximum peak current is determined by the equation:

$$I_{pk} = \frac{R2}{R11} \times (480\mu A - 2 \times I_{FF})$$

where I_{FF} is the feedforward compensation current. As supplied, the PWR-EVAL8 does not use feedforward compensation, so the I_{FF} term will normally be zero. However, if feedforward is used, the I_{FF} term should be taken into account when selecting R2 and R11. When choosing values for R2 and R11, two factors should be considered. The current comparator reference voltage set by R2 should be reasonably large to provide noise immunity. However, if it is set too high, power dissipation across R11 will be excessive at the current limt point. The value of R2 used in the EVAL8 demonstration circuit (2.4 kΩ) sets the maximum current compararator reference to 1.15 V. Since R11 is set at

3

1Ω, the maximum peak current is set at 1.15 A. Given the waveshape and duty cycle of the primary current, the maximum RMS current through R11 is about 600 mA, which yields a power dissipation of 360 mW at the current limit point, which is adequate derating for R11 at the current limit point.

The PWR-SMP240 control circuit blanks the first 100-200 ns of the signal from the current sense resistor. This feature helps to eliminate spurious termination of the switching cycle caused by output rectifier reverse recovery spikes. In conventional current-mode circuits this leading edge spike is usually suppressed by filtering the current sense signal. This can add substantially to the delay time in the current feedback loop, which increases the minimum on time of the switching cycle. This can cause problems at high line and during fault conditions, especially at a high operating frequency. The PWR-SMP240 does not require passive filtering for the blanking function, and the overall speed of the current sense loop is not affected.

The effect of current limit on the output voltage can be seen in Figure 21. The shape of the current limit function is fairly close to a constant power curve. This is because the circuit regulates the peak current in the transformer primary, providing a constant energy delivery to the core during current limit. Since the power supply operates at a constant frequency, constant power is delivered in current limit.

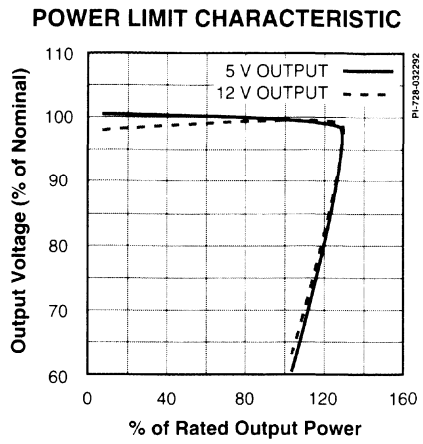

Figure 21.

Operating Frequency

The operating frequency of the PWR-EVAL8 is typically 130 kHz. The frequency of operation is adjustable by varying the timing capacitor C11 connected to pin 3 of U1. The nominal output operating frequency can be estimated with the following formula:

$$f = \frac{127 \times 10^{-6}}{C_{EXT}(\text{in pF})}$$

Where f is the frequency expressed in kilohertz, and C_{EXT} is expressed in pF. Note that the oscillator of the PWR-SMP240 will run twice as fast as the output due to the internal frequency divider in the 50% maximum duty cycle mode. If the 90% duty cycle mode is selected, the internal frequency divider is disabled, and the output frequency will be identical to the oscillator frequency. The nominal oscillator frequency with C_{EXT} = 470 pF is 270 kHz. The PWR-EVAL8 printed circuit board includes circuit traces for a transformer-coupled synchronization option. This circuit, when populated, allows the frequency of the power supply to be synchronized to a external TTL-level source. The schematic diagram for this option is shown in Figure **22**. The secondary turns should be wound on one-third of the circumfrence of the toroid. The primary turns should then be spaced evenly around the entire circumfrence. "Start" and "finish" of the primary should be on opposite sides of the core from the "start" and "finish" of the secondary.

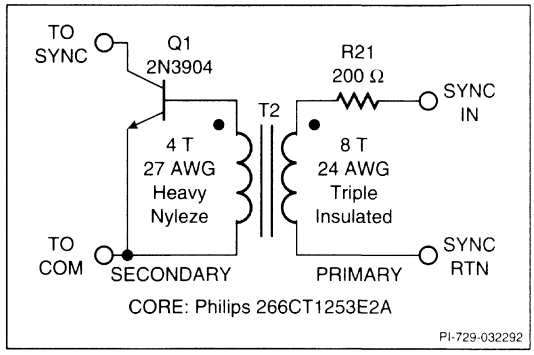

Figure 22. Optional External Synchronization Circuit.

A transfomer approach was chosen over an optically-coupled approach because affordable optocouplers lack the required speed to run properly at the operating frequency of the PWR-EVAL8. In practice, the nominal operating frequency of the oscillator should be set about 10% below the synchronizing frequency to allow the oscillator to lock in properly to the external source. Pulse width of the synchronizing signal should be at least 100 ns to allow the synchronizing transformer and transistor time to turn on. Pulse width into Pin 6 of U1 should be limited to 1 µs or less to avoid activating the ON/OFF function of the IC. The ON/OFF function will shut down the output and trigger the soft start sequence. Transistor Q1 has a storage and fall time of about 500 ns as used in the synchronizing circuit. This time should be considered when determining the maximum pulse width for the synchronization signal.

Remote Inhibit

The SYNC pin of the PWR-SMP240 can also be used to implement a remote inhibit function. If Pin 6 is pulled down to analog common for more than 10 µs, the power supply will shut down. If this pin is held down, the power supply will remain off indefinitely. Releasing Pin 6 allows the controller to initiate a soft-start cycle and restart the supply. Circuit traces are provided on the PWR-EVAL8 to allow implementation of an optically-coupled remote inhibit circuit. Isolation of the inhibit circuit is required because the control IC is on the primary side of the power supply. A schematic diagram for the inhibit circuit is provided in Figure **23**. The inhibit circuit is activated by a TTL-level "high" signal.

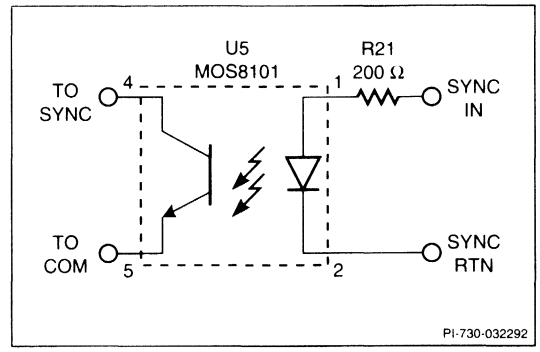

Figure 23. Optional External Inhibit Circuit.

Maximum Duty Cycle Select

The PWR-EVAL8 is configured for a maximum duty cycle of 50%. In most circumstances, this is an optimum value for use in a universal input flyback power supply, allowing sufficient dynamic range to comfortably cover the entire input voltage swing. Also, limiting the input duty cycle range allows the use of current-mode control without the danger of current-mode oscillation. To select a 50% maximum duty cycle, SLOPE COMP (pin 4) of the PWR-SMP240 is tied to V_{S1}/V_{S2} (Pins 10 and 11).

If a wider duty cycle range is required, SLOPE COMP can be connected through a resistor to COM. This sets the maximum duty cycle to 90%, and the value of the resistor sets the amount of slope compensation provided. This modification can be done by removing JMP1 and inserting resistor R1. If the wide duty cycle option is selected, slope compensation should be employed to prevent current-mode oscillation. The amount of slope compensation is determined by R1, and is inversely proportional to its value. The installed value of R1 is 36 kΩ. The range of values for R1 can be from 7 to 36 kΩ. Refer to AN-11 for a more detailed description of current mode control theory and criteria for selecting current mode compensation components.

Control Loop

The PWR-SMP240WTC utilizes current-mode control[7]. Current mode control uses the signal from the output voltage error amplifier to set the threshold of a comparator which monitors the peak current in the primary power switch. This comparator turns off the output switch when the peak current exceeds the level set by the error amplifier. The error amplifier signal is used to program the cycle-by-cycle peak current in the primary switch. This has several advantages in terms of power supply operation. First, since the peak primary switch current is controlled by the error amplifier, current limit protection is inherently provided. Additionally, since a peak current level is programmed by the error signal instead of a fixed duty cycle, open loop correction for input ripple is obtained, greatly reducing the demand on the output error amplifier. Lastly, current mode control transforms the power supply into a controlled current source. This effectively eliminates one of the poles in the output filter transfer function, making the power supply easier to stabilize. The PWR-EVAL8 uses the PWR-SMP240 control circuit to construct a current-mode controlled flyback power supply designed to operate in the continuous current mode. The DC input to output voltage transfer function for a flyback supply when operating in the continuous current mode is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

where D is equal to the duty cycle of the switching transistor[8]. The duty cycle is controlled by the output voltage error amplifier, which sets the cycle by cycle peak current in the primary power switch. The error amplifier will adjust the duty cycle to maintain a constant output voltage.

The spice model listing for the control loop[9,10,11] is included in the documentation disk. T1, U1, U2, U3, R2, R11, R13, R14, R15, R18, R26, C2, C14, C23, C24, C26, and C30 are the circuit elements that affect the control loop. The model for the transformer uses two transconductance generators and two resistances. The coefficients of the small-signal pulse width modulator transfer function generators are calculated by knowing the transformer inductance, the duty cycle of the operating point of interest, the switching period, the current sense resistor, and the on-time slope of the current sense waveform.

The input voltage feedforward gain is:

$$k_f = \frac{-D \times T_S \times R_i}{L} \times \left(1 - \frac{D}{2}\right)$$

The output voltage feedback gain is:

$$k_r = \frac{(1-D)^2 \times T_S \times R_i}{2L}$$

The modulator gain is:

$$F_m = \frac{1}{(S_n + S_e) \times T_S}$$

D is the duty cycle at the operating voltage of intrest. T_S is the switching time, which is equal to the reciprocal of the operating frequency. L is the primary inductance of the power transformer, and R_i is the value of the current sense resistor. S_n is the slope of the inductor current waveform, equal to L/V_{in}, where V_{in} is the voltage across the transformer primary during the on time of the switching cycle. S_e is the slope of the slope compensation ramp. If no slope compensation is used, this value is zero. The measured open loop gain/phase response curve for 120 V_{RMS} input (solid lines) and 240 V_{RMS} input (dashed lines) are shown in Figure 24. The 120 V_{RMS} input control loop has 76° phase margin, an open loop unity gain crossover frequency of 1.4 kHz, and 21 dB gain margin at 10 kHz with a 20 W load. The 2430 V_{RMS} input control loop has 50° phase margin, an open loop unity gain crossover frequency of 3.1 kHz, and 15 dB gain margin at 10 kHz with a 20 W load.

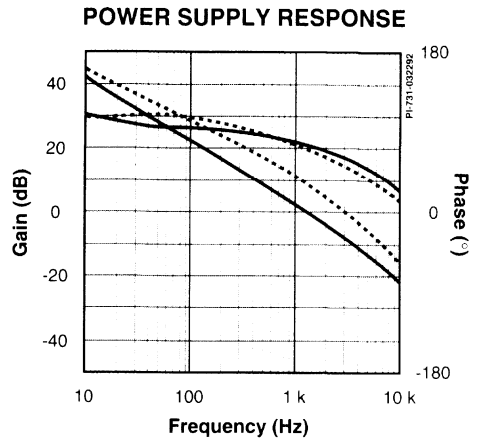

Figure 24.

The output load transient response can also be used to provide an indication of power supply control loop stability. Because this test exercises the loop in the large signal domain by forcing it to slew, it is useful in uncovering areas of marginal or conditional stability. Figure 25 gives the load transient response of the 5 V output of the PWR-EVAL8 for a 75%-100%-75% repetitive load step. The 12 V output was loaded at 1 A, and the input voltage was set to 162 VDC. The initial transient recovers in about 100 µs for a 25% load step. The pedestal portion of the waveform is due to the finite load regulation of the 5 V output. The slight ringing is due to the second LC output filter on the 5 V output.

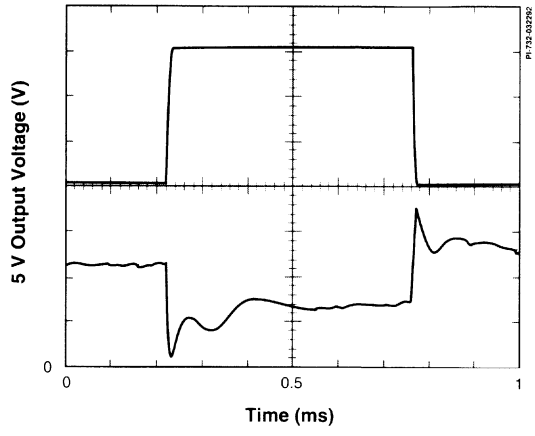

Figure 25. Transient Response.

Protection Features

Overtemperature

The overtemperature protection circuit disables the power device when the junction temperature reaches approximately 140°C and keeps it off until the junction temperature decreases 45°C[12].

Test Mode

The I_{LIMIT} input (pin 9) controls the built-in test logic of the integrated circuit. The test logic turns on the power transistor continuously when the voltage on pin 9 is equal to the pin 10 & 11 voltage (5.8 V) ±1.5 V. Do not put the PWR-EVAL8 into test mode while operating in a power supply circuit as this could destroy the PWR-SMP240.

Control Circuit Undervoltage Protection

The internal undervoltage lockout circuit ensures that the internal bias voltages are within specification before the output power switching transistor will operate. The threshold is the regulation voltage of the V_S regulator.

Input Filtering and Rectification

BR1 and C1 perform the input rectification and filtering function. The rectifier bridge should have a voltage rating of 400 to 600 V and a surge current rating exceeding the input surge current of the circuit. The voltage rating on C1 is equal to the peak value of the maximum rectified input voltage, 200 V for 120 VAC and 400 V for 240 VAC applications.

Capacity of the Input Storage Capacitor

The capacity of the input storage capacitor C1 can be computed by knowing the maximum input power of the power supply, the minimum DC input voltage provided to a regulated output voltage at maximum power, and the minimum AC input voltage[13]. The calculation uses the capacitive energy equation:

$$C = 2 \times W \times \frac{T}{V_1^2 - V_2^2}$$

where W is the input power of the power supply, T is the time the input bridge rectifiers are not conducting current, V_1 is the voltage on C1 when the input bridge stops conducting, and V_2 is the voltage on C1 when the input bridge starts conducting.

A "Rule of Thumb" has been developed over the years for the size of the input capacitor. This rule is that the capacitance in microfarads is equal to two times the output power in watts. This rule is useful for a first approximation of the minimum input capacitor value for both 120 VAC and universal input voltage ranges.

Input Surge Current

When mains voltage is applied to the power supply, a surge of current flows into the input to charge the input storage capacitor C1[14]. The magnitude of current must be within the surge ratings of the power switch, fuse, EMI filter, and input rectifiers. The surge current is limited by the resistance of the input surge limiting thermistor R20. This device is a negative temperature coefficient thermistor with a room temperature resistance value of 10 Ω. The thermistor initially presents this value of resistance to the AC line when the power supply is first turned on, limiting the input inrush current to a maximum value of 37 A. After limiting the initial surge current, the thermistor heats up and assumes a low value of resistance, allowing the supply to operate without undue power loss.

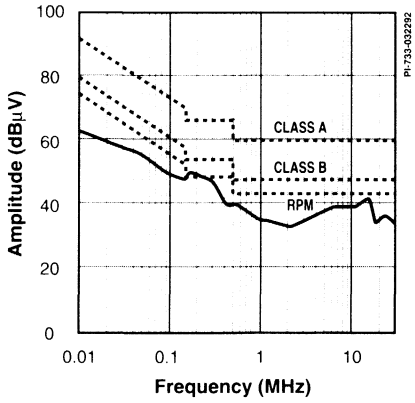

Figure 26. EMI Plot of the PWR-EVAL8.

EMI Considerations

This power supply was designed to meet worldwide EMI (DIN VDE 0805/05.90) and safety (UL1950 and IEC950) specifications. Figure 26 is a plot of the maximum conducted EMI relative to the VDE specification limits. Additional information is available in DA-4, which discusses Electro-Magnetic Interference (EMI).

Differential Mode Filter
L1, L3, and C6 filter differential-mode conducted emissions.

Common Mode Filter
L2, L6, C7, C8, C12, and C20 filter common-mode conducted emission currents[15]. There is a Faraday shield inside the transformer to direct the primary to secondary capacitive currents away from the secondary circuit. This shield provides appreciable attenuation for common mode currents.

C20 couples high-frequency noise back to the system chassis ground. C7, C8, and C12 conduct common-mode noise currents back to their source, which is the DRAIN of the PWR-SMP240. L2 prevents the common-mode current from flowing back into the AC mains.

Power Cord Damping
A six foot long 3-wire power cord will resonate at between 15 and 25 MHz. Any emissions in this frequency band will be amplified by the power cord.

The characteristic impedance of the power cord is approximately 100 Ω. The small inductor L6 in series with the ground lead of the power connector is a "lossy" bead and is equal to a 100 Ω resistor at frequencies above 15 MHz. The "lossy" bead provides damping for the power cord so that any emissions in this band will not be amplified by the resonance of the power cord.

Shielding
Shielding of the high-voltage, high-frequency waveforms may be necessary to provide greater margin from the class B conducted emissions requirements of FCC and IEC specifications.

Safety Agency Requirements

The PWR-EVAL8 has been submitted to TUV Rhein Land for evaluation per IEC 950.

Additional information on safety and layout-related issues is available in DA-2.

Documentation Disks

The PWR-EVAL8 package includes two floppy disks (one 3.5 inch, and one 5.25 inch) which carry a large selection of reference information regarding the PC board design and layout. These files were used in the manufacture of the evaluation board, and are provided to facilitate the reproduction or modification of the PWR-EVAL8 design. Both disks are high density MS-DOS format. Each of these disks contain the following files:

README8.BAT	(This file) contains a summary and last minute information on PWR-EVAL8
PWB1006B.APR	Aperture file with assigned D-codes
EVAL8.BOM	Bill of Materials file
EVAL8ASY.DWG	Assembly drawing file
FAB1006B.DWG	Fabrication drawing for the PC board
1006BCL.G23	Copper layers gerber file
1006BSM.G23	Solder mask layers gerber file
1006BSKP.G23	Silkscreen and padmaster gerber file
EVAL8.LIB	Library file of the part symbols used in both schematics
PWB1006B.NCD	NC drill file for computerized drilling of the PCB
EVAL8.SCH	Schematic file of PWR-EVAL8
SPICEMDL.SCH	PSpice model schematic
SPICE_AC.TXT	PSpice listing
FUNCDES8.TXT	Functional description of the power supply circuitry used in PWR-EVAL8
ICDESC2.TXT	Functional description of the PWR-SMP240 integrated circuit used in PWR-EVAL8
EVL8COST.TXT	Estimated parts cost
T1005 Directory	Transformer specification

- All files with a .DWG extension were prepared in AutoCAD 286, Rel. 10.
- The gerber files were extracted using Gerber absolute 2.3 format.
- The NC drill file was extracted in Excellon format.
- The schematic file was created in OrCAD SDT Version 4.04. The library file is used with OrCAD SDT to create the symbols used in both the schematics.
- The README8.BAT and the EVAL8.BOM files are ASCII text files.
- The DXF format version of the assembly print, fabrication print and schematic are available from Power Integrations request.

Power Integrations grants all design rights to this circuit layout or any modifications thereof to customers for use in their end products.

Power Integrations reserves the right to make changes to the design at any time and cannot guarantee availability or price on any product listed other than the PWR-SMP240.

Although the circuit has been designed with all pertinent EMI and safety standards in mind, this is an evaluation board only, and has not been approved by any regulatory agency at this time. The customer assumes all responsibility for compliance with all pertinent regulatory requirements regarding the use of modification of this evaluation board. Power Integrations does not assume any liability arising from the use or modification of any device or circuit described in this document or on the disks, nor does it convey any license under its patent rights or the rights of others.

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Applications Information 4

INDEX

Designing Power Supplies with PWR-SMP3

APPLICATION NOTE AN-6

POWER INTEGRATIONS, INC.

This application note will explain the development of a flyback power supply using the PWR-SMP3 Power Integrated Circuit. The PWR-SMP3 is a monolithic device which combines a new high voltage power MOSFET switch with all the analog and digital control circuitry required to implement isolated, regulated, and protected power supplies. Designing the power supply has been greatly simplified because few external components are required. The high switching frequency of 1 MHz reduces the size of the power supply by allowing the use of smaller energy storage components. The PWR-SMP3 was designed for use in isolated power supplies or DC to DC converters. Power levels up to 3 Watts can be delivered from AC voltages of 90 to 140 volts or DC voltages of 75 to 200 volts. Operation from lower input voltages is also possible with reduced levels of output power.

The Flyback power supply is explained in detail. Ideal and non-ideal circuit operation are explained. The difference between the discontinuous and continuous mode of operation is discussed. The benefits of high frequency operation are presented. Other types of power supplies using both linear and switching techniques are examined.

The PWR-SMP3 Power Integrated Circuit is explained in detail. The features of the power MOSFET switch including low input capacitance, low Miller capacitance, and logic level threshold voltage are discussed. The advantages of integrating the power switch with analog and digital circuit functions are presented and each circuit function is explained.

An actual power supply design is presented as an example. Specifications are given, and key design parameters are discussed. Selection criteria for each component is presented and printed circuit design guidelines are listed. Component part numbers and sources of material are presented to implement the example power supply.

Key areas are discussed in greater detail in the appendices. Input capacitor selection, power transformer design guidelines, and feedback loop stability analysis are all discussed in detail.

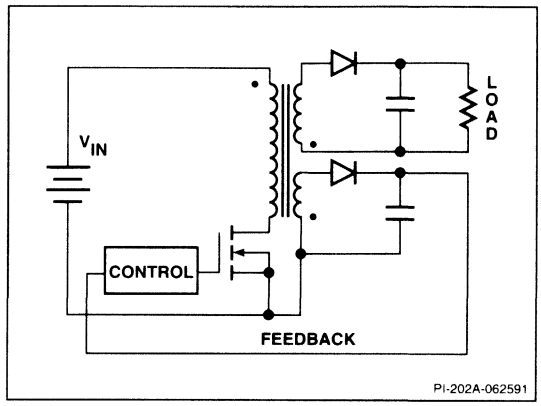


Figure 1. Basic Flyback Converter Circuit.

The Flyback Power Supply

The Flyback topology, shown in Figure 1, operating in discontinuous mode is recommended for off-line, isolated, low power applications. The flyback technique has a low parts count, wide DC conversion range, inherent feedback voltage sensing, single or multiple output voltage capability, output voltages that can be higher or lower than the input voltage, and can provide both positive and negative voltages. The discontinuous mode makes the control system simpler to stabilize with wider bandwidth (see appendix F for discussion).

Isolated power supplies require a power transformer to provide isolation. Switching power supplies need an inductor as part of the low pass filter required for a DC output. The flyback topology is attractive for low power isolated switching power supplies because the transformer is combined with the inductor in a single magnetic component. The flyback power supply has the fewest magnetic components and the lowest parts count resulting in the lowest cost. The topology retains these same advantages at power levels up to 100 watts. Component stress levels above 100 watts require the use of more expensive components allowing other topologies to become cost effective.

Another important advantage of the flyback topology is that a feedback voltage proportional to the output voltage can be obtained directly by adding a "feedback" winding to the power transformer. Additional optocouplers or pulse transformers

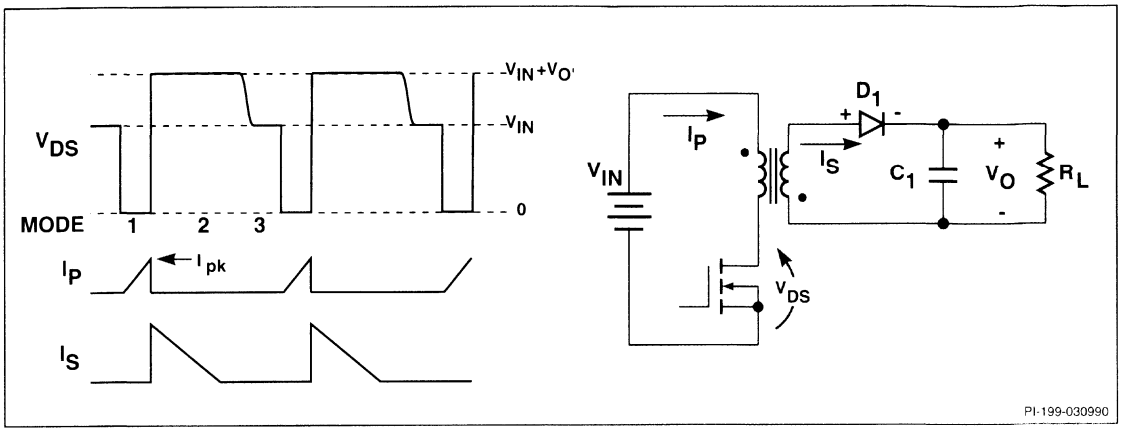


Figure 2. Ideal Flyback Converter Waveforms - Discontinuous Mode.

needed by other approaches for closing the feedback loop are not required at this low power level.

Single or multiple, higher or lower, positive or negative output voltages are primarily a function of the construction of the power transformer.

Ideal Model (Discontinuous Mode)

There are three distinct intervals of circuit operation for flyback power supplies operating in the discontinuous mode as shown in Figure 2.

The first interval (1) of operation occurs when the switch is closed. Current I_P ramps up in the transformer primary winding which causes a magnetic field to build in the transformer core. The voltage across the power MOSFET transistor is nearly zero during this interval. The output diode prevents current flow in the secondary due to the transformer dot polarity.

The second interval (2) of operation starts when the switch is opened. The energy stored in the magnetic field of the transformer causes the voltage across both the primary and secondary windings to reverse polarity. In an ideal circuit the primary current I_P instantly stops flowing while the secondary current I_S instantly starts flowing (it will be shown later how important it is to consider non-ideal behavior). The voltage across the secondary winding is equal to the sum of the output voltage and diode forward voltage. The secondary voltage is "reflected" back through the transformer to the primary winding. Note that the voltage across the transistor is equal to the sum of the reflected output voltage V_{O}' and the input voltage V_{IN}.

The third interval (3) of operation occurs when the magnetic field within the core has decayed to zero. No current flows in the primary or secondary of the transformer (which defines the discontinuous mode of operation). Note that the voltage across the transistor has decayed to the level of the input voltage.

Ideal Model (Continuous Mode)

Refer to Figure 3 for the characteristic waveforms for the continuous mode of operation (the circuit is the same as in Figure 2).

The difference between continuous and discontinuous operation is shown in the current waveforms. The secondary current I_S does not decay completely to zero as it did in discontinuous mode. The primary current I_P starts with a current step equal to the final value of the secondary current I_S reflected through the turns ratio. The voltage across the transistor is also different since the third interval has been eliminated as previously discussed. The reflected output voltage state persists for the balance of the cycle until the switch is turned on again.

The size of the inductance of the power secondary winding on the power transformer determines continuous or discontinuous operation. A smaller inductance will give up the energy stored

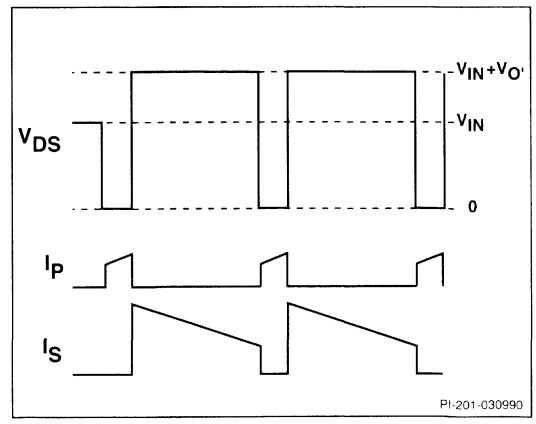


Figure 3. Ideal Flyback Converter Waveforms - Continuous Mode.

in the magnetic field at a faster rate and result in discontinuous conduction mode. Conversely, a larger inductor will not give up all the energy stored in the core each cycle and operate in continuous mode. While more average power can be delivered by operating in continuous mode, loop stability is more difficult to achieve (refer to appendix F).

Non-ideal Model (Discontinuous Mode)

The circuit for the non-ideal flyback power supply and the associated waveforms are shown in Figure 4. The non-ideal flyback topology has three additional parasitic elements: two inductances and one capacitance. The inductor L_1 is the leakage inductance of the primary winding on the power transformer. The inductor L_2 is the leakage inductance of the secondary winding on the power transformer. The capacitor C_2 is the combination of the output capacitance of the power MOSFET switch and stray circuit capacitance.

As previously shown, the circuit has three intervals of operation per switching cycle. The impact on circuit operation by the three additional parasitics in each of three intervals of operation will now be discussed.

In the first interval (1) the power MOSFET switch is turned on which instantly discharges C_2. The energy stored by C_2 at the end of the previous cycle is dissipated in the power MOSFET switch at the beginning of the turn on interval. This dissipated energy is proportional to the square of the voltage on the capacitor. Because of this effect large values of output capacitance dramatically lower efficiency at high frequency. Leakage inductance has little effect during the turn on interval.

In the second interval of operation the power switch is turned off. The energy stored in the transformer magnetic field during the previous interval is now transferred to the secondary circuit. A problem that arises during this transfer is that leakage inductances L_1 and L_2 are both trying to oppose changes in current flow: L_1 is trying to maintain primary current flow and L_2 is trying to block secondary current flow. There is a "crossover region" during which the primary current ramps down and the secondary current ramps up. The primary current ramps down to zero with a slope determined by the value of leakage inductance and circuit voltage levels. The secondary current ramps up to the final value with a slope determined by leakage inductance and circuit voltage levels. The big problem is that the primary current must continue to flow "somewhere" during this crossover interval. The decaying primary current ends up flowing into the capacitance C_2 which charges up to some peak voltage V_{pk}. This peak voltage, caused by leakage inductance, will be referred to as the "leakage spike".

During the third mode of operation the reflected output voltage goes to zero. The transformer magnetic field has given up all the energy stored during the first interval. The MOSFET transistor voltage makes a transition from the level associated with the sum of the reflected output voltage and input voltage (V_{IN}) down to a level equal to the input voltage V_{IN}. This transition excites the resonant tank circuit formed by the capacitance C_2 and the primary inductance to create a decaying oscillatory waveform. This waveform "modulates" the voltage on (and the amount of energy stored in) C_2 which determines the power loss when the switch is turned on at the beginning of the next cycle.

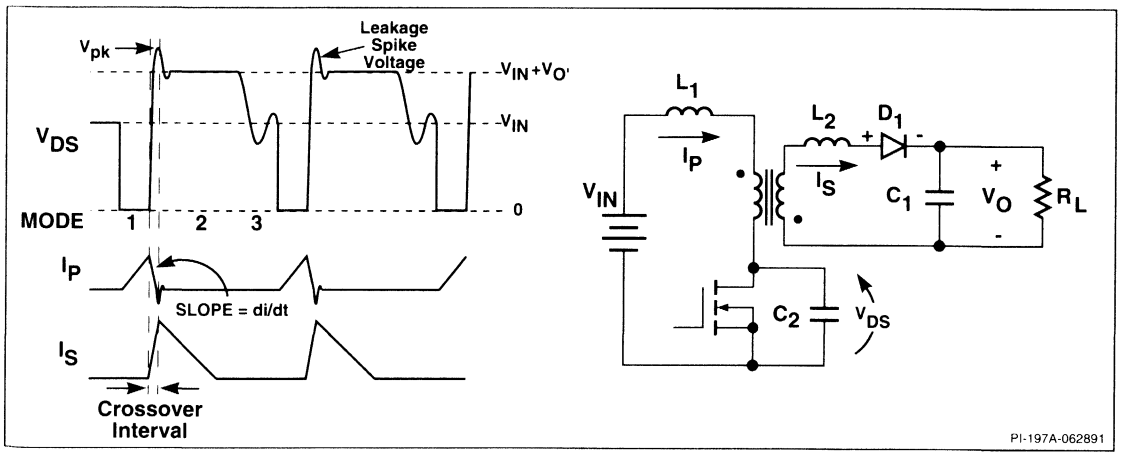


Figure 4. Non-ideal Flyback Converter Waveforms - Discontinuous Mode.

Advantages of 1 MHz Operation

There are several advantages to high frequency operation:

- Smaller output filter capacitance required
- Smaller power transformer required
- Wider bandwidth control loop

The output capacitor size and value varies inversely with the switching frequency for a given load current and ripple specification. A higher operating frequency allows the use of highly reliable ceramic capacitors. Electrolytic capacitors are not required.

The size of the power transformer is also smaller at higher frequencies, though the reduction is not as dramatic as the output capacitor. Lower numbers of turns on each winding and smaller core cross sectional areas can be used to implement high frequency transformers.

The combination of smaller output capacitor and smaller transformer reduces the overall power supply size. High frequency operation squeezes the power supply into those applications requiring the smallest size possible.

The bandwidth of the control loop is much wider when a high switching frequency used. Faster transient response to both line and load variations are the direct result. The input capacitor may be reduced in size because the larger ripple voltage can be adequately rejected by the wide bandwidth control loop. Allowing larger ripple voltage has the added benefit of improving power factor and reducing the harmonic content of the input current waveform slightly.

Comparison to Other Techniques

Linear Power Supplies
The linear power supply is characterized by the use of a 60 Hz transformer, rectifier, filter, and linear regulator as shown in Figure 5. This type of power supply is inexpensive and reliable but suffers from the following disadvantages:

- Largest size
- Highest weight
- Poorest efficiency

Switching Power Supplies
There are many different switching power topologies available. The Buck, Boost, and Forward converters are described below. Multiswitch and resonant converters are also briefly discussed.

Buck Converter - The buck converter (shown in Figure 6) is useful for stepping down from a high voltage to a low voltage.

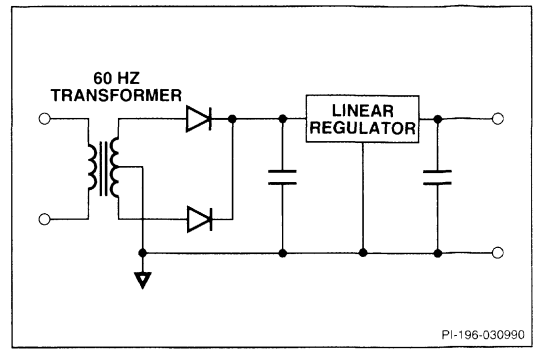


Figure 5. Linear Regulator Circuit.

Key points:

- Not isolated
- High side switch requires level shift or bootstrap circuit to drive
- Limited to approximate 10:1 conversion range by duty cycle requirements
- Provides only down converted, positive output voltages

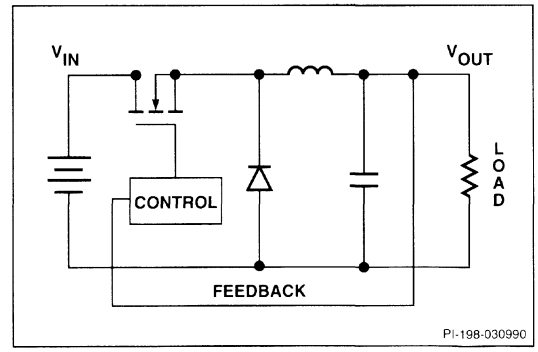


Figure 6. Buck Converter Circuit.

Boost Converter - The Boost converter (shown in Figure 7) is useful for stepping up from a lower voltage to a higher voltage.

Key points:

- Not isolated
- Limited to approximate 10:1 conversion range by duty cycle requirements
- Provides only up converted, positive output voltages

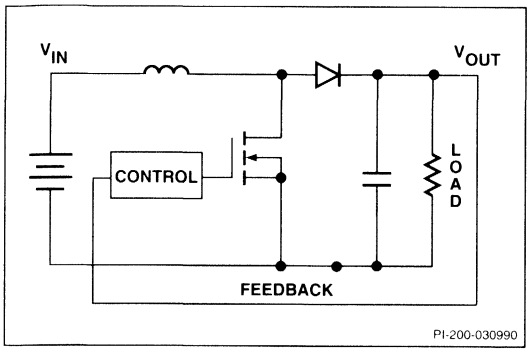


Figure 7. Boost Converter Circuit.

Forward Converter - The Forward converter (shown in Figure 8) is an isolated version of the Buck. Single or multiple, positive or negative, higher or lower output voltages are available by transformer design.

Key points:

- Inductor required for each output voltage
- Extra diode required for each output voltage
- Additional isolated feedback circuit required

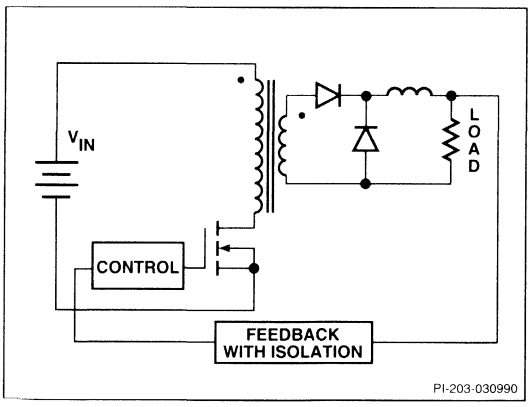


Figure 8. Forward Converter Circuit.

Multiple Switch Converters - Multiple switch converters include the push-pull, half bridge, full bridge, two transistor flyback, and two transistor forward. All these converters require at least one additional power switch and are much more complex and costly. They are used to implement power supplies ranging from 100 watts to several kilowatts and are inappropriate for this power level.

Resonant Converters - In general resonant converters require additional components and operate at frequencies considerably higher than 1 MHz. Peak stress levels are higher than power converters using square edged waveforms characteristic of the techniques described above. The most effective resonant converters use both high side and low side switches adding to circuit complexity. Resonant converters are not cost effective at these power levels.

The PWR-SMP3 Power Supply IC

Advantages of the Integrated Approach

High Performance MOSFET Switch - The high performance power switch features a proprietary technology that gives the user the following benefits:

- High Voltage Operation
- Small Die Area
- Low Input and Miller Capacitance
- Logic Level Threshold
- Integrates with Standard CMOS Building Blocks

High voltage capability makes it possible to use this technology in power supplies that operate from the 120 VAC power line. Other integrated approaches are restricted to lower input voltages.

The area occupied by the power MOSFET switch in the Power Integrations high voltage process is comparable with the best discrete devices for a given voltage breakdown rating and $R_{DS(ON)}$. This technology offers lower input capacitance and extremely low Miller capacitance. Easier gate drive and faster switching are two benefits of the lower capacitance.

Another key feature of this technology is the logic level threshold voltage. The MOSFET is fully enhanced with 5 volts applied to the gate. Discrete devices must be driven to 10 volts for complete enhancement. The amount of drive power required to drive the gate is actually the energy needed to charge the gate capacitance multiplied by the frequency of operation. The amount of energy required is directly proportional to the gate capacitance but increases with the square of the gate voltage. The combination of low input capacitance and a logic level threshold results in a tremendous savings in drive power. The input capacitance can be as much as three times lower than an equivalent discrete device. Reducing the gate voltage from 10 to 5 volts reduces the amount of drive power by an additional factor of four. The amount of power required to drive the gate of the MOSFET switch is lower by a factor of 12 or more (see appendix G for details).

The power switch is easy to integrate with CMOS analog and digital circuitry such as operational amplifiers, comparators, logic gates, latches, etc. Functions normally requiring costly external or discrete circuitry can be integrated for a reduction in total parts count and better reliability.

Fast Current Limit Response - A current mirror integrated into the power MOSFET switch provides a way of measuring the drain current. An integrated current sense function eliminates the delays associated with discrete sensing and filtering techniques.

Another benefit is reduced susceptibility to noise. The integrated approach provides physically short current paths and eliminates connections which can inject noise into sensitive circuit nodes.

Fast Temperature Response - The actual junction temperature of the integrated power MOSFET switch can now be sensed directly. As a result the power MOSFET switch can be protected through the use of on-chip temperature protection. This approach provides a fast response to an overtemperature condition. External or discrete approaches suffer from poor accuracy and slow response time. The integrated approach gives better performance and offers higher demonstrated reliability.

The integrated temperature protection prevents catastrophic failure from shorted outputs by shutting down the power supply. The external power supply components will also be protected by the integrated over temperature feature. The lack of integrated temperature protection in a discrete circuit approach may lead to a "brute force" design using overrated power handling components to survive the current limit condition.

PWR-SMP3 Functional Description

The block diagram of the PWR-SMP3 is shown in Figure 9. All circuit functions required to implement an isolated, regulated, and protected power supply are included in the power integrated circuit.

Pre-regulator and On-board Voltages

The pre-regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5.6 volts by controlling the gate of the MOSFET. V_{BIAS} is used by another linear regulator to generate the on board supply voltage V_S.

The Pre-regulator MOSFET dissipates significant amounts of power when supplying bias current. Typical values for operation from V_{IN} generate a power dissipation of 600 to 800 mW. This dissipation is eliminated when the feedback winding and filter drives the V_{BIAS} pin above 8.25 volts. The pre-regulator is then cut off and the supply current is then by the feedback circuit.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and reducing noise.

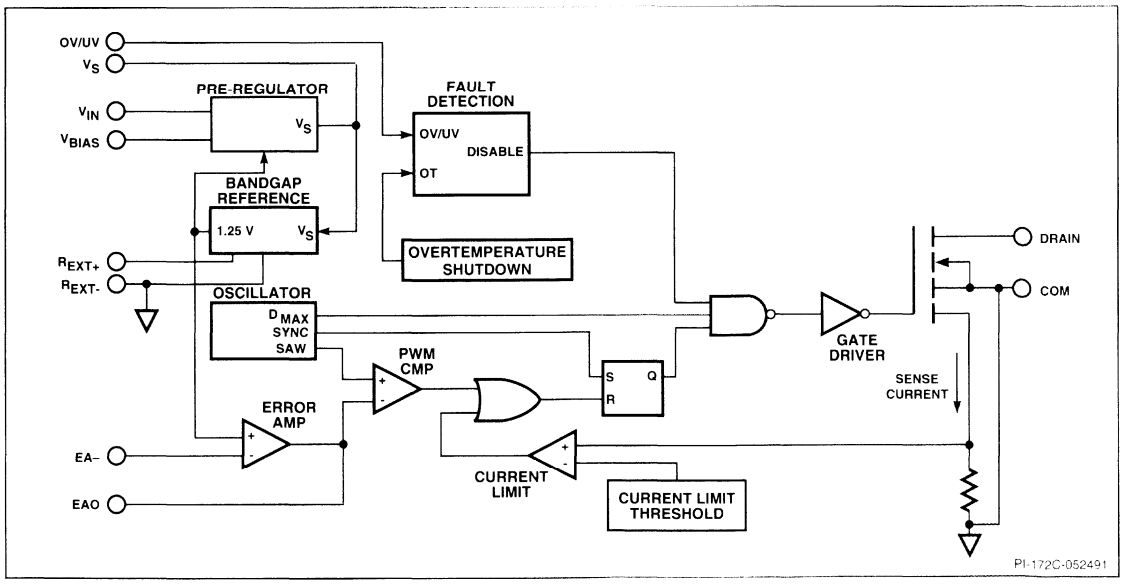


Figure 9. Functional Block Diagram of the PWR-SMP3 Power Supply IC.

Band Gap Reference

V_{REF} is the reference voltage generated by the temperature compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier, over temperature circuit, and current limit circuit.

Oscillator

The oscillator is completely self-contained. An internal capacitor is alternately charged and discharged by switched constant current sources. The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier

The error amplifier consists of a high performance operational amplifier with the non inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch. The output of the error amplifier is buffered, and has a 2 V offset and an output impedance of 1.5 kΩ.

Pulse Width Modulator

The voltage-mode pulse width modulator generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

The protection circuitry inhibits the driver signal when the input voltage is outside the limits of operation or the temperature of the device is too high.

OV/UV Lockout Protection

Undervoltage/Overvoltage Lockout disables the power switch when the input voltage is either too low or too high. A simple resistor divider to the UV/OV input will determine the voltage levels at which lockout occurs.

Current Limit Protection

The current limit sense consists of a current mirror on the power device and a sense resistor. The current mirror produces a current proportional to the drain current of the power switch. A sense voltage is generated by passing the mirror current through a sense resistor. This voltage is then compared to a reference voltage with a comparator.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit turns the power switch off when the junction gets too hot (typically 135°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

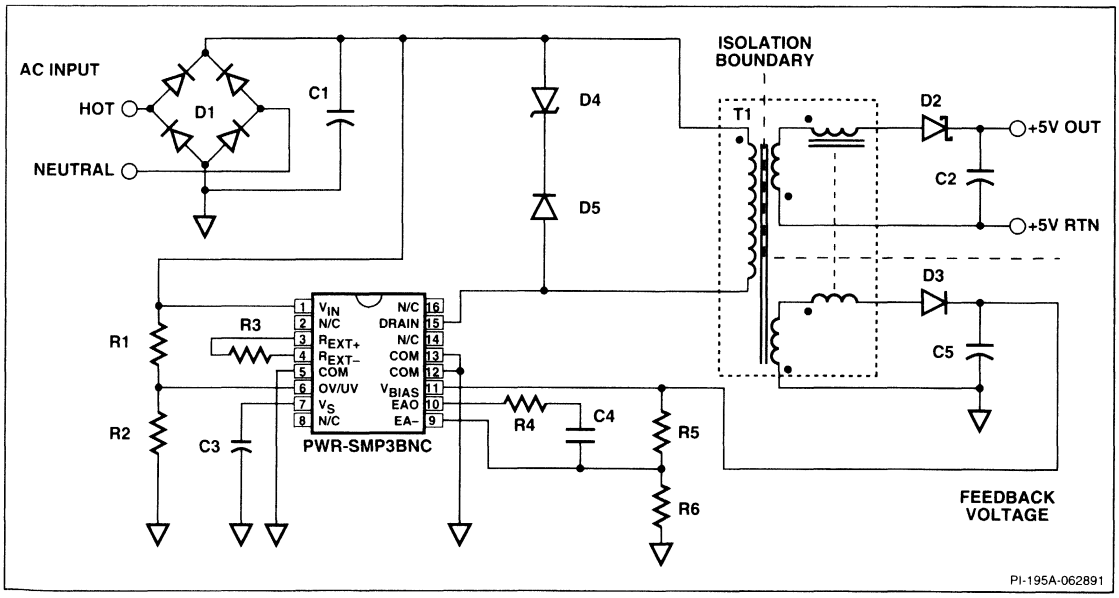


Figure 10. Simplified Schematic Diagram of a 3 W AC-DC Converter Using the PWR-SMP3.

Power Supply Example

The PWR-SMP3 was developed for applications up to 3 watts. Trade-offs such as size and cost need to be considered for each application. The basic design criteria for each component shown in the circuit diagram of Figure 10 will be developed.

Power Supply Specifications:

Output Power Range (P_O)	0.3 to 3 W
Output DC Voltage Level (V_O)	5 V
Output DC Current Range (I_O)	120 to 600 mA
AC Input Range	90 to 140 VAC
DC Input Voltage Range (V_{IN})	75 to 200 VDC
Line and Load Regulation	±5%

Design Parameters:

Frequency of Operation (f)	1 MHz
Peak Drain Current (I_d)	300 mA
On Time Maximum Duty Cycle (D)	40%
Off Time Minimum Duty Cycle (D')	50%
Feedback Voltage Average Value (V_{BIAS})	8.5 V
Bias Current (I_b)	4 mA
Efficiency (h)	65%
Input Power (P_{in})	4.6 W

General Circuit Operation
The frequency of operation is fixed by the internal oscillator at a typical value of 1 MHz.

The peak drain current was selected as a conservative value compared to the rated peak drain current. The duty cycle has been intentionally limited to a maximum value of 40%.

The off time duty cycle will always be at least 50%. This fixes the amount of time the flyback transformer has to dump the energy into the load. The long interval reduces the peak value of the secondary current and improves load regulation. This interval also ensures that discontinuous conduction operation can be maintained.

The output voltage of the feedback filter must be high enough to cut off the pre-regulator. The PWR-SMP3 has been designed to operate with an average feedback voltage of 8.5 V.

Supply current for the PWR-SMP3 is typically 4 mA.

Efficiency has been experimentally determined to be approximately 65% for the component guidelines given here. The use of different techniques or components will require a new evaluation of efficiency.

Average input power was calculated from the output power and efficiency.

External Component Selection
Bridge Rectifier Selection - The bridge rectifier diodes should have the following characteristics for a 120 VAC application:

- 600 V PIV rating
- Standard recovery speed
- 500 mA average rectified current rating
- 20 A surge current rating for 1/2 cycle @ 60 Hz
- Package pin spacing to satisfy desired safety specification

Input Capacitor Selection - The input filter capacitor C_1 smooths out the full wave rectified AC waveform into the DC voltage required by the power supply. The input capacitance should have the following characteristics:

- 5.2 µF minimum capacitance
- 200 V minimum operating voltage
- Surge voltage sufficient for expected transients

There are two strategies for the selection of the type of input capacitor: minimum size or minimum cost. The minimum size solution requires a single ceramic capacitor with an X7R or equivalent dielectric. The minimum cost solution requires a low cost aluminum electrolytic capacitor.

Power Transformer Selection - The power transformer provides energy storage, isolation, down conversion, and feedback. The size of the power transformer may depend on the safety specification that the application must meet. The smallest standard pot core acceptable for this application is the 1107 series available from a number of manufacturers. Creepage distance or isolation voltage requirements may require the selection of a larger core. General guidelines independent of core size are given below:

- Choose gapped ferrite pot core with A_L of 100 mH per 1000 turns
- Wind 32 turns on the primary in a single, uniform layer with no overlap for a nominal inductance of 102 µH.
- Wind 5 turns on the feedback secondary in a single, uniform layer over the primary for a nominal inductance of 2.5 µH.
- Insulate with 1 or more layers tape and/or paper as required by the appropriate safety specification.
- Wind 3 turns on the power secondary using insulated wire wide enough to completely cover the primary winding. Nominal inductance should be 900 nH.
- Tape windings in place and assemble transformer.

Clamp Component Selection - The clamp circuit limits voltage spikes on the turn off transition of the power MOSFET switch caused by transformer leakage inductance. The clamp circuit is formed by Zener diode D_4 and blocking diode D_5. An alternative

would be to replace the high-voltage Zener diode with the parallel combination of a 1 nF capacitor and a 240 kΩ resistor.

Zener Diode D_4 Characteristics:

- Avalanche breakdown voltage of 100 V @ 300 mA
- Power rating of 1.5 W minimum

Blocking Diode D_5 Characteristics:

- Voltage rating of 400 V
- Medium to fast recovery (less than 400 ns)
- Power rating of 250 mW minimum

Output Rectifier Selection - Diode D_2 rectifies the power secondary winding. D_2 should have the following characteristics:

- Schottky type rectifier
- Voltage rating between 40 and 50 V
- Forward voltage/current characteristic of less than 100 mV change for a current range of 550 mA to 2.7 A
- Power rating of 3 W or higher

Output Capacitor Selection - The output capacitor C_2 provides the filtering required to maintain the DC output voltage. C_2 should have the following characteristics:

- Ceramic dielectric (X7R or Z5U)
- Voltage rating of 25 V minimum
- Capacitance of 4.5 µF minimum

Feedback Component Selection - The feedback filter produces the DC feedback voltage V_{BIAS}, divides the feedback voltage to compare with the internal reference, and compensates the feedback loop.

- Rectifier and Filter:
  Diode D_3 should be a high speed signal diode with a breakdown rating of at least 75 V
  C_5 should be a ceramic capacitor, 0.1 µF, 25 V

- Divider:
  R_5 should be 18.2 kΩ
  R_6 should be 3.16 kΩ
  (NOTE: These values require the leakage inductance correction technique described in the next section)

- Compensation:
  R_4 should be 1.82 kΩ
  C_4 should be 2200 pF

Miscellaneous - The OV/UV resistor divider sets the window of operation for the DC input voltage. For a nominal window of 63 to 200 V:

- R_1 should be 845 kΩ, rated for full input DC voltage
- R_2 should be 5.36 kΩ
- The V_S VS capacitor C_3 should be 0.1 µF to adequately filter internal current peaks
- The reference current resistor R_3 should be 20.5 kΩ, 1%

A New Technique For Improving Load Regulation

Power supply load regulation is degraded by the leakage inductance of the power transformer. This section describes a patented new technique[1] for correcting for the effects of transformer leakage inductance and improving load regulation.

The accuracy of the output voltage depends heavily on the coupling between the windings of the power transformer. Poorly coupled transformers have high values of leakage inductance. Transformers designed for good coupling have smaller values of leakage inductance. Minimizing leakage inductance may be sufficient to meet the regulation requirements of the application if the output voltage value is not critical or the load relatively fixed. Higher accuracy can be obtained with the technique described below.

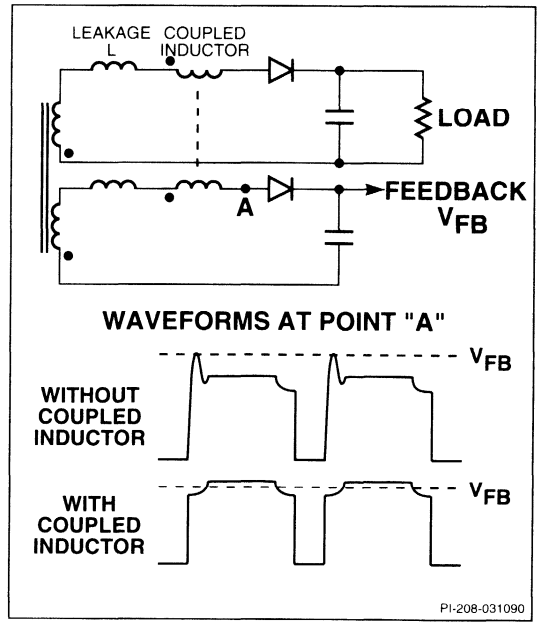


Figure 11. Coupled Inductor Waveforms.

Figure 11 shows how leakage inductance affects the regulation of the power supply. Current builds in the primary when the power switch is on. The problem occurs when the power switch turns off. The primary leakage inductance tries to maintain current flow while the power secondary leakage inductance tries to inhibit current flow. The current eventually crosses over by ramping down to zero in the primary and ramping up in the power secondary. There is a substantial voltage drop across both the primary and secondary leakage inductances during the crossover interval. The voltage drop across the power secondary leakage inductance reflects through the feedback secondary winding as a voltage spike. The feedback filter tends to charge up to the peak value of the spike rather than the reflected output "plateau" voltage. The key to achieving good regulation is to block the spike voltage.

The addition of a simple pulse transformer as shown in Figure 11 dramatically improves regulation. The pulse transformer consists of a small toroid with a single "primary" turn and wound with several turns of insulated wire for the "secondary". The "primary" of the pulse transformer is created by slipping the toroidal core over the transformer power secondary winding. The "secondary" is then placed in series with the feedback winding. The core is selected so that the inductance created by the transformer "primary" is less than the effective leakage inductance of the power secondary winding. The "primary" generates an additional voltage drop during the crossover interval. This voltage drop is then multiplied by the number of secondary turns and subtracts from the voltage spike generated on the feedback winding. The number of "secondary" turns are adjusted until the spike has been completely blocked.

Guidelines:

- Use a small Nickel-Zinc toroid core for currents up to 2 A Use a powdered iron core for currents above 2 A
- Primary inductance should be 1/2 to 1/3 the leakage inductance
- Minimize length of single turn primary
- Secondary should be wound with insulated wire rated for 120 VAC operation and suitable for the desired safety specification
- Wind sufficient secondary turns to block feedback winding spike

Summary

A new power integrated circuit, the PWR-SMP3, has been presented which simplifies the implementation of off-line switching power supplies. The PWR-SMP3 has been used to create small flyback power supplies operating at a switching frequency of 1 MHz that provide isolation, regulation, and protection.

The advantages of this monolithic approach including high frequency operation and the high level of integration have been discussed in detail. Higher frequency operation has been shown to result in smaller size and wider control loop bandwidths. Few external components, faster current limit, and overtemperature protection have been identified as some of the benefits of the new integrated technology.

The advantages as well as the operating modes of the flyback power supply have been presented in detail. The use of the PWR-SMP3 in flyback power supplies including guidelines for component selection, suggested sources of material, and PC design guidelines have been presented.

APPENDICES

APPENDIX A:
Input Capacitor Selection

The input filter capacitor C_1 of Figure 10 smooths out the full wave rectified AC waveform into the DC voltage required by the power supply. The waveform shown in Figure 12 shows the DC voltage with a superimposed AC ripple voltage. The bridge rectifier conducts current (and charges the capacitor) during a small portion of the sinusoidal input voltage waveform. The capacitor supplies current to the power stage for the balance of the cycle. The capacitor is sized to keep the DC bus within the required ripple voltage limits. Current is drawn from the capacitor in high frequency triangle shaped pulses. The effective input capacitance must provide both energy storage and high frequency bypass.

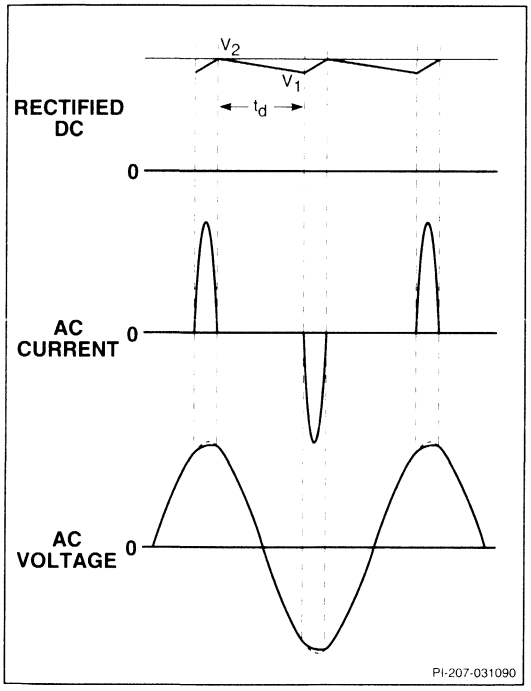


Figure 12. Bridge Rectifier Waveforms.

Capacitors are available in various dielectric materials which dictate size, cost, and reliability. The aluminum electrolytic capacitor offers lowest cost at a moderate size but degrades over time. Metallized film (polyester, polycarbonate, etc.) or metalized paper offer high frequency operation but are the largest in both size and cost. Ceramic capacitors with an X7R or similar dielectric offer the smallest size, high frequency operation, and good long term reliability but at a higher cost. A key disadvantage of the ceramic capacitor is that capacitance values are functions of the bias voltage. The X7R dielectric has a moderate decrease in capacitance with bias voltage and is acceptable for both energy storage and high frequency VS. Ceramic capacitors with a Z5U, Y5U, or similar dielectric should not be used for providing energy storage as their capacitance value drops dramatically with increased voltage. These capacitors can be used as a high frequency VS in parallel with an aluminum electrolytic capacitor.

An expression for the input capacitor C is given by equation 1 in terms of the input power P_{IN}, the peak voltage V_2, the valley voltage V_1, and the effective time t_d between the peak and the valley voltages. Given an input power of 4.6 watts, a peak voltage of 127 volts (from 90 VAC), a valley voltage of 75 volts, and a discharge time of 6 ms (based on 60 Hz input and a conduction angle estimate) the value for C is 5.3 µF.

$$C = \frac{2 \times P_{IN} \times t_d}{\left(V_2^2 - V_1^2\right)} \qquad (1)$$

Applying AC input power to a discharged input capacitor will cause a large surge current to flow. This current can weaken fuses, damages switch contacts, and create noise on the power line. Figure 13 shows the equivalent circuit with series impedances attributed to source impedance, EMI filter impedance, diode dynamic impedance, etc. The impedances appropriate for the application should be estimated to determine the peak of the current surge. Additional series resistance can be added to reduce the peak value with little effect on power supply efficiency due to the low power levels involved.

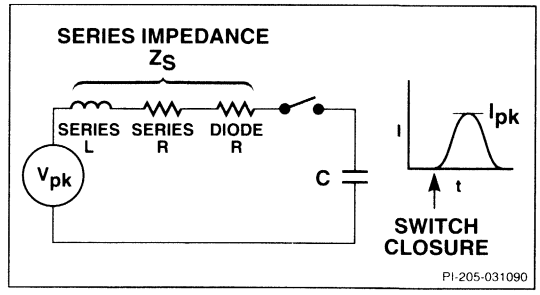


Figure 13. Input Surge Model.

APPENDIX B:
Power Transformer Design Criteria

The power transformer provides energy storage, safety isolation, voltage step down, and feedback. The primary, power secondary, and feedback secondary are shown in Figure 14. This section will describe how to specify the different transformer parameters described below:

- Primary and Power Secondary Inductances
- Feedback/Power Secondary Turns Ratio
- Primary, Power Secondary, and Feedback Secondary Number of Turns
- Maximum Flux Density (B_{max})
- Core Ampere-Turn Capability

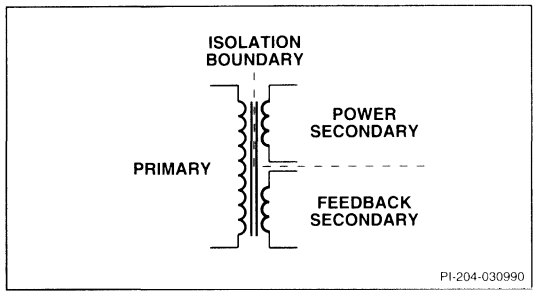


Figure 14. Isolation Transformer Schematic Diagram.

Leakage Inductance

The material best suited for the high frequency power transformer is ferrite. Gapped pot cores are a good choice for a number of reasons: low cost, wide availability, inherent shielding, inductance accuracy, and lower leakage inductance. Other shapes and styles such as the E core tend to have higher leakage inductance while the EP, RM, and PQ cores are more expensive. The toroid core is the poorest choice because of winding costs, excessive leakage inductance (due to the large turns ratios used), and the difficulty in gapping.

Primary and Secondary Inductance Selection

The primary inductance is a function of the minimum input voltage level, the maximum duty cycle, the frequency of operation, and the peak current permissible. The inductance is determined by equation 2. For a minimum DC input voltage V_{min} of 75 volts, a duty cycle D of 0.4, a frequency f of 1 MHz, and a peak primary current I_{PP} of 300 mA the primary inductance L_P is 100 µH.

$$L_P = V_{min} \times \frac{D}{(f \times I_{PP})} \qquad (2)$$

The secondary inductance is sized so that all the stored energy is completely released at the end of each switching cycle. The inductance value is given by equation 3. For an output voltage V_O of 5 volts, a Schottky diode drop V_d of 0.5 volts, an effective "off time" duty cycle D' of 0.5, a frequency f of 1 MHz, and a DC output current I_O of 600 mA the secondary inductance L_S is 1.15 µH.

$$L_S = \frac{(V_O + V_d) \times (D)^2}{(2 \times f \times I_O)} \qquad (3)$$

Feedback/Power Secondary Turns Ratio Selection

The output voltage V_O is related to the feedback voltage V_{BIAS} by the turns ratio of the power winding and feedback winding. The effects of diodes D_2 and D_3 must also be taken into account. The relationship for the turns ratio N_{FS}/N_{PS} as a function of the output voltage V_O, the feedback voltage V_{BIAS}, diode D_2 forward voltage, and diode D_3 forward voltage is given by equation 4. With V_{BIAS} of 8.5 volts, V_{D3} of 0.7 volts, V_O of 5 volts, and V_{D2} of 0.5 volts, the desired turns ratio is 1.673 to 1.

$$\frac{N_{FS}}{N_{PS}} = \frac{(V_{BIAS} + V_{D3})}{(V_O + V_{D2})} \qquad (4)$$

The turns ratio must be implemented with an integer number of feedback and power windings. This turns ratio requires 5 feedback turns and 3 power turns.

A_L Selection/Final Number of Turns

The inductance of the power secondary winding has been established. This information is used to select the core with the proper effective Inductance Index (A_L). A_L is the inductance for a particular core with a 1000 turn winding. Equation 5 gives the relationship for the A_L value as a function of the desired power secondary inductance L_{PS} and the number of power secondary turns N_{PS}. For 1.15 µH and 3 turns the desired A_L value is 128 mH (per 1000 turns).

$$A_L = L_{PS} \times \left(\frac{1000}{N_{PS}}\right)^2 \qquad (5)$$

Achieving this A_L value requires gapping of a standard size core. Cores from different manufacturers will require different gaps due to the minor differences in permeability of the ferrite material (even though the physical dimension of the core are the same).

A better solution is to pick a standard sized core already gapped to an A_L specification and allow the desired inductance to change slightly. The manufacturer adjusts the gap to meet the specification. The user does not have to worry about the size of the gap. Pot cores are available in various sizes with an A_L of 100 mH/1000 T. The new secondary inductance L_{PS} can be calculated using equation 6. With A_L of 100 mH and N_{PS} of 3 turns the new L_{PS} is found to be 900 nH.

APPENDIX B:
Power Transformer Design Criteria

$$L_{PS} = A_L \times \left(\frac{N_{PS}}{1000}\right)^2 \quad (6)$$

The feedback winding inductance can be found from the same equation. With N_{FS} of 5 turns the feedback inductance is found to be 2.5 µH.

The number of primary turns can be calculated from the primary inductance because there is no turns ratio restriction. Using equation 7 with L_P of 100 µH and A_L of 100 mH the primary number of turns is found to be 32 turns.

$$N_P = 1000 \times \sqrt{\frac{L_P}{A_L}} \quad (7)$$

Flux Density Calculation

The flux density B_{max} determines the core loss (power dissipated in the core due to hysteresis and eddy current losses). Determining the appropriate peak flux density analytically is difficult to do. Empirical results and industry "rules of thumb" place the maximum flux density between 300 and 400 gauss (for reasonable core loss) for 1 MHz operation with manganese-zinc ferrite core materials. The peak flux density is given by equation 8 where V_{min} is the lowest DC input voltage, D is the maximum duty cycle, A_e is the cross sectional area of the core (in square centimeters), N_P is the number of primary turns, and f is the switching frequency. For V_{min} of 75 volts, D of 0.4, N_P of 32 turns, f of 1 MHz, and Ae of 0.167 cm^2 (for 1107 pot core) B_{max} is found to be 560 gauss.

$$B_{max} = \frac{V_{min} \times D \times 10^8}{A_e \times N_P \times f} \quad (8)$$

Flux density can be expressed in units of Gauss or Teslas. There are 0.1 MilliTeslas in 1 Gauss. 560 Gauss = 56 MT.

Ampere-Turn Capability

The ampere-turn capability refers to the effective current the core can support before saturation occurs. Data is provided by the manufacturer for each core based on the product of the peak primary current I_{PP} and the number of primary turns N_P as given in equation 9. For a peak primary current of 300 mA and 32 primary turns the capability of 9.6 Ampere-Turns is required. Pot cores gapped for an A_L value of 100 mH typically do not saturate until at least 20 Ampere-Turns.

$$B = \frac{N \times I \times A_L}{10 \times A_e} \quad (9)$$

Leakage Inductance

Leakage inductance is an undesirable parasitic inductance that appears in series with each winding causing voltage spikes, increased power MOSFET switch voltage stress, and degraded load regulation. It is important to minimize leakage inductance as much as possible. Leakage inductance is a measure of the coupling between the primary and secondary windings and depends heavily on transformer construction and spacing. Safety considerations which tend to separate primary and secondary windings also causes leakage inductance to increase. Leakage inductance increases as the square of the number of turns. Reducing the number of turns tends to lower leakage inductance but increases core loss by running higher flux densities.

Leakage inductance is measured across the primary winding with the power secondary shorted. The measured value is the primary referenced total leakage inductance L.

The construction tips given below will reduce leakage inductance to acceptable levels for 3 watt applications.

Power Transformer Construction Details

High frequency transformers should be constructed with self shielding core shapes such as pot cores. The windings are wound on bobbins as indicated below:

- Wind primary in single, uniform layer with no overlap.
- Wind feedback secondary in single, uniform layer over primary.
- Insulate with 1 or more layers tape and/or paper as required by the appropriate safety specification.
- Wind power secondary litz wire windings to completely cover the primary winding.
- Tape windings in place and assemble transformer.

APPENDIX C:
Clamp Component Selection

The clamp circuit limits voltage spikes on the turn off transition of the power MOSFET switch. The voltage spikes are caused by the power transformer leakage inductance. Current flowing in the primary while the power switch was turned on induces a voltage spike when the power switch is turned off. The voltage spike is the effect of the primary leakage inductance trying to maintain current flow in the primary while the secondary leakage inductance tries to block current flow to the secondary.

The amount of energy that must be dissipated by the clamp circuit is a function of the magnitude of both the leakage inductance and the primary current. For low leakage transformers the voltage spike may be low enough that the circuit actually clamps only in over current situations. Higher leakage transformers may require clamping of the voltage spike during normal steady state operation which would dissipate more energy and require a higher power rating on the clamp circuit. The clamp circuit can be implemented with a high-voltage Zener diode or a parallel resistor network. The capacitor can be relatively small (typically 1 nF) and the resistor is calculated by the desired dissipation and leakage inductance/current values.

Some applications may not require the clamp circuit. These applications would typically operate at lower levels of primary current (and hence lower power levels), have lower maximum values of input voltage (such as 48 VDC), or sacrifice the current limit function for overall lower power supply cost. For overall reliability over worst case line, load, temperature, and fault conditions the use of the clamp circuit is recommended.

Zener Diode Selection

The avalanche breakdown voltage of zener diode D_4 is chosen high enough to minimize losses and low enough to prevent breakdown of the MOSFET power switch. The first step is to establish the magnitude of the reflected output voltage that occurs when the power switch is turned off. The output voltage is reflected back to the primary with a magnitude given by equation 10 where N_P is the primary number of turns and N_{PS} is the power secondary number of turns. For a 32 turn primary, 3 turn power secondary, 0.5 volt diode drop, and 5 volt output voltage the reflected output voltage V_{OP} is 59 volts. The Zener diode voltage must be higher than this value.

$$V_{OP} = (V_O + V_d) \times \frac{N_P}{N_{PS}} \qquad (10)$$

The maximum value for the Zener diode is a function of both the breakdown voltage of the power MOSFET switch and the input voltage as given in equation 11. For a drain-source voltage V_{DS} of 350 volts and a maximum input DC voltage of 200 volts the maximum Zener voltage should be 150 volts. A Zener voltage of 100 volts would be a suitable choice.

$$V_Z = V_{DS} - V_{IN} \qquad (11)$$

The last step for selecting the Zener diode is to establish the power dissipation. The conduction time D t for the Zener diode is calculated with equation 12 from the Zener voltage V_Z, the reflected output voltage V_{OP}, the peak current I_{PP}, and the primary referenced total leakage inductance L. For a leakage inductance of 6 µH, a peak current of 300 mA, a Zener voltage of 100 volts, and a reflected output voltage of 59 volts the conducted time Δ t is 44 ns.

$$\Delta t = \frac{L \times I_{PP}}{V_Z - V_{OP}} \qquad (12)$$

The power dissipated in the Zener diode is simply the product of the Zener voltage V_Z and the average value of the Zener current as shown in equation 13. For the values given above and a frequency of 1 MHz the power dissipation is found to be 660 mW.

$$P = \frac{V_Z \times I_{PP} \times \Delta t \times f}{2} \qquad (13)$$

This dissipation can be reduced by using techniques to minimize the leakage inductance of the transformer. Cutting the primary and secondary turns by 33% reduces the leakage inductance to less than half the original value.

Example:

A 2 turn power secondary on a core with an A_L value of 250 mH/1000 T will develop 1 µH as required. 20 turns on the primary will generate 100 µH. The leakage inductance will be cut approximately in half reducing the clamp loss to 330 mW. The reduced clamp loss will be offset somewhat by increased transformer core loss due to the 60% higher flux density. The feedback voltage V_{BIAS} will require special consideration. The feedback winding can provide only a limited number of voltages due to the small number of turns. A 4 turn feedback secondary will generate a nominal 10.3 volt feedback voltage. The resistor divider in the feedback network will have to be adjusted to generate the proper output voltage. An external circuit must also be used to drop the new feedback voltage to properly bias the PWR-SMP3 at the recommended operating level of 8.5 volts.

Blocking Diode Selection

The blocking diode D_5 prevents current flow through the clamp when the MOSFET switch is turned on. This diode should have a blocking voltage capability of 400 volts, a reverse recovery time less than 400 ns, and an average forward current capability of at least 100 mA.

APPENDIX D:
Output Rectifier Selection

A Schottky diode is most appropriate for rectifier D_2. The low forward voltage drop and low series impedance are both necessary for accurate regulation. In addition the high turns ratio required for discontinuous operation results in low reverse voltages. The most important parameters are the reverse breakdown voltage, forward voltage versus current characteristic, and power rating.

Reverse Voltage

The steady-state reverse voltage seen by the diode when the power switch is on equals the sum of the output voltage V_O and transformer voltage. The transformer voltage is a function of the input voltage and turns ratio. The reverse voltage requirement V_r is given in equation 14 where N_P is the number of primary turns, N_{PS} is the number of power secondary turns, and SR is a stress ratio applied for reliability considerations. For a nominal input voltage of 170 VDC, 32 primary turns, 3 secondary turns, 80% stress ratio, and 5 volt output the reverse voltage requirement is 26 volts DC.

$$V_r = \frac{V_O + \left(V_{IN} \times \frac{N_{PS}}{N_P} \right)}{SR} \qquad (14)$$

The reverse voltage must then be checked for worst case DC input voltage. A 200 VDC maximum input voltage (and setting the stress ratio to 100%) produces a V_r of 24 volts.

The capacitance of the output diode forms a resonant circuit with the leakage inductance of the power secondary. In continuous mode, the current in the diode is rapidly switched which excites the resonant circuit and causes voltage spikes to be superimposed on the transformer voltage . The spike tends to be suppressed in discontinuous mode converters but could occur in current limit where the continuous mode of operation is possible. The reverse voltage of the rectifier must be increased depending on the magnitude of the spike. A 5 volt spike superimposed on the maximum V_r of 25 volts would require a 30 volt breakdown. A suitable part would have a breakdown voltage of at least 40 volts. However, most Schottky diodes have an avalanche rated junction in parallel with the Schottky junction to absorb low energy voltage spikes.

Forward Voltage Characteristics

The output voltage specification determines the requirements for diode forward voltage characteristics.

The peak secondary current and the dynamic impedance of the diode creates a voltage drop which reflects back into the feedback circuit, creates an error term, and degrades regulation. A tight regulation specification may require a diode with a steep voltage vs current curve in the active region. The active region is determined by the peak secondary currents for the load range of interest. The steepness of the curve depends on the voltage change allowable to meet the regulation specification. An error budget should be determined which assigns acceptable deviations to those circuits producing error.

Example:

A 5 volt, 3 watt application with a load variation of 20% to 100% and a regulation specification of 4.75 to 5.25 volts may have a peak current range of 550 mA to 2.7 A. Assigning 20% of the total allowable error to the forward diode characteristic results in a voltage deviation of 100 mV for the peak current range.

Forward Biased Power Dissipation

The forward biased power dissipation occurs when current is flowing through the power secondary winding. The current waveform has a peak value which is much larger than the average value. The average value of the diode current is equal to the DC load current. An approximation of the forward power dissipation is given in equation 15 where V_d is the forward drop of the diode at the maximum peak current and I_{avg} is the average current. For a forward drop of 0.4 volts and an average current of 600 mA the forward power loss is found to be 240 mW.

$$P_D = V_d \times I_{avg} \qquad (15)$$

A more accurate value for the power dissipation can be determined by taking into account the slight voltage change with current level by either graphical or analytical integration.

APPENDIX E:
Output Capacitor Selection

The output capacitor C_2 of Figure 10 provides filtering required to maintain the DC output voltage. This capacitor provides the entire load current while the power switch is on and current flows in the power transformer primary. When the power switch is off current flows in the power secondary winding. Some of this current charges the capacitor back up to the proper output voltage level while the remainder is delivered to the load.

Ceramic surface-mount capacitors in either Z5U or X7R dielectrics are a good choice for this application. Ceramic capacitors have good high frequency characteristics and occupy minimal physical volume. The parasitic series impedance is low due to the lack of wire leads. The Z5U dielectric is cost effective for applications that do not require operation over wide ranges of temperature. Operation over a wide temperature range requires the stability of the X7R. Ceramic capacitors with wire leads can be used as long as the leads are kept short.

Tantalum or aluminum electrolytic capacitors have high values of ESR (equivalent series resistance) and ESL (equivalent series inductance) which make them difficult to use in high frequency application. ESR and ESL lead to higher values of ripple voltage. Reducing ESR and ESL to acceptable levels to meet low ripple voltage specifications requires larger case sizes and high quality dielectrics. These types of capacitors are not recommended for this application.

The capacitance value is chosen such that the output ripple voltage requirement is met while the capacitor sources the entire load current. The worst case ripple occurs at high line and load since these conditions produce the smallest duty factor and highest load current. The load can be modeled as a constant current source. The capacitance C can be calculated by using Equation 16 where I_O is the DC output load current, DV is the peak to peak ripple voltage allowable, and D t is the off time for the power switch.

$$C = I_O \times \frac{\Delta t}{\Delta V} \qquad (16)$$

Example:

For a current of 600 mA, a voltage change of 100 mV, and time of 750 ns the value of required capacitance is 4.5 µF.

Higher accuracy can be obtained by calculating the additional increment of time when the switch is on and the diode current is less than the load current. In this condition the load current is supplied by both the power secondary and the capacitor.

Ceramic capacitors also have ESR and ESL. A somewhat larger capacitor may be required to meet the ripple voltage specification depending on the manufacturer chosen.

APPENDIX F:
Stability Analysis
Discontinuous Mode

A complete treatment of this subject is beyond the scope of this paper and can be found elsewhere[2]. Equations and models will be stated here without proof.

The design of the feedback control loop system is straightforward as long as the converter stays in discontinuous mode. In discontinuous mode and at less than half the switching frequency the power stage has a single pole rolloff. Should the converter enter the continuous mode the frequency response will have two poles and a right half plane zero which require a more complex compensation scheme, reduce the overall bandwidth, and degrade transient response and line rejection.

Loop gain is the term given to the gain found by multiplying all the gains around the closed feedback loop. This gain must be reduced to less than 0 db before the loop phase reaches -180 degrees. The elements that make up the loop gain are shown in Figure 15 and include terms involving the pulse width modulator, power transformer, power filter, and the compensated error amplifier.

There are two terms that must be defined before the loop gain equations can be written: the DC voltage gain M and dimensionless term K. M is given by equation 17 where V_{IN} is the DC input voltage, V_O is the output voltage, N_P is the number of primary turns, and N_{PS} is the number of power secondary turns. The dimensionless term K is given by equation 18 where L_P is the primary inductance, R is the load resistance, and f_S is the switching frequency.

$$M = \frac{V_O}{V_{IN}} \times \frac{N_P}{N_{PS}} \qquad (17)$$

$$K = \frac{2 \times L_P \times f_S}{R \times \left(\frac{N_P}{N_{PS}}\right)^2} \qquad (18)$$

The pulse width modulator gain is a transconductance term which converts the control voltage to a modulated current source. Equation 19 gives the modulator gain G_{PWM} in terms of the maximum duty cycle D_M, the voltage V_M required to sweep the duty cycle from 0 to the maximum value, the output voltage V_O, the load resistance R, K, N_P, N_{PS}, and M.

$$G_{PWM} = \frac{\frac{D_M}{V_M} \times 2 \times V_O}{R \times \frac{N_P}{N_{PS}} \times \sqrt{K} \times M} \qquad (19)$$

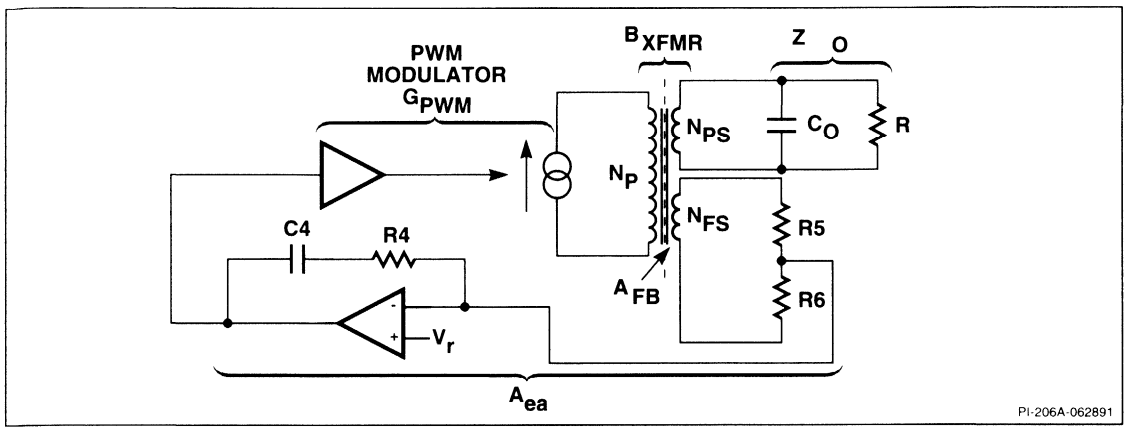


Figure 15. Loop Gain Elements.

APPENDIX F:
Stability Analysis

The flyback transformer steps up the current and produces a gain term of its own. The gain through the transformer, B_{XFMR}, is given in equation 20 where N_P is the number of primary turns and N_{PS} is the number of power secondary turns.

$$B_{XFMR} = \frac{N_P}{N_{PS}} \qquad (20)$$

The modulated current source previously described is amplified by the power transformer and applied to the parallel impedance formed by the load resistance and output capacitance to generate the modulated output voltage. The parallel impedance Z_O of the output filter is given by equation 21 where R is the load resistance, C_O is the power supply output capacitance, and S denotes complex impedance. Note that the load resistance is divided by 2 (characteristic of discontinuous flyback power supplies). Note also that the impedance has a frequency response with a pole determined by R and C_O.

$$Z_O = \frac{\frac{R}{2}}{1 + \left(\frac{R}{2} \times C_O \times S\right)} \qquad (21)$$

The turns ratio between the power and feedback winding introduces a voltage gain term A_{FB}. This term is given in equation 22 where N_{PS} is the number of power secondary turns and N_{FS} is the number of feedback secondary turns.

$$A_{FB} = \frac{N_{FS}}{N_{PS}} \qquad (22)$$

The gain of the compensated error amplifier is the final term in the loop gain. The gain characteristic is determined by the compensation network shown in Figure 15. The magnitude G_{ea} as a function of component values R_5, R_4, and C_4 is given by equation 23. Note that the AC gain is independent of the value of R_6. This gain is frequency dependent and is characterized by a pole at DC and a zero determined by the values of R_4 and C_4.

$$A_{ea} = \frac{-1}{S \times R_5 \times C_4} \times \left(1 + \left(R_4 \times C_4 \times S\right)\right) \qquad (23)$$

Low f Term Zero Term

The total loop gain T is found by multiplying each gain term:

$$T = G_{PWM} \times B_{XFMR} \times Z_O \times A_{FB} \times A_{ea} \qquad (24)$$

The loop gain T must be established at all combinations of line voltage and load resistance to ensure stability.

APPENDIX F:
Stability Analysis

Example:

A power supply circuit has an input voltage of 150 volts DC and a load resistance of 42 Ω (20% of 3 W maximum).

From equation 17 with V_{IN} of 150 volts, V_O of 5 volts, N_P of 32 turns, and N_{PS} of 3 turns, the value of M is found to be 0.356.

From equation 18 with L_P of 100 μH, f_S of 1 MHz, R of 42 Ω, N_P of 32 turns, and N_{PS} of 3 turns, the value of K is found to be 0.0419.

The pulse width modulator gain G_{PWM} is found from equation 19 to be 0.126 with D_M of 0.4, V_M of 1, V_O of 5, R of 42, N_P of 32, N_{PS} of 3, and the constants K and M as found above.

The power transformer gain term B_{XFMR} is found to be 10.7 from equation 20 with N_P of 32 and N_{PS} of 3.

The impedance term can be broken into two different terms: the DC impedance and the pole frequency where the impedance begins to roll off. The DC impedance is found to be 21 Ω from equation 21 with R of 42 Ω and S defined to be zero. The pole frequency is determined by the point at which the complex term in the denominator of equation 21 is equal to the real term. With R of 42 Ω and C_O of 4.5 μF the pole frequency is found to be 1.7 kHz.

The feedback winding gain term is found to be 1.67 from equation 22 with N_{FS} of 5 and N_{PS} of 32.

The compensated error amplifier gain characteristic can also be broken into two different terms: the low frequency gain term which is rolling off at a single pole rate and the zero frequency where the gain breaks to a flat response. The low frequency gain term A_{ea}' given in equation 25 is derived from equation 23 with R_5 of 18.2 kΩ, C_4 of 2200 pF, and the magnitude of S defined as (2 pf):

$$A_{ea}' = \frac{3975}{f} \qquad (25)$$

The zero frequency is found to be 39.7 kHz from equation 23 with C_4 of 2200 pF and R_4 of 1.82 kΩ.

The total loop gain T will consist of a low frequency gain term modified by the additional pole and zero determined above. The low frequency gain will be a function of frequency and roll off at the rate of a single pole. The low frequency gain T_{lf} given in equation 26 is calculated from equation 24 with G_{PWM}, B_{XFMR}, $Z_{O(DC)}$, A_{FB}, and A_{ea}' determined above.

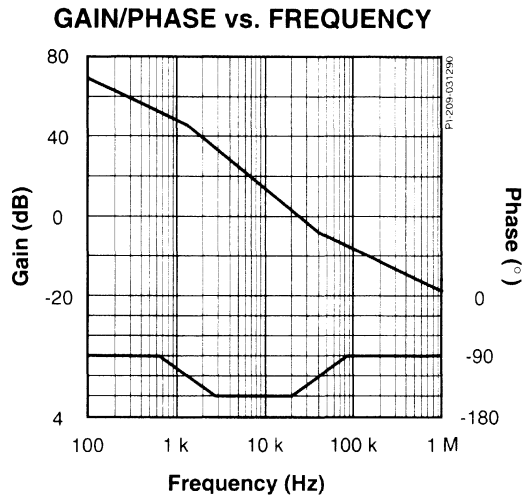


Figure 16. Control Loop Frequency Response.

$$T_{lf} = \frac{188,000}{f} \qquad (26)$$

Bode techniques can now be used to examine the frequency response characteristics. The low frequency loop gain can be calculated for a specific frequency. For example: the gain at a frequency of 120 Hz is 1567 or 64 dB. The gain response is plotted by drawing a straight line with a 20 db/decade rolloff through the 64 db point at 120 Hz as shown in Figure 16. The next step is to introduce the effect of the pole in the output filter impedance. Find the spot on the line that crosses the pole frequency of 1.7 kHz. Draw a line from this point with a 40 db/decade rolloff. The last step is to add in the effect of the zero in the compensation network. Find the spot where the new line crosses the zero frequency of 39.7 kHz. Start a new line with a rolloff of 20 db/decade.

The phase response can be estimated from the pole and zero locations by using tables for single pole responses. The pole tends to increase the phase shift. At the pole frequency of 1.7 kHz the phase shift will be 135 degrees. The phase will continue to shift beyond the pole frequency and approach 180 degrees. The high frequency zero will begin to pull the phase shift back towards 90 degrees. At the zero frequency of 39.7 kHz the phase shift should be back down to 135 degrees. Beyond the zero the phase shift will approach 90 degrees.

APPENDIX F:
Stability Analysis

Phase margin is defined where the gain curve crosses the 0 db axis. Phase margin is the difference between the loop phase shift and 180 degrees. The phase margin for this example is found from Figure 14 to be 30 degrees. Phase margin can be increased by moving the zero to a lower frequency. The phase margins will improved with heavier loads due to the upward shift in the pole frequency of the output filter.

The gain crossover point should be kept below the switching frequency by a factor of at least 4 to maintain the single pole rolloff characteristic of discontinuous conduction.

Continuous Mode

The continuous mode of operation is more difficult to stabilize. The power stage no longer has a single pole frequency response. Flyback power supplies in continuous conduction mode are characterized by a second order frequency response that includes a pair of complex poles and a right half plane zero.

The complex poles are associated with the inductance of the transformer power secondary winding and the output capacitance. Pulse width modulation varies the "effective" value of the inductance causing the corner frequency of the complex pole pair to change as a function of duty cycle.

The right half plane zero has a gain characteristic that will increase with frequency at 20 db/decade while the phase characteristic decreases from 0 to 270 degrees. The corner frequency of the right half plane zero also changes as function of both duty cycle and load.

Dominant pole compensation can be used to stabilize the feedback system. This requires rolling off the loop gain below 0 db before the poles and zero contribute significant phase shift. This tends to reduce the bandwidth of the control loop which degrades transient response and ripple rejection.

For a detailed treatment of continuous conduction mode see reference (2).

APPENDIX G:
Gate Charge Analysis

Charging a conventional MOSFET gate requires an amount of energy E_C given by equation 27 where C_C is the input capacitance of the conventional MOSFET and V_C is the voltage level required for full enhancement.

$$E_C = \frac{1}{2} \times C_C \times V_C^2 \qquad (27)$$

The energy E_P to charge a Power Integrations's MOSFET is given by equation 28 where C_P is the input capacitance of the integrated MOSFET and V_P is the voltage level required for full enhancement.

$$E_P = \frac{1}{2} \times C_P \times V_P^2 \qquad (28)$$

The reduction in energy required to drive the MOSFET gates can be expressed as a ratio of the energy terms as shown in equation 29.

$$\text{Reduction} = \frac{E_P}{E_C} \qquad (29)$$

With one third the input capacitance and one half the required gate voltage the ratio of the energy reduction is found to be 0.083.

REFERENCES

1 U.S. Patent # 5,008,794
2 Advances in Switched-Mode Power Conversion, TESLAco Power Electronic Series, Vol. 1, 1981

Custom Transformers for the PWR-SMP Family

APPLICATION NOTE AN-7

Specifying transformers to a knowledgeable vendor is considerably easier than designing them from scratch. The purpose of this document is to present enough information for a transformer to be completely specified without requiring design at the magnetic circuit level. Transformer vendors understand hysteresis curves, flux density, ampere-turn capability, core loss and current density, but may not have the insight regarding how the transformer is actually intended to be used.

Basic Flyback Transformer

The basic flyback power transformer is shown in Figure 1. Three separate windings and a shield are wound on a common core. The primary winding stores energy in the transformer core, the power winding transfers the energy from the core to the load, and an auxiliary winding to provide bias power to the integrated circuit. The auxiliary winding may also be used for regulation (see Design Aid AN-8). The shield reduces Electro-Magnetic Interference (EMI).

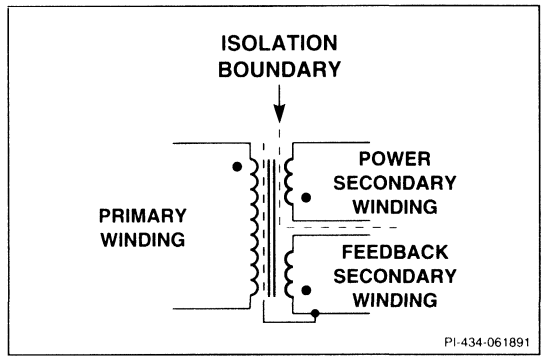


Figure 1. Schematic Diagram of the Three Transformer Elements.

What Information is Needed?

Since 5 V is the most commonly requested output voltage, a standard 5 V single-output transformer has been optimized for each member of the PWR-SMP family. DA-3 gives a list of transformer manufacturers who have worked with Power Integrations to provide these as standard, "off-the-shelf" items.

These standard transformers can also be used as the basis for other "custom" designs based on specific output voltage and current requirements. As an example, several variations of the standard T1002 transformer design are given at the end of this application note. If, for some reason, these standard transformers cannot be used as the basis for a "custom" design, then additional data must be provided to the vendor.

When working on a custom design, the transformer vendor needs certain information about the application to develop the proper transformer. This information can be broken down into two categories. The first set of parameters is electrical in nature and determines factors such as core cross section, core path length, number of turns per winding, and gauge of magnet wire. These parameters are developed as a by-product of the power and thermal analysis presented in AN-9.

The parameters are:

- Primary Inductance
- Primary to Power Winding Turns Ratio
- Maximum Peak Primary Current
- DC Load Currents on Each Output Winding
- Minimum DC Input Voltage
- Maximum Duty Cycle
- Frequency of Operation

The second set of information is mechanical in nature and determines the type of core, PC footprint, temperature rise, and safety rating of the finished transformer. The determination of these parameters is the subject of this application note:

- Number of Auxiliary Windings
- Turns Ratios on Auxiliary Windings
- Primary Winding Technique
- Feedback Winding Placement
- EMI Considerations
- Conformal Coating
- Safety Requirements
- Insulation Systems
- Coupled Inductor Considerations

Turns Ratios

The primary to main power secondary turns ratio is established during the power and thermal analysis. Turns ratios must then be established between the main power secondary and the auxiliary windings, which includes the feedback winding. The relationship between the main power winding and an auxiliary winding is shown in Figure 2. Current flows solely in the primary winding when the power MOSFET switch is on. Current flows in all the other windings (main power winding and auxiliary windings) when the switch is off. The winding with the lowest impedance determines the voltage on all other windings during this time.

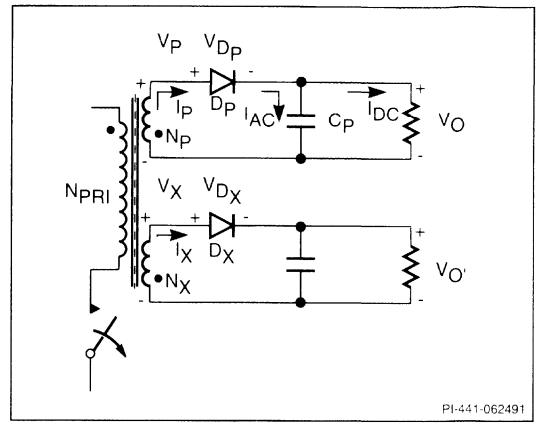


Figure 2. Secondary Currents and Voltages with the Switch in the off-state.

Energy stored in the transformer core induces a current (I_P) to flow in the power winding when the switch is off. This current causes a diode voltage drop (VD_P) across the power rectifier (D_P). The power winding current then splits into an AC component flowing into capacitor (C_P) and a DC component flowing out to the load. Capacitor C_P is chosen large enough that the AC current causes a negligible change in the output voltage (V_O). The voltage across the power winding (V_P) is equal to the sum of VD_P and V_O:

$$V_P = VD_P + V_O \quad (1)$$

V_P reflects across to the auxiliary winding (V_X) by the ratio of the number of power turns (N_P) to auxiliary turns (N_X):

$$V_X = V_P \times \left(\frac{N_X}{N_P} \right) \quad (2)$$

The auxiliary output voltage (V_O') is simply the difference between V_X and the auxiliary diode drop (VD_X):

$$V_{O'} = V_X - VD_X \quad (3)$$

Combining equations 1-3 and rearranging yields a formula for the turns ratio from the auxiliary winding to the power winding as a function of voltages and diode voltage drops:

$$\frac{N_X}{N_P} = \frac{(V_O + VD_X)}{(V_O + VD_P)} \quad (4)$$

The magnitude of the diode voltage drops depends on the reverse voltage found on each winding. Schottky diodes have a voltage drop typically between 0.4 and 0.5 volts but are usually constrained to output voltages of 10 volts by their reverse voltage rating. Higher voltage ultra-fast recovery rectifiers are used for output voltages above 10 volts and have a forward drop between 0.6 and 0.8 volts.

A reverse voltage appears across each winding when the power switch is on as shown in Figure 3. The diodes must have a sufficient blocking rating voltage to withstand this reverse voltage. The reverse voltage (V_R) can be calculated given the following parameters: power winding to primary winding turns ratio, auxiliary winding to power winding turns ratio, maximum DC input voltage (V_{MAX}), and the auxiliary output voltage:

$$V_R = \left(V_{MAX} \times \left(\frac{N_P}{N_{PRI}} \right) \times \left(\frac{N_X}{N_P} \right) \right) + V_O \quad (5)$$

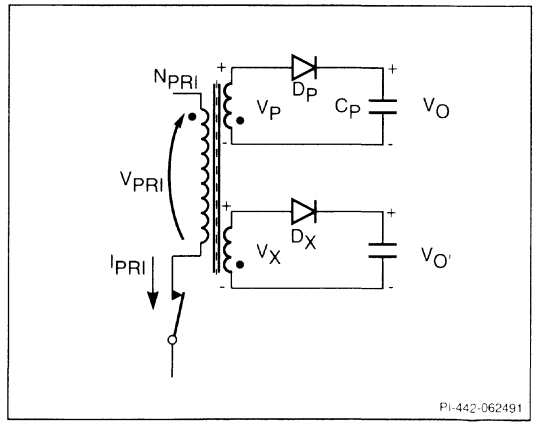


Figure 3. Secondary Currents and Voltages with the Switch in the on-state.

Primary Winding Techniques

The transformer vendor will derive the number of primary layers required by determining the number of turns and wire gauge for a given design on a given core. Cores come in a variety of shapes and sizes. The selection of the core shape will depend on cost, overall size, and whether or not the transformer will be built using automated assembly techniques. Special considerations must be given to both single layer and multiple layer winding constructions to minimize parasitic capacitance and system noise.

Single Layer Winding

Most cores (with the exception of the toroidal core) have an accompanying bobbin on which the windings are wound. The cross sectional view shown in Figure 4 shows a single layer primary, a shield, and a single layer secondary. The accompanying circuit shows the parasitic capacitance terms associated with the transformer. Each winding has two types of distributed capacitance terms: winding to shield and winding to winding. Energy, which is proportional to the square of the peak AC voltage, is stored in these parasitic capacitances during each cycle. This energy is lost each time the power MOSFET switch turns on, creating a switching or AC power loss (see AN-7).

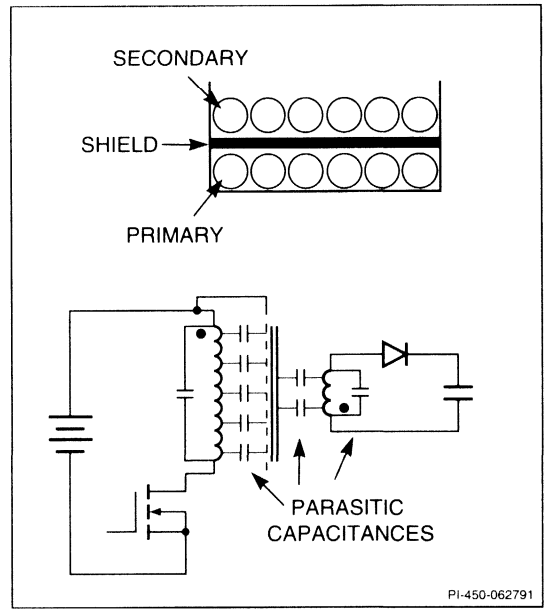


Figure 4. Single Layer Winding Capacitances.

Each winding has a "quiet" end connected to either a DC source or return and a "noisy" end with considerable AC voltage swing. On the primary side, the winding to shield capacitance near the MOSFET drain will have significant current flow, while that near the high-voltage bus will have no current flow. The same is true for the secondary side, though the "noisy" end will be the end connected to the diode.

These parasitic capacitance terms limit the switching frequency at which the power supply can operate. Figure 5 shows the impedance of the primary winding of the T1002 transformer (see DA-3) with all other windings open. The impedance rises with frequency due to the magnetizing inductance, reaches a resonant point determined by inductance and capacitance, and then falls with increasing frequency due to the parasitic capacitance. The switching frequency should be selected well below resonance. Minimizing the parasitic capacitance of the transformer winding reduces the switching or AC losses and allows for higher frequency operation.

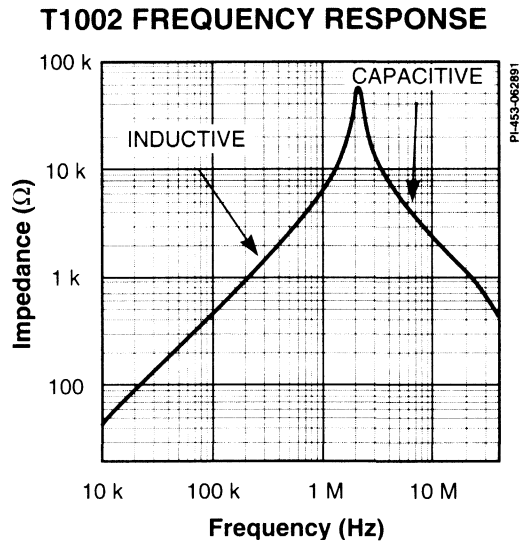


Figure 5. Plot of Frequency Response for the T1002 Transformer.

Widest bandwidth and highest frequency of operation can be achieved with single layer windings. Cores for this type of winding are typically low profile with relatively long bobbins.

Sometimes a single layer is insufficient to accommodate either the number of turns or the gauge of wire required. In this case multiple layer winding techniques must be used. Careful consideration of the winding capacitance, the "noisy" end of the winding, and the resultant energy stored is required.

Multiple Layer Windings

A double layer winding with additional parasitic capacitance is shown in Figure 6. There will be a distributed capacitance between the two layers similar to the winding to shield capacitance described above. Steps must be taken to minimize the AC potential between these two layers as well as between the top layer and the shield.

Figure 6(a) shows a double layer winding with minimal effects of stray capacitance. The top layer adjacent to the shield is the quieter half of the winding where one end has no AC voltage and the other has only half the AC voltage appearing at the power MOSFET drain. The maximum AC voltage between the windings is half the value of the MOSFET drain voltage and is constant over the width of the winding. The energy stored by the parasitic capacitance is uniformly distributed across the winding.

Figure 6(b) illustrates a poorly wound double layer winding. The "noisiest" half of the winding is located near the shield where one end has half the MOSFET drain AC voltage and the other end has the full drain AC voltage. The AC voltage between the windings varies linearly across the width of the winding. The full drain AC voltage exists at one end and no AC voltage exists at the other end. More energy is stored at one end of the winding due to the higher AC potential. Total stored energy is higher than the previous example because of the square law dependence on the peak AC voltage. The energy stored and released from the distributed capacitance each switching cycle is higher with this winding technique.

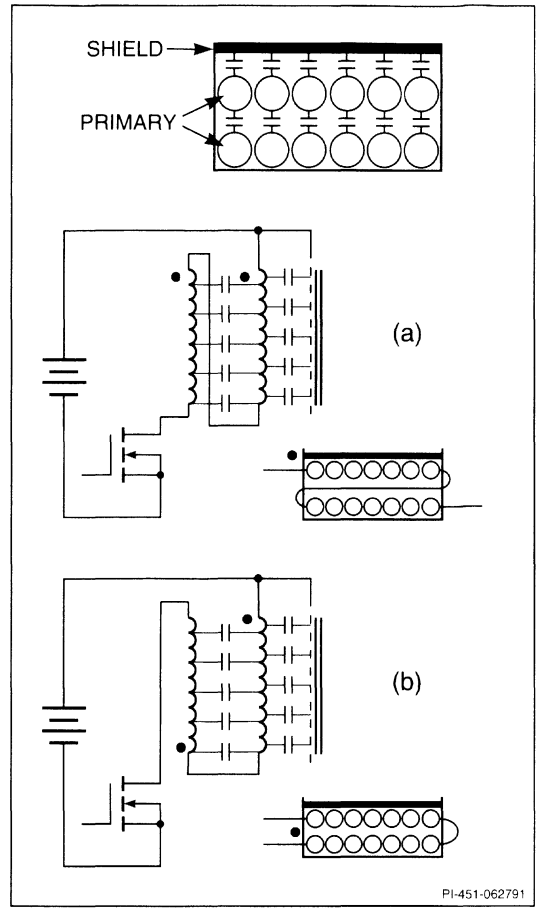


Figure 6. Multi-layer Winding Example.

Bias Winding Isolation

Proper positioning of thebias auxiliary winding will reduce capacitive coupling and noise currents to the primary bias and feedback circuitry. The circuit diagram shown in Figure 7 illustrates the parasitic capacitance between the primary and bias windings. The key is to locate the bias winding over a "quiet" part of the primary winding to minimize the AC voltage between the windings. Figure 7(a) shows proper placement of the bias winding for a single layer primary. Note that the bias winding is wound beneath the "quiet" side of the primary winding. Figure 7(b) illustrates proper placement for a multiple layer primary winding. Note that the bias winding is wound over the "quiet" side of the primary winding.

Tape Between Layers

One layer of thin polyester film tape (3M #78 - 0.8 mil) is recommended between each distinct winding and between each winding and the shield. This layer of tape protects the enamel coating of the magnet wire from abrasion and helps ensure the integrity of the insulation between windings.

EMI Considerations

Electromagnetic interference as well as system noise levels can be reduced with a foil copper shield wound between the primary and secondary windings. The shield can be connected to either the high voltage DC bus or the primary reference as shown in Figure 8. Grounding the core to the primary reference will improve the shielding effects of the transformer even further. These connections are especially important in applications without an overall shielded enclosure or 2 wire AC input where earth ground is not available.

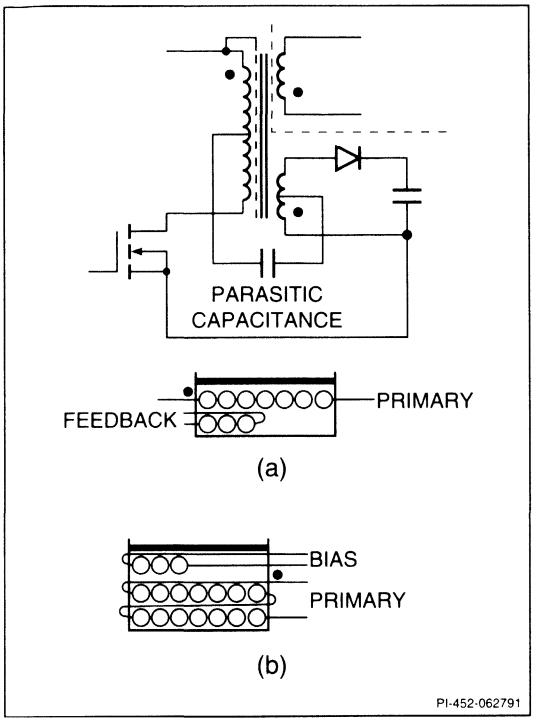


Figure 7. Proper Placement of the Feedback Winding.

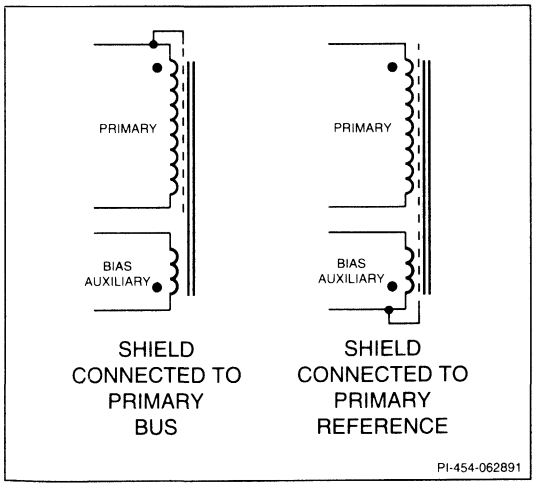


Figure 8. Building the Transformer to minimize EMI.

Conformal Coating

Conformal coating with epoxy or some other resin can be used to improve the electric strength between the primary and secondary windings. High voltage breakdown performance can be improved when the transformer is properly encapsulated. Protection for fine magnet wire connections is an additional benefit.

Safety Considerations

Safety agencies such as UL, CSA, VDE, and TUV specify both the electric strength between primary and secondary windings and the minimum distances between primary and secondary windings. Creepage and clearance distance are described in the design aid on Safety and Layout (DA-2).

Insulation Systems

Two transformer insulation systems will be presented that meet the safety requirements of the North American and European agencies.

Margin Wound Transformers

A typical margin wound transformer is shown in Figure 9. Margins are placed between the edges of each winding and the walls of the bobbin. The distance M depends on the input voltage, type of equipment, and safety agency requirements. The shield is considered primary circuitry and stays within the margin limits as shown. A reinforced insulation layer is placed between the primary and secondary windings and extends beyond each margin all the way to the bobbin flange. Typical construction for the reinforced insulation layer uses three layers of UL recognized polyester film tape (3M #1298) cut to the full width of the bobbin.

Creepage distance is measured from the end of the primary winding to the end of the secondary winding around the edge of the reinforced insulation layer. Typical commercial or consumer equipment requires a total creepage distance of 3.0 mm (0.118 inches) for 110 VAC and 5.0 mm (0.197 inches) for 220 VAC applications. The distance M is actually half the specified creepage distance. The creepage and clearance distances must also be maintained as the wire exits the bobbin and terminates to a pin.

Margin winding is the preferred approach for transformers with more than two output voltages of significant power capability. Higher voltage outputs (above 12 volts) are also best served by margin wound transformers.

Insulated Wire Transformers

A typical insulated wire transformer is shown in Figure 10. No margins are required between the primary and secondary windings for creepage and clearance because the secondary is insulated with UL or VDE rated wire. All windings and the shield cover the bobbin from flange to flange.

Note that termination of the insulated wire is subject to the creepage and clearance requirements stated above. The creepage and clearance dimensions are measured from where the insulation system exposes the secondary conductor (from the point the insulation is stripped from the wire). For North American applications UL 1430 wire is used. A special wire is available with three individual layers of insulation for European or Universal input applications. Agency-approved wire vendors are listed at the end of this document.

This technique is generally appropriate for small transformers with one or two low voltage outputs of 12 V or less although single output transformers to 24 V have been constructed.

Coupled Inductor Considerations

The coupled inductor feedback approach (discussed in AN-8) is effectively implemented by combining the toroid core with the power transformer in a single unit as shown in Figure 11. Overall cost is less and the electric strength requirement can be verified with a single test by the transformer vendor.

The coupled inductor works best with the insulated secondary approach. The toroid is treated as a primary circuit requiring safety insulation between the conductors. Shrink tubing can be substituted if insulated wire is not used but will be cumbersome to build. The toroid core should be fastened as close to the transformer core as possible to achieve proper creepage and clearance distances.

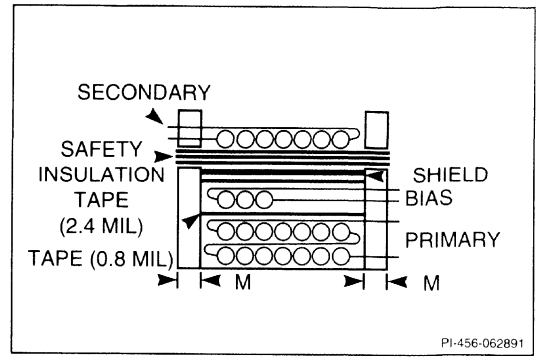


Figure 9. Margin Wound Transformer Cutaway View.

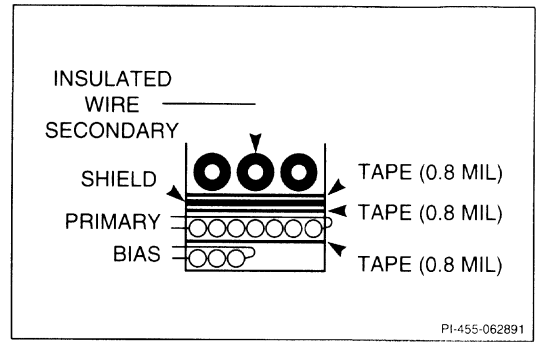


Figure 10. Insulated Wire Transformer Cutaway View.

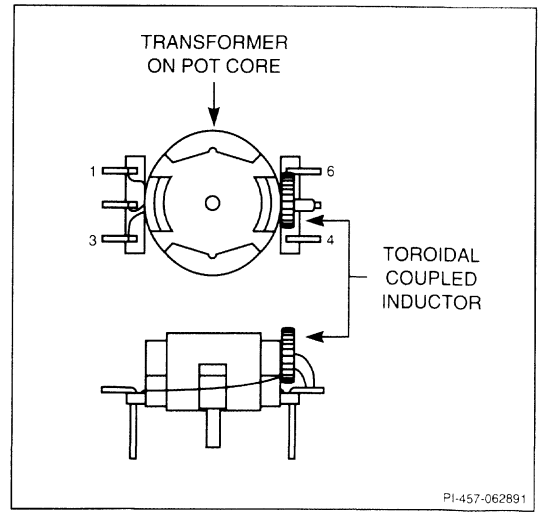


Figure 11. Coupled Inductor Transformer for Better Regulation.

Cookbook Variations

The T1002 transformer is the most versatile member of the standard transformer family. "Custom" variations of the base transformer yield several different output configurations without any major redesign. Variations of the single output transformer are shown here for use in various applications.

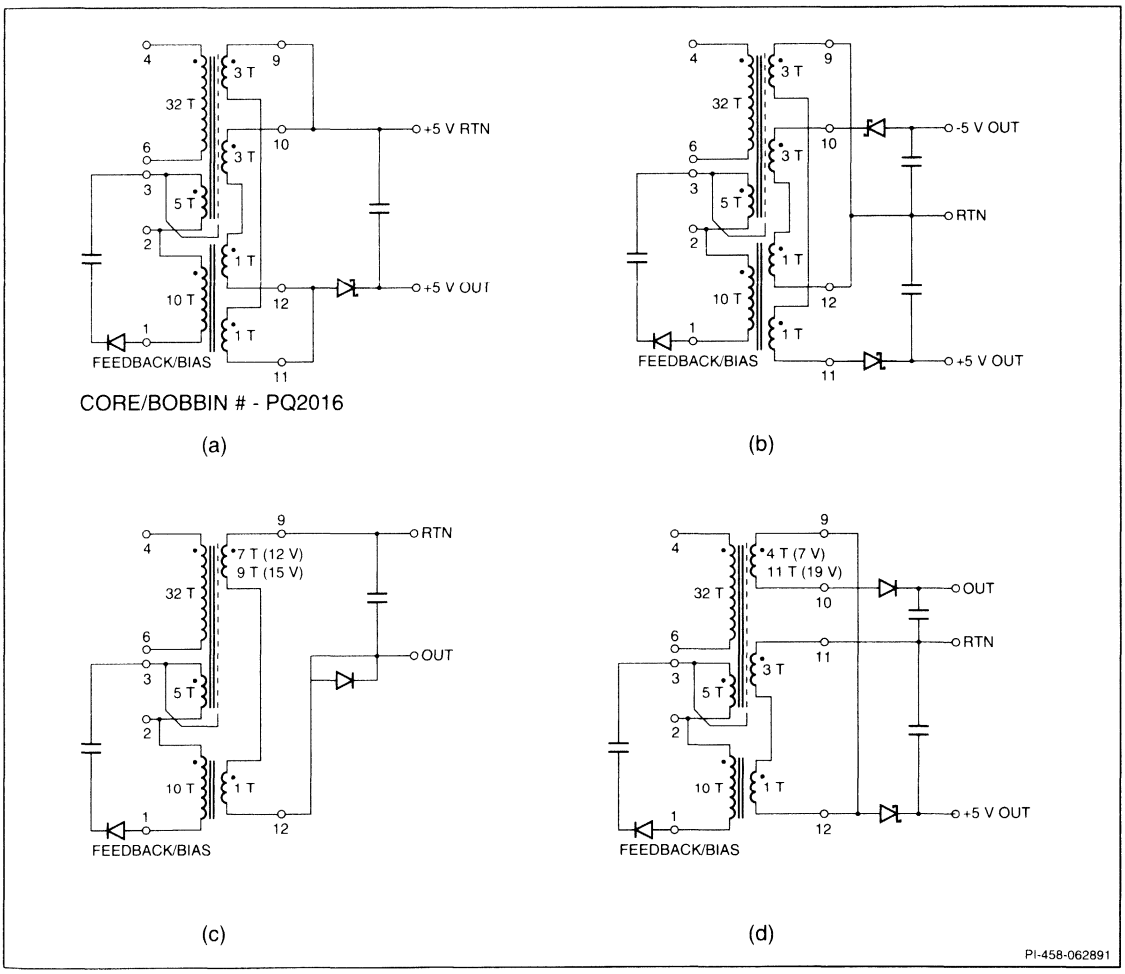
(a) Original T1002 showing the parallel 5 V windings

(b) Separated windings configured for ± 5 V output with coupled inductor.

(c) Single 12 V winding (replace dual 3 turn windings with single 7 turn winding using existing coupled inductor) or single 15 V winding (replace dual 3 turn windings with single 9 turn winding using existing coupled inductor).

(d) 3 turn 5 V winding with coupled inductor. Stack 4 turn winding without coupled inductor on top of 5 V winding as shown to create 12 V output, or stack 11 turn winding without coupled inductor on top of 5 V winding as shown to create 24 V output.

(e) 3 turn 5 V winding without coupled inductor. Stack 4 turn 7 volt winding on top of 5 V winding as shown to create 12 V output. Add additional 7 turn winding for 12 V output. This circuit is for use with a secondary side reference with optocoupler feedback.



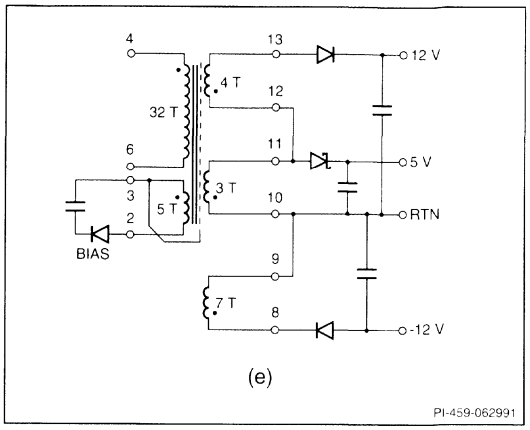
Agency-Approved Wire Vendors

For 120 VAC Applications (UL1430 Wire)

- Weico Wire & Cable
  161 Rodeo Drive
  Edgewood, NY 11717
  (516) 254-2970

For 240 VAC Applications (Triple Insulated Wire)

- Rubudue Wire Company, Inc.
  11080 Rose Avenue
  Fontana, CA 92335
  (714) 357-0151



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PI-459-062991

Feedback Methods for the PWR-SMP Family

APPLICATION NOTE AN-8

Flyback power supplies and DC/DC converters require some type of feedback control system to accurately regulate the output voltage. FeedBack is used to control the output voltage by adjusting the duty cycle of the power MOSFET switch. Performance requirements must be balanced with economic constraints since the most accurate feedback control systems tend to be the most expensive. Two feedback systems and their inherent advantages and disadvantages will be presented here.

The first approach uses a low cost, patented[1] technique with minimal component count to accurately "sense" the output voltage of the power supply using a feedback winding on the power transformer. Typical feedback winding voltage waveforms have leading edge voltage spikes (or pulses) which seriously degrade regulation and accuracy. This technique uses a novel "coupled inductor" as a pulse transformer to eliminate the leading edge pulse. A new pulse is created and scaled equal to and opposite in phase with the leading edge pulse. Cancellation of the two pulses results in a clean waveform with no leading edge spikes or pulses, improving regulation from the feedback winding.

The second feedback system offers the traditional approach of a secondary side reference with an optocoupler to attain the greatest accuracy.

Choosing a FeedBack System

Use the feedback winding approach for applications under the following conditions:

- Small Size or Minimal Parts Count Applications
- Main Output Voltage Accuracy: ±5%
- Output Load Range: 20% to 100% Rating (5 to 1 Range)
- Systems such as battery back-up requiring minimal current consumption when the power supply is off

Use secondary side reference with an optocoupler for applications under the following conditions:

- Main Output Voltage Accuracy: Better than ±5%
- Wide Output Load Range: 0% to 100% Rating (No Load to Full Load)

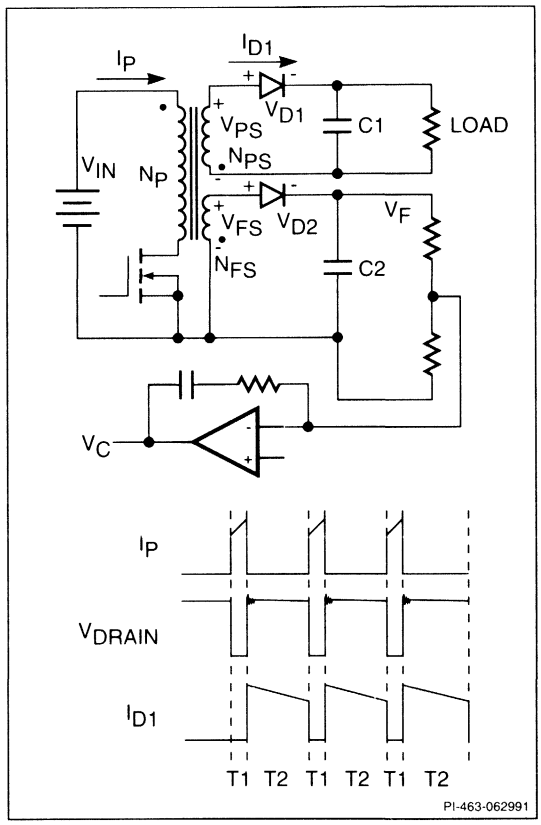

Figure 1. Flyback Power Supply Waveforms.

Transformer FeedBack Winding

This technique uses the minimal number of parts and delivers accuracy sufficient for many applications. The output voltage is measured indirectly through the use of a feedback winding on the power transformer. Power transformer leakage inductance and stray circuit inductance will be shown to have the most significant effect on the accuracy and regulation of the output voltage.

Basic flyback power supply operation is shown in Figure 1. The MOSFET switch turns on for time T1 to store energy in the transformer core. Current builds linearly in the transformer primary while diodes D1 and D2 block current flow in the power and feedback windings respectively. At some point the MOSFET switch turns off which causes voltage reversals on each transformer winding. Diodes D1 and D2 begin to conduct current during interval T2 which delivers energy from the transformer core to the load. Output voltage V_O does not change significantly due to the presence of filter capacitor C1. The voltage on the transformer secondary during T2 is equal to the sum of the output voltage V_O and the voltage drop (eq 1). Transformer action reflects a voltage V_{FS} to the feedback secondary from the power secondary winding by the turns ratio of the two windings (eq 2). The voltage V_{FS} on the feedback secondary winding is rectified (causing a diode voltage drop V_{D2}) and filtered to generate a feedback voltage V_F (eq 3). Combining equations 1-3 and rearranging leads to a relationship for feedback voltage V_F in terms of the output voltage V_O, transformer turns ratio, and the diode drops (eq 4).

$$V_{PS} = V_O + V_{D1} \quad (1)$$

$$V_{FS} = V_{PS} \times \frac{N_{FS}}{N_{PS}} \quad (2)$$

$$V_F = V_{FS} - V_{D2} \quad (3)$$

$$V_F = \left(V_O \times \left(\frac{N_{FS}}{N_{PS}} \right) \right) + \left(\left(\left(\frac{N_{FS}}{N_{PS}} \right) \times V_{D1} \right) - V_{D2} \right) \quad (4)$$

FeedBack voltage V_F consists of two terms as shown in equation 4. The first term is proportional to the output voltage by the ratios of the two windings. The second term represents error created by the forward voltage drops of the two rectifiers. The two voltage drops V_{D1} and V_{D2} usually do not completely cancel. The error term causes slight differences in tracking between the output voltage V_O and the feedback voltage V_F. Since the voltages on the rectifiers changes with load current the error term will be somewhat load dependent. Nonetheless, the output voltage V_O can be controlled between specified limits by directly regulating the feedback voltage V_F. The feedback voltage is connected to an error amplifier and compared with a reference to generate the duty cycle control voltage V_C. The DC value of the regulated feedback voltage is typically 8.5 volts. The power supply output voltage will track the accurately regulated feedback voltage.

Circuit parasitic series inductances and resistances will degrade the tracking and accuracy between the feedback voltage V_F and output voltage V_O. Actual behavior for transformer secondary windings and filters can be modeled by the circuit shown in Figure 2. Note that parasitic resistive and inductive elements occur in the rectifier and filter capacitor as well as the transformer winding. The effects of parasitic resistance are usually minimized

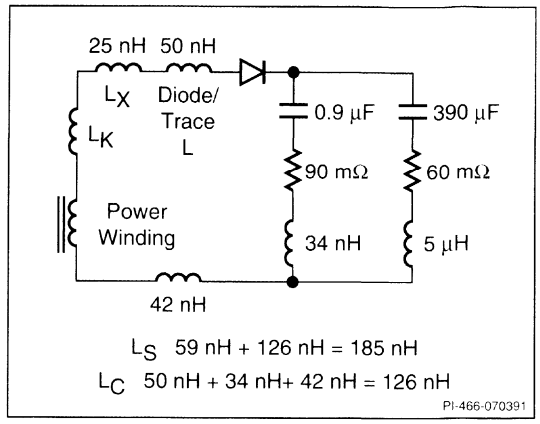

Figure 2. Parasitic Elements of the Power Secondary Circuit.

through the use of low impedance capacitors and properly rated power rectifier diodes. The circuit inductance terms can be collected and combined with transformer leakage inductance L_K into a single inductance L_S as shown in Figure 3.

Current flow through the power secondary will generate an additional voltage drop V_S across the inductors L_S proportional to the rate of change (*di/dt*) of the inductor current (eq 5).

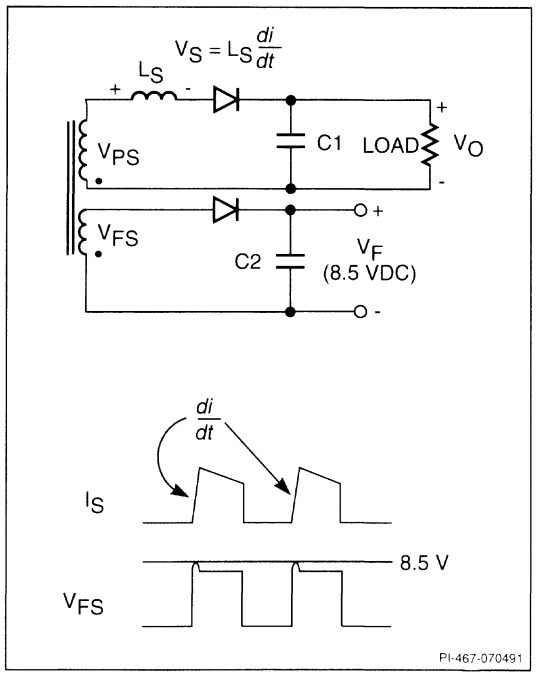

Figure 3. Effects of Parasitic Inductance on V_F.

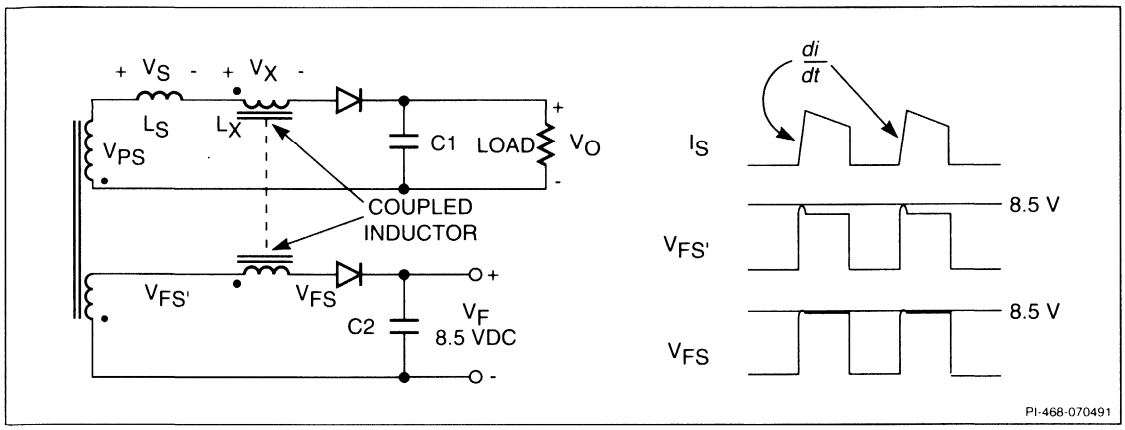

Figure 4. Cancelling the Effects of Parasitic Inductance on V_F.

$$V_S = L_S \times \frac{di}{dt} \qquad (5)$$

The trapezoidal current waveform has a leading edge with a steep slope (high *di/dt*) which creates a significant voltage V_S. This voltage is present during the entire leading edge of the current waveform and varies directly with load current. V_S reflects through the transformer to the feedback winding and appears as a leading-edge voltage spike superimposed on the existing waveform with a new peak value $V_{FS'}$ (eq 6).

$$V_{FS'} = (V_{PS} + V_S) \times \left(\frac{N_{FS}}{N_{PS}}\right) \qquad (6)$$

FeedBack voltage V_F will have a significant error because filter capacitor C2 charges to the new feedback winding peak voltage $V_{FS'}$ rather than the plateau level (V_{FS}) proportional to the output voltage. The error amplifier regulates V_F to the same DC level (8.5 volts typical) which pushes the plateau voltage V_{FS} and output voltage V_O lower than expected. The observed drop in V_O gets worse with increased load current because the effect is load dependent.

Regulation can be improved with the circuit shown in Figure 4. This technique uses a coupled inductor to effectively improve load regulation by canceling out the effects of series inductance L_S. Transformers designed with this technique behave more like the ideal circuit shown in Figure 1. An additional inductance L_X, significantly less than the effective value of inductor L_S, is inserted in series with the power winding.

Power winding current induces a small voltage across the new inductance. A second "coupling" winding on the inductor amplifies the voltage to match the leading edge spike on the feedback transformer winding. Proper connection of the "coupled inductor" secondary and transformer winding will cancel the leading edge spike. Filter capacitor C2 will now charge to the plateau voltage V_{FS} instead of the leakage induced peak voltage $V_{FS'}$.

Coupled inductor construction typically uses requires a small toroidal core with a single turn "primary" and a "secondary" between 5 and 25 turns depending on the output voltage, load current, core material, and effective series inductance. The most economical approach combines the coupled inductor with the power transformer in a single assembly as shown in Figure 5. This allows the manufacturer to match the parameters of the coupled inductor with the effective series inductance expected in the application. The coupled inductor "primary" is insulated to meet the primary to secondary safety requirement of the application.

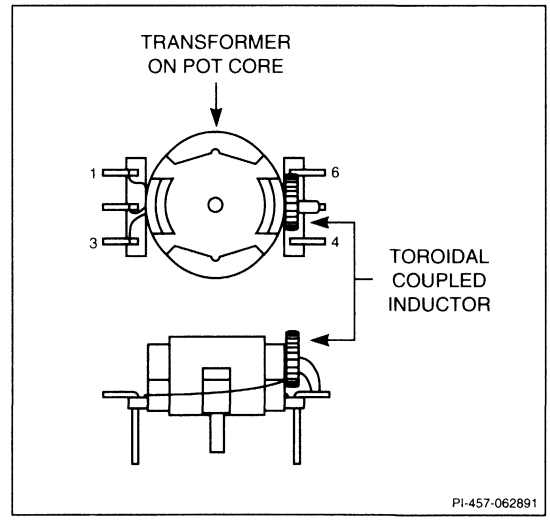

Figure 5. Transformer with Integrated Coupled Inductor L_X.

Small toroidal cores of Nickel-Zinc ferrite (such as Philips/ Ferroxcube 1041T060-4C4, 25 nH/T^2) are suitable for applications with DC load currents below 2 amps. Low permeability powdered iron (such as MicroMetals T30-8, 14 nH/T^2) are best for applications with DC load currents above 2 amps. Other core materials with sufficient bias current capability can be used as long as saturation at peak current levels is avoided.

Determining the Turns Ratio

Gain-phase Analyzer Method

The key to selecting the correct number of coupled inductor secondary turns is to accurately determine the magnitude of series inductance L_S. To simplify analysis series inductance L_S is further reduced to the series combination of the power secondary leakage inductance L_K and circuit series inductance L_C.

Power winding leakage inductance L_K can be found with the technique shown in Figure 6. The transformer primary winding is driven from an AC current source. Shorting the power winding effectively places the impedance of the leakage inductance L_K directly across the output of the transformer. The leakage inductance now acts like a load impedance. The voltage across this load impedance will reflect by the turns ratio over to the feedback winding. Impedance Z_K can now be calculated by measuring the open circuit feedback winding voltage, adjusting for the turns ratio, and dividing by the power winding current I_P (eq 7). Inductance L_K is then calculated from Z_K and the frequency of excitation f (eq 8).

$$Z_K = V_F \times \frac{\left(\frac{N_F}{N_P}\right)}{I_P} \quad (7)$$

$$L_K = Z_K \times 2\pi f \quad (8)$$

Circuit series inductance L_C can be found by summing the inductance of the PC layout, output diode, and filter capacitor. Total series inductance L_S is the sum of circuit inductance L_C and leakage inductance L_K. The feedback coupled inductor is inserted in series with transformer windings as shown in Figure 4. Note that the coupled inductor primary inserts additional inductance L_X in series with L_S. Primary current induces a voltage V_S across L_S and a smaller voltage V_X across L_X. V_S and V_X are related by the ratio of inductors L_S and L_X (eq 9). The sum of voltage V_X and V_S are reflected by the power transformer turns ratio to the feedback winding as a leading edge spike V_{SPIKE} with a magnitude given by equation 10. The secondary winding on L_X sets up a voltage V_Y related to V_X by the ratio K of coupled inductor windings (eq 11). Cancellation occurs when the spike voltage is equal to coupled inductor voltage.

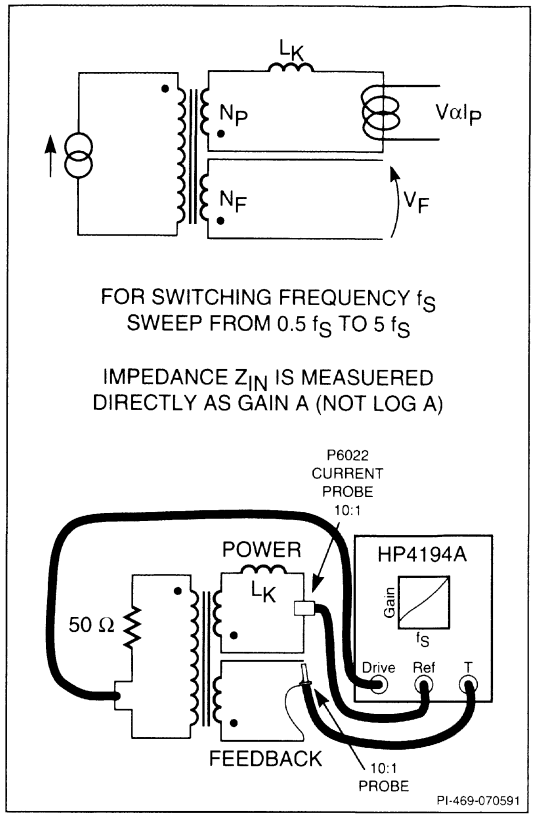

Figure 6. Gain-phase Analyzer Test Setup.

Setting the spike voltage V_{SPIKE} equal to V_Y and rearranging terms yields the solution for turns ratio K (eq 12).

$$V_S = V_X \times \frac{L_S}{L_X} \quad (9)$$

$$V_{SPIKE} = (V_S + V_X) \times \frac{N_F}{N_S} = V_X \times \left(\frac{L_S}{L_X} + 1\right) \times \frac{N_F}{N_S} \quad (10)$$

$$V_Y = V_X \times K \quad (11)$$

$$K = \left(\frac{L_S}{L_X} + 1\right) \times \frac{N_F}{N_S} \quad (12)$$

Example: For a measured total series inductance L_S of 185 nH, a coupled inductor single turn inductance L_X of 25 nH, transformer power winding with 3 turns, and feedback winding of 5 turns, the number of turns for the coupled inductor secondary should be 14 turns.

Empirical Method

An experimental method can also be used to determine the optimum turns ratio for the coupled inductor. A power supply is built using the desired transformer, rectifier, output capacitor, and PC board. BreadBoards can be used but will have different series inductance characteristics leading to different coupled inductor turns ratios. The coupled inductor is wound with an excessive number of secondary turns (typically 25 for a single-turn coupled inductor primary). The power supply is operated from a fixed input voltage into a fixed maximum load. The DC output voltage is measured and recorded. The power supply is then turned off and one turn removed from the secondary winding of the coupled inductor. Keep lead wires short to minimize inductance. The power supply is again turned on and the DC output voltage recorded. The output voltage should have increased slightly (if not rewind the coupled inductor with more turns and start again). Repeat the operation until the output voltage begins to decrease. The curve shown in Figure 7 is typical for the variance in the DC output voltage as a function of the turns ratio of the coupled inductor. Find the peak of the curve, determine the desired ratio, and select the next highest integer value.

The feedback diode D2 anode voltage waveform can be examined with an oscilloscope to verify operation. The voltage should rise to the plateau level with little or no leading edge spike voltages. Too few turns on the coupled inductor will allow some fraction of the leading edge spike to appear at the diode anode. Too many turns will cause an undershoot at the leading edge. Both conditions lead to lower output voltage and poor regulation.

Variations of this technique for lower current, higher voltage applications requiring higher values of L_X include using more than one core in parallel with a single turn primary or multiple primary turns on a single core.

A typical multiple output application with symmetric positive and negative output voltages is shown in Figure 8. A typical multiple output application with stacked positive outputs is shown in Figure 9.

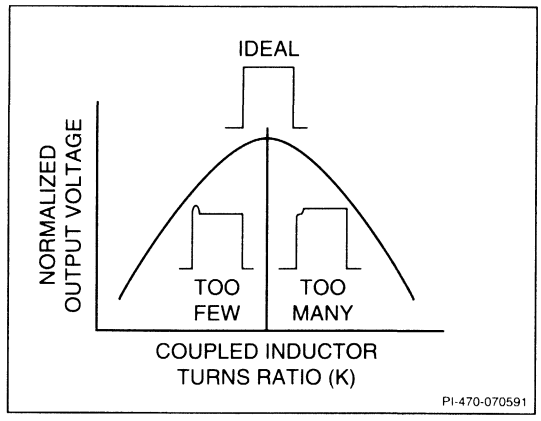

Figure 7. Effect of K on the Feedback Waveform.

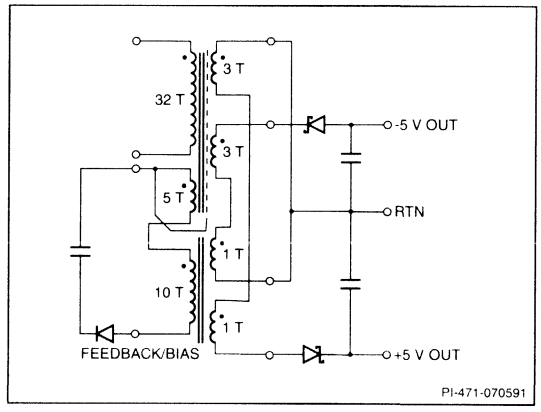

Figure 8. Dual 5 V Output Transformer with Coupled Inductor.

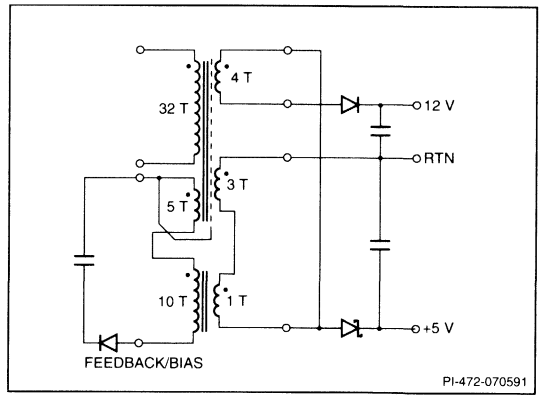

Figure 9. 5/12 V Output Transformer with Coupled Inductor.

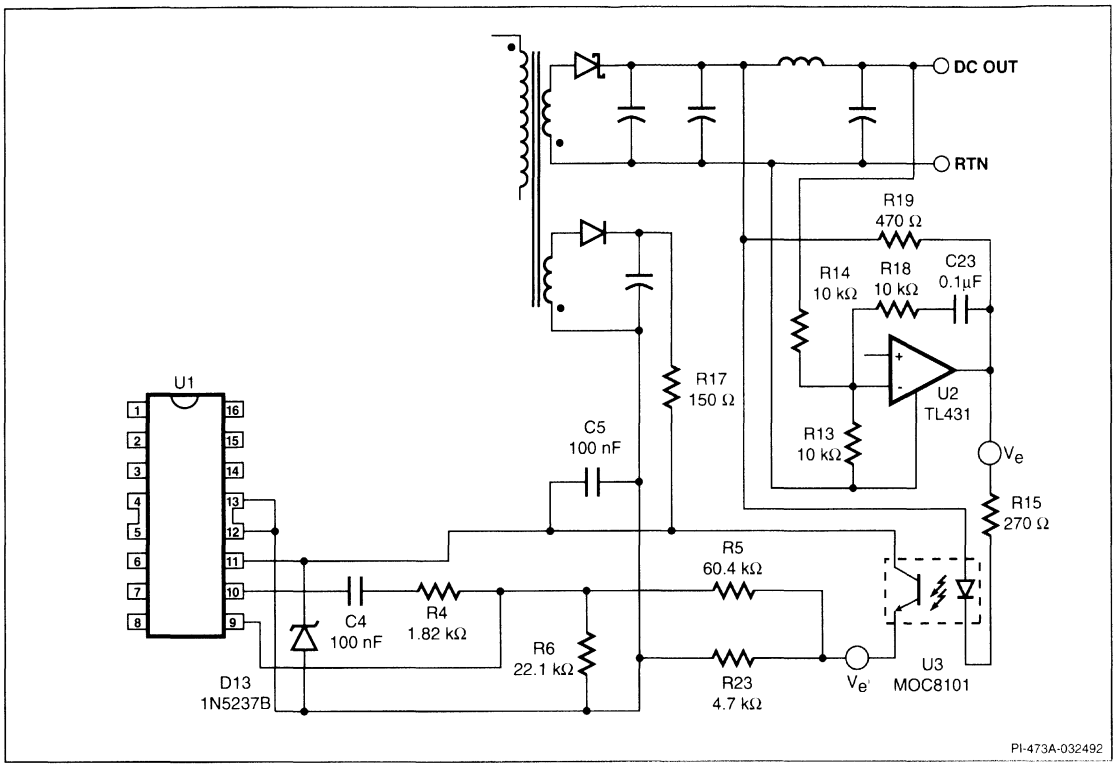

Figure 10. Feedback Circuit Using Optical Isolation with Optional LC Post Filter.

Optocoupler FeedBack

This feedback technique is inherently more accurate because the output voltage is measured directly. The accuracy of the output voltage is basically determined by the accuracy of the TL431 reference voltage (± 1%) and resistors R13 and R14.

The circuit shown in Figure 10 contains a secondary side reference and an optocoupler to measure the output voltage directly and generate an isolated error signal. The output voltage is sensed and compared to an accurate reference voltage by an error amplifier to create an error signal. The output of the error amplifier drives the error signal through the optocoupler to the power supply IC to produce the proper duty cycle and output voltage.

The reference, error amplifier, and driver function are combined in the TL431 shunt regulator U2. The output voltage is divided down by R13 and R14 and compared with the nominal 2.5 volt reference by the error amplifier U2 to create an error signal voltage. R18, C23, R4, and C4 are used for tailoring the frequency response of the control loop. The error signal voltage is converted to a current by the series combination of R15 and the optocoupler light emitting diode. The Current Transfer Ratio (CTR) of the optocoupler delivers an emitter current proportional to light emitting diode current. This emitter current is converted back to a voltage signal by the effective parallel resistance Re of resistors R23, R5, and R6. The operational amplifier inside the power supply IC U1 together with R4, C4, and R5 create an inverting amplifier useful for tailoring the frequency response of the control loop. Refer to the appendix for a complete frequency response analysis.

For output voltages greater than 5 volts up to 36 volts change R13, R15, and R18 as shown (eq 13, 14, 15)

$$R13 = \frac{2.5V}{(V_O - 2.5V)} \times R14 \qquad (13)$$

$$R15 = \frac{(V_O - 4.5V)}{2mA} \qquad (14)$$

$$R19 = \frac{(V_O - 4V)}{2mA} \qquad (15)$$

Resistor R19 provides necessary bias current for U2 (minimum of 2 mA).

The bias circuit for power supply IC U1 consists of zener diode D13, capacitor C5, and resistor R17. This circuit maintains a bias voltage between 8.25 and 9.0 volts and provides typically 4 mA of bias current to the power supply IC. Adjustments to the value of R17 or different zener diodes may be necessary depending on the construction of the transformer T1.

Secondary-referenced LC Post Filters

Applications with LC post-filters require special attention to avoid introducing additional phase shift into the feedback loop. Figure 10 shows how the optocoupler diode and resistor R19 are connected to the input side of the post-filter while the resistor divider formed by R13 and R14 are connected to the output side. This has the effect of sensing the DC voltage at the connector for highest DC accuracy while sensing the AC signal components before post-filtering. Refer to the appendix for determining the frequency response of this circuit.

APPENDIX

SPICE Modelling for Voltage-mode Flyback Power Supplies Operating in Continuous Mode

Power supplies will oscillate if the feedback control loop is not properly compensated. Compensating the feedback control loop requires knowledge of the frequency response (gains, phase shifts, and pole/zero locations) of the various function blocks making up the power supply. Thankfully, computer modeling tools can now be used to properly simulate the frequency response of the power supply and select appropriate compensation.

Analyzing the frequency response of a switching power supply requires replacing the actual discrete, nonlinear circuit implementation with a linear, small signal model that behaves in the same manner over the frequency range of interest. Several different models are available to choose from, and have varying degrees of accuracy. A slightlly modified version of the well known "canonical circuit model" developed by Middlebrook and Cuk[1] will be used to model flyback power supplies. This model is accurate at frequencies approaching half the switching frequency.

Note that this appendix covers only continuous mode of operation for Power Integrations' voltage-mode power supply circuits used in flyback power supplies. For a treatment of discontinuous mode of operation, refer to AN-6. For Power Integrations' current-mode power supply circuits, refer to AN-11.

The PWR-EVAL5 demonstration power supply is based on the PWR-SMP210, and is used as an example throughout this appendix.

Computer Modelling

Various ways exist to implement the models for computer simulation. Different simulators may limit the types of components available for modeling. The computer models and hints shown here have been successfully used with both PSPICE[3] and the SPICE based Analog Workbench[4].

Computer Model Schematic Diagram

The schematic and accompanying input file is shown in Figures 12 and 13 for an actual SPICE model successfully used in simulating the frequency response of the PWR-EVAL5. Each section will be briefly described and the means for calculating or selecting each parameter will be defined.

Components with one or two digit numeric designators correspond to actual component values on the PWR-EVAL5 (C10, C2, etc). Components with alphabetic designators correspond to behavorial model components (Le, EE, Fd, etc.). Components with three digit numeric designators are used to implement functions (R112, R113, etc.) or for adding high impedance to a "floating" node to satisfy SPICE DC operating point calculations (R115, R119, etc.).

AC Input

The AC input power source is modeled by source V_g. During control loop analysis this source is effectively shorted to ground by assigning an AC value of 0 volts. Simulation of input impedance or line rejection are performed by assigning a value to this source, sweeping over the frequency range of interest, and plotting the results.

EMI Filter

The EMI filter components are included in the model because of the effects of the current generator, which will be discussed later. In most applications, the output impedance of the EMI filter has little effect on the control loop and is included for completeness of the model.

Power Path

The power path contains all the stages from the control input voltage to the modulator (node 13) to the output voltage (node 8).

Power Transformer

The Middlebrook/Cuk canonical model was derived for buck-boost converters with a single inductor. Flyback power supplies (isolated versions of the buck/boost power stage) require a transformer to model the step-up or step-down effect of the flyback transformer. The transformer is modeled by voltage controlled voltage source E_t and current controlled current source F_t. Independent voltage source V_t is used as an ammeter by SPICE to measure the control current for F_t. E_t and F_t both have the same gain value K_t equal to the turns ratio of the actual flyback transformer (equation 16) where N_S is the secondary number of turns while N_P is the primary number of turns. For example, the gain value of transformer T1002 with a 32 turn primary and 3 turn secondary is:

$$K_t = \frac{N_S}{N_P} = \frac{3}{32} = 0.0938 \qquad (16)$$

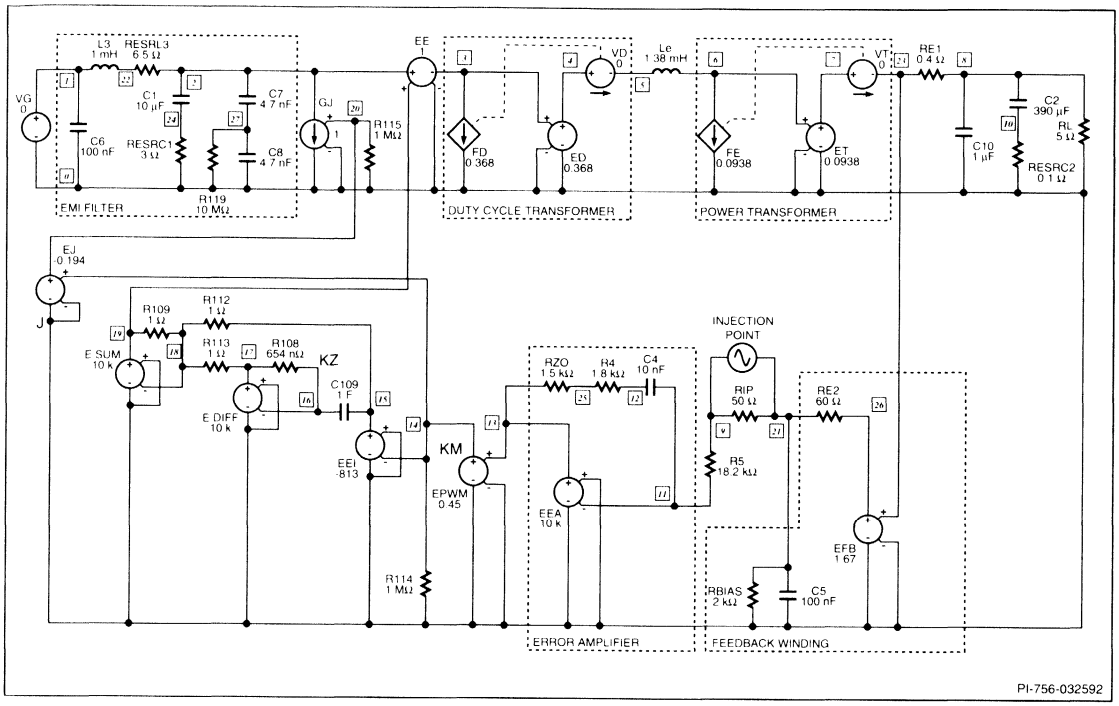

Figure 12. SPICE Model Schematic Diagram of the PWR-EVAL5.

Key Parameters

The following three key parameters will be used repeatedly in the various stages of the power path.

Effective Output Voltage

The effective output voltage V_P is defined as the sum of the actual output voltage V_O and rectifier diode drop V_D reflected to the primary side of the power transformer. For V_O of 5 V and V_D of 0.5 V:

$$V_P = (V_O + V_D) \times \frac{1}{K_t} = (5 + 0.5) \times \frac{1}{0.0938} = 58.8V \quad (17)$$

Effective Load Resistance

The effective load resistance R_P is defined as the actual load resistance R_{LOAD} reflected to the primary side of the power transformer. For R_{LOAD} of 5 Ω:

$$R_P = \frac{R_{LOAD}}{K_t^2} = \frac{5\Omega}{.0088} = 568\Omega \quad (18)$$

Duty Cycle

The average duty cycle D is given by equation 19 where V_P is the reflected DC output voltage and V_G is the DC input voltage. Most of the parameters used for the power path linear model depend on the value of D and will vary as V_G varies. For V_G of 160 V and V_P of 58.8 V:

$$D = \frac{V_P}{(V_G + V_P)} = \frac{58.8}{(160 + 58.8)} = 0.269 \quad (19)$$

Effective Inductor

L_e represents the effective inductance of the buck-boost inductor which includes the effects of the duty cycle. L_e, together with the output capacitors, form the low pass filter for the pulse width modulator. The value for L_e is defined by the actual measured primary inductance L_P of the flyback transformer and D. For T1002 L_P of 738 µH and D of 0.269:

$$L_e = \frac{L_P}{(1-D)^2} = \frac{738\mu H}{(1-0.269)^2} = 1.38mH \quad (20)$$

```
* PSPICE STATEMENTS
.PROBE

*SPICE STATEMENTS
.OP
.AC DEC 25 10 100K

* LOAD
RL 8 0 5

* EFFECTIVE INDUCTOR
Le 5 6 1380UH

* EMI FILTER
C6 1 0 100NF
R119 0 27 10MEG
C1 2 24 10UF
L3 1 22 1M
RESRC1 24 0 3
C7 2 27 4700PF
C8 27 0 4700PF
RESRL3 22 2 6.5

* DUTY CYCLE XFMR
FD 3 0 VD 0.368
VD 4 5 0
ED 4 0 3 0 0.368

* POWER XFMR
FT 6 0 VT 0.0938
VT 7 23 0
ET 7 0 6 0 0.0938

* OUTPUT FILTER
RE1 8 23 0.4
RESRC2 10 0 100M
C10 8 0 1U
C2 8 10 390U

* FEEDBACK WINDING
EFB 26 0 23 0 1.67
RBIAS 21 0 2K
RE2 21 26 60

* INJECTION POINT
VIP 21 9 AC 1
RIP 21 9 50

* ERROR AMPLIFIER
C4 12 11 0.01UF
C5 21 0 0.1UF
EEA 13 0 0 11 10K
R5 9 11 18.2K
RZO 13 25 1800
R4 25 12 1800

* PULSE WIDTH MODULATOR
EPWM 14 0 13 0 0.45

* E GENERATOR WITH RHP ZERO
EEI 15 0 0 14 -813
EE 2 3 19 0 1
C109 16 15 1
R109 19 18 1
R112 18 15 1
R113 18 17 1
EDIFF 17 0 0 16 10K
ESUM 19 0 0 18 10K
R114 14 0 1MEG
R108 17 16 654E-9

* J GENERATOR
EJ 20 0 14 0 -0.194
GJ 2 0 20 0 1
R115 20 0 1MEG

* INPUT
VG 1 0 0

.END
```

Figure 13. Net List of the PWR-EVAL5 SPICE Model.

Modulator Gain

The modulator compares a control voltage with a sawtooth voltage waveform to create a duty cycle waveform which drives the power MOSFET switch in the flyback power stage. The linear model for the modulator is the voltage-controlled voltage source E_{PWM} with small signal AC gain K_m defined as the ratio of the maximum duty cycle D_{max} to the peak to peak voltage of the sawtooth waveform. For the PWR-SMP power supply circuits previously identified, D_{max} is typically 0.45 and V_{PP} is typically 1 volt. Therefore:

$$K_m = \frac{D_{max}}{V_{PP}} = \frac{0.45}{1} = 0.45 \qquad (21)$$

Dependent Voltage Generator with RHP Zero

Dependent voltage generator EE directly modulates the converter. There is a gain term K_e represented by voltage-controlled voltage source EEI. The gain K_e is defined as the negative of the reflected output voltage V_p divided by the square of the duty cycle D. For V_p of 58.8 V and D of 0.269:

$$K_e = \frac{-V_P}{D^2} = \frac{-58.8}{0.0724} = -813 \quad (22)$$

The right half plane zero model uses an inverting differentiator stage (Ediff, C109, R108) followed by an inverting summing stage (Esum, R109, R112, R113). The gain K_z of the differentiator stage is actually the value assigned to resistor R108 when C109 has a value of unity:

$$K_z = \frac{D \times L_e}{R_P} \quad (23)$$

The frequency response of a RHP zero has a flat 0 dB gain at low frequency with a positive gain break above the corner frequency at a rate of 20 dB/decade and a phase shift that lags up to 90 degrees as shown in Figure 14. The corner frequency occurs at:

$$F_{ZERO_{RHP}} = \frac{1}{2\pi \times K_z} \quad (24)$$

For D of 0.269, effective inductance L_e of 1.38 mH, and R_p of 568 Ω:

$$K_z = \frac{0.269 \times 1.38\text{mH}}{568} = 6.54 \times 10^{-7} \quad (25)$$

$$F_{ZERO_{RHP}} = \frac{1}{2\pi \times 6.54 \times 10^{-7}} = 243\text{kHz} \quad (26)$$

Note that the dependence of K_z on D causes the right half plane zero to migrate with changing V_G. In normal applications, the limit on D (40% to 50%) will keep the right half plane zero at a high enough frequency to minimize the effect on the control loop.

Dependent Current Generator

Switching power supplies have a constant input power characteristic which exhibits a negative input impedance under DC conditions and over some low frequency range. Negative input impedance means that if the input voltage should rise, the measured input current will fall because of the effects of the converter. Dependent current generator GJ models the negative input impedance and is controlled by the modulator. This current generator indirectly modulates the converter due to the effects of finite source impedance.

RHP GAIN/PHASE vs. FREQUENCY

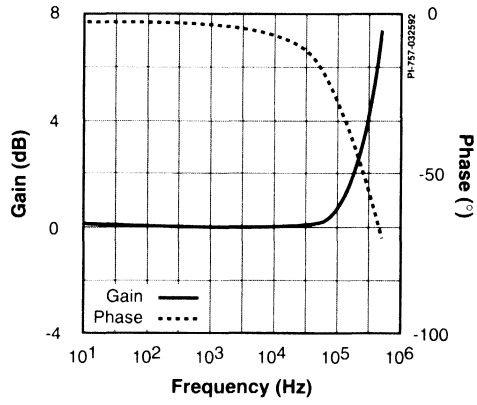

Figure 14.

The gain K_j from the modulator to generator GJ is calculated using V_p, R_p, and D. For V_p of 58.8 V, D of 0.269, and R_p of 568 Ω:

$$K_j = \frac{-V_P}{(1-D)^2 \times R_P} = \frac{-58.8}{(1-0.269)^2 \times 568} = -0.194 \quad (27)$$

DC-DC Conversion Trnasformer

The duty cycle transformer models the effective DC-to DC transformation of duty cycle D. The transformer is modeled by voltage-controlled voltage source E_d and current-controlled current source F_d. Independent voltage source V_d is used as an ammeter by SPICE to measure the control current for F_d. E_d and F_d both have the same gain value K_d equal to the ratio of the effective output voltage V_p to the input voltage V_g as shown in equation 28. For Vp of 58.8 V and Vg of 160 V:

$$K_d = \frac{V_P}{Vg} = \frac{58.8V}{160V} = 0.368 \quad (28)$$

Output Filter

The output filter model consists of the actual filter components used in the switching power supply combined with an effective output resistance R_{EI}. R_{EI} lumps various series circuit resistance terms with other "lossless" resistance terms that arise from switch modulation. Note that capacitor C2 has an equivalent series resistance (ESR) term which must be included in the model.

Estimating the Value of R_{E1}

An initial value for effective output impedance R_{E1} can be estimated from the load regulation curve of the power supply when feedback winding control is used. This parameter is intended to be refined when simulation data is compared with measured data. The effect of R_{E1} on the power path frequency response will be used to deduce the true effective value. Output impedance R_{E1} is initially assigned the value of the DC output impedance defined as the ratio of the change in voltage to the change in current. Referring to the documentation of the PWR-EVAL5, the output voltage varies approximately 5% or 250 mV for a load change 1.2 A load change (from 0.4 to 1.6 A):

$$R_{E1} = \frac{\Delta V}{\Delta I} = \frac{250\ mV}{1.2\ A} = 208\ m\Omega \qquad (29)$$

Measured data will later show that 400 mΩ is a more appropriate value. 400 mΩ will be used for the remainder of this discussion.

Power Path Gain Response

The power path frequency response consists of a low frequency DC gain term and a low pass filter rolloff characteristic depending on L_e, R_{E1}, and the output filter capacitors. The low frequency gain A_p is defined as the product of the gains of the individual stages making up the power path:

$$A = K_m \times K_e \times K_d \times K_t \times \frac{R_{LOAD}}{(R_{E1} + R_{LOAD})} \qquad (30)$$

$$= 0.45 \times 813 \times 0.368 \times 0.0938 \times \frac{5}{(0.400 + 5)} = 11.7 \text{ or } 21.4\ dB$$

The low pass filter characteristic depends on the effective value of R_{E1}. The circuit values define corner frequencies that cause the gain response to either decrease (poles) or increase (zeros). For power paths with relatively high values of R_{E1} (such as the PWR-EVAL5), the gain response will begin to roll off at a pole frequency F_{p1} determined by output capacitor C2 and the parallel combination of R_{E1} and R_{LOAD} at the rate of 20 dB/decade. Inductor L_e and R_{E1} will contribute a second pole frequency F_{p2} that would cause the gain to decrease at 40 dB/decade were it not balanced by a zero frequency F_{z1} depending on capacitor C2 and ESR. Gain response can be quickly approximated with straight lines on a gain plot to verify the model as shown in Figure 15.

$$F_{p1} = \frac{1}{\frac{2\pi \times R_{E1} \times R_{LOAD} \times C2}{(R_{E1} + R_{LOAD})}} \qquad (31)$$

$$= \frac{1}{\frac{2\pi \times 0.4 \times 5 \times C2}{(0.4 + 5)}} = 1.10\ kHz$$

POWER PATH GAIN vs. FREQUENCY

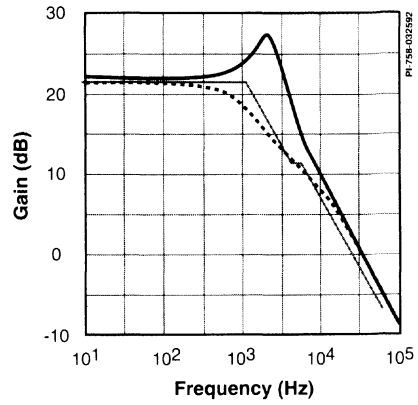

Figure 15.

$$F_{p2} = \frac{R_{E1}}{2\pi \times L_e \times K_t^2} = \frac{0.4}{2\pi \times 1.38mH \times .0088} = 5.24kHz \qquad (32)$$

$$F_{z1} = \frac{1}{2\pi \times ESR \times C2} = \frac{1}{2\pi \times 0.1 \times 390\mu F} = 4.08kHz \qquad (33)$$

Power paths with relatively low values of R_{E1} will have a gain response dominated by a complex pole pair at the resonant frequency f_R determined by L_e and C2. R_{E1} determines the amount of peaking in the gain at f_R. The gain response falls at a 40 dB/decade rate until the zero frequency F_{z1} created by capacitor C2 and ESR defined above. This gain response is also shown in Figure 15. The computer simulated gain response is calculated from the ratio of the voltage at node 8 to the voltage at node 13. For an assumed R_{E1} of 10 mΩ:

$$f_R = \frac{1}{2\pi \times K_T \times \sqrt{C2 \times L_e}} \qquad (34)$$

$$= \frac{1}{2\pi \times 0.0938 \times \sqrt{390\mu F \times 1.38mH}} = 2.31kHz$$

$$\text{Peaking} = \frac{K_T \times \sqrt{\frac{L_e}{C2}}}{(R_{E1} + ESR)} \qquad (35)$$

$$= \frac{0.0938 \times \sqrt{\frac{1.38mH}{390\mu F}}}{(0.1 + 0.01)} = 1.6 \text{ or } 4.08\ dB$$

The K_T term in each equation effectively reflects L_e to the secondary side of the power transformer. The pole contributed by C10, the right half plane zero, and the effects of the EMI filter have been ignored.

Error Amplifiers

Accurate DC output voltages require an error amplifier which senses the output voltage either directly or indirectly, and generates an error voltage. This error voltage drives the modulator input to increase or decrease the duty cycle as necessary to minimize the error term of the output voltage.

The error amplifier within the power supply IC is modeled as an inverting amplifier as shown in Figure 16. This amplifier has a low frequency gain response that decreases at a rate of 20 dB/decade. At high frequency, the gain A_e is flat and determined by resistors R4, R5, and the output impedance of the internal amplifier R_{ZO}:

$$A_e = \frac{(R4 + R_{ZO})}{R5} = \frac{(1.8k\Omega + 1.5k\Omega)}{18.2k\Omega} = 0.181 \text{ or } -14.9dB$$

The zero frequency f_{ez} above which the gain flattens is determined by C4, R4, and R_{ZO}.

$$f_{ez} = \frac{1}{2\pi \times C4 \times (R4 + R_{ZO})} \quad (36)$$

$$= \frac{1}{2\pi \times 10nF \times (1.8k\Omega + 1.5k\Omega)} = 4.82 \text{ kHz}$$

FeedBack Winding

FeedBack windings on flyback transformers provide a simple means of controlling the output voltage. The linear model is shown in Figure 16. Dependent generator voltage source E_{FB} models the turns ratio of the feedback winding to the power winding. Note that the generator is connected in front of resistance R_{E1} (to node 23). This models the fact that the output voltage is not being sensed directly, and allows the output voltage to vary slightly with R_{LOAD} (characteristic of feedback winding control). Resistor R_{E2} models the effect of leakage inductance on the feedback winding while resistor R_{BIAS} is simply the ratio of bias voltage to bias current of the power supply IC. Bias bypass capacitor C5 forms a pole with R_{E2}.

The effective value of R_{E2} is another parameter that is estimated initially and refined when simulation data is compared with measured data. The effect of R_{E1} on the loop gain and phase response will be used to deduce the true effective value. The initial value should be chosen to provide a divider effect proportional to R_{E1} and R_{LOAD}. For a bias current of 4 mA and a feedback voltage of 8.5 V, R_{BIAS} is approximately 2 kΩ. Solving for R_{E2}:

$$R_{E2} = \frac{R_{E1}}{R_{LOAD}} \times R_{BIAS} = \frac{0.4}{5} \times 2 \text{ k}\Omega = 160 \ \Omega \quad (37)$$

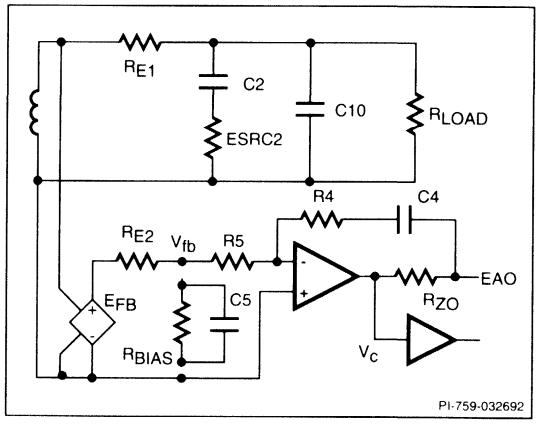

Figure 16.

Measured data will later show that 60 Ω is a more appropriate value. 60 Ω will be used for the remainder of this discussion.

The feedback winding connection has a low frequency gain term K_{fb} defined by the flyback transformer power winding turns N_S, feedback winding turns N_F, and the divider effect of R_{E1}:

$$K_{fb} = \frac{N_F}{N_S} \times \frac{R_{BIAS}}{(R_{BIAS} + R_{E2})} \quad (38)$$

The feedback winding connection has a single pole frequency f_{FP} determined by capacitor C5 and the parallel combination of R_{E2} and R_{BIAS}. The gain will decrease beyond f_{FP} at a rate of 20 dB/decade

Example: for the T1002 transformer and given parameters:

$$K_{fb} = \frac{5}{3} \times \frac{2k\Omega}{(2k\Omega + 60\Omega)} = 1.62 \text{ or } 4.18dB$$

$$f_{FP} = \frac{(R_{E2} + R_{BIAS})}{2\pi \times R_{E2} \times R_{BIAS} \times C5} \quad (39)$$

$$= \frac{(60\Omega + 2k\Omega)}{2\pi \times 60\Omega \times 2k\Omega \times 100nF} = 27.3 \text{ kHz}$$

Figures 17 and 18 are overlays of measured and simulated PWR-EVAL5 loop gain and phase response from node 21 to node 9. The loop gain can be generated by plotting the ratio of the voltage at node 21 to the voltage at pin 9 in dB. The loop phase is generated by plotting the difference between the phase of the voltage at pin 21 and the phase of the voltage at pin 9.

Total Loop Gain and Phase Response

The total control loop gain is the product of the power path, feedback winding, and error amplifier frequency responses. Gain terms (in dB) and phase terms both add to produce the overall gain and phase response curves.

Control Loop Stability

Stable control loops require that the total loop gain does not reach 0 dB before the loop phase shifts 180 degrees. Two figures of merit, phase margin and gain margin, define the relative stability of a given control loop.

Phase Margin

Phase margin is defined as the difference between the measured phase shift and 0 degrees when loop gain crosses 0 dB as shown in Figures 17 and 18. Phase margin should be at least 45 degrees with 60 degrees as a goal for most applications.

Gain crossover for the PWR-EVAL5 occurs at approximately 17 kHz. The phase shift at 17 kHz is approximately 60 degrees.

Gain Margin

Gain margin is defined as the difference between the measured gain and 0 dB when the loop phase crosses 0 degrees. Gain margin should be at least 10 dB with 12 dB as a goal for most applications.

The simulated loop phase crosses 0 degrees at approximately 80 kHz (measured phase crossover was found to be higher). Gain margin at 80 kHz is found to be approximately 20 dB.

Stabilizing the System

Stabilizing the feedback loop requires knowledge of the main component impedances, calculation of each model parameter, verification of power path response, verification of feedback path response, and proper selection of compensation components. The individual steps are given below for power supplies such as the PWR-EVAL5 using feedback winding control.

1) Measure impedances of selected components. Verify output capacitor ESR and flyback transformer primary inductance with both analyzers and in-circuit waveforms.

2) Ensure that the feedback winding voltage is a good representation of the output voltage by performing DC load regulation measurement. Use coupled inductor technique and properly optimize the number of turns for best accuracy and regulation when using feedback winding control.

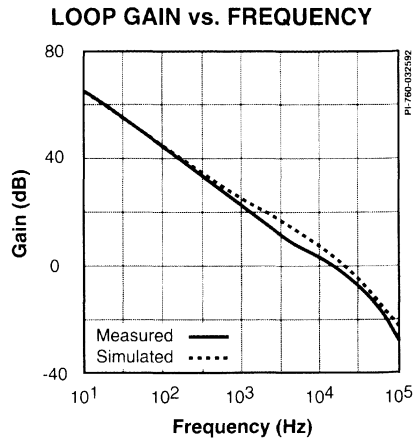

Figure 17.

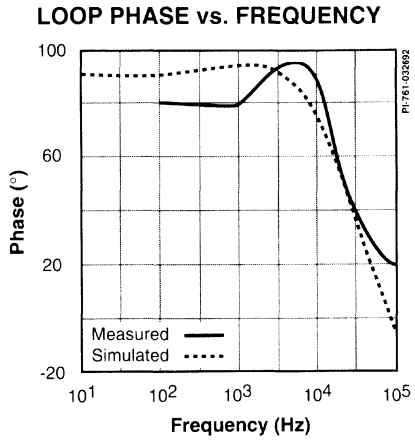

Figure 18.

3) Calculate model parameters based on input voltage, load, and transformer inductance and turns ratios.

4) Measure power path gain and phase response. Compare with simulated results. (Watch out for the effects of the error amplifier output impedance discussed in following section. Temporarily increase C4 if necessary)

5) Adjust value for RE1 and ESR to match the measured frequency response to the simulated response.

Stabilizing the System (cont.)

6) Simulate the total loop gain and measure gain margins and phase margins. Adjust the value of R5 to change the effective gain and C4 to change the effective phase shift to meet gain and phase crossover requirements. Note that values for R4 below the typical output impedance of the error amplifier (1.5 kΩ) will not have much effect on the error amplifier frequency response.

7) Measure the loop gain and phase response and compare with the simulated response.

8) Adjust value for $R_{1,2}$ comparing loop phase shift around the pole frequency of the feedback winding circuit (27.3 kHz in this example).

9) Repeat for various line voltage and load current conditions.

Note that this analysis covers continuous mode of operation. The measured response will diverge from the modeled response if light load conditions result in discontinuous operation. Refer to stability analysis section of application note AN-6.

Measurement Techniques

A test setup for measuring control loop gain and phase with the Hewlett Packard HP4194A Impedance/Gain/Phase Analyzer is shown in Figure 19. Resistor R_{IP} is chosen much smaller than resistor R5 to minimize the effect on the DC output voltage. A coupling transformer with inductance of at least 100 mH, 1:1 turns ratio, and self resonant frequency above 100 kHz is used to apply an AC voltage across R_{IP}. This voltage is then swept over the frequency range of interest while measuring node voltages.

Hints:

Always isolate the power supply from the AC input mains with an isolation transformer for personnel safety. The voltage probes are connected to earth ground and will effectively short the AC mains if the isolation transformer is not used.

Do not load down the output of the signal source. The resultant signal may not be sinusoidal.

Care must be taken not to overdrive the amplifiers into large signal conditions as this will introduce nonlinear effects. Verify linear operation by changing the magnitude of the AC driving source with an attenuator or variable resistor. The measured gain/phase response should not change when driven with an appropriate signal level.

Use long integration times and average multiple passes to reduce the measurement errors caused by noise.

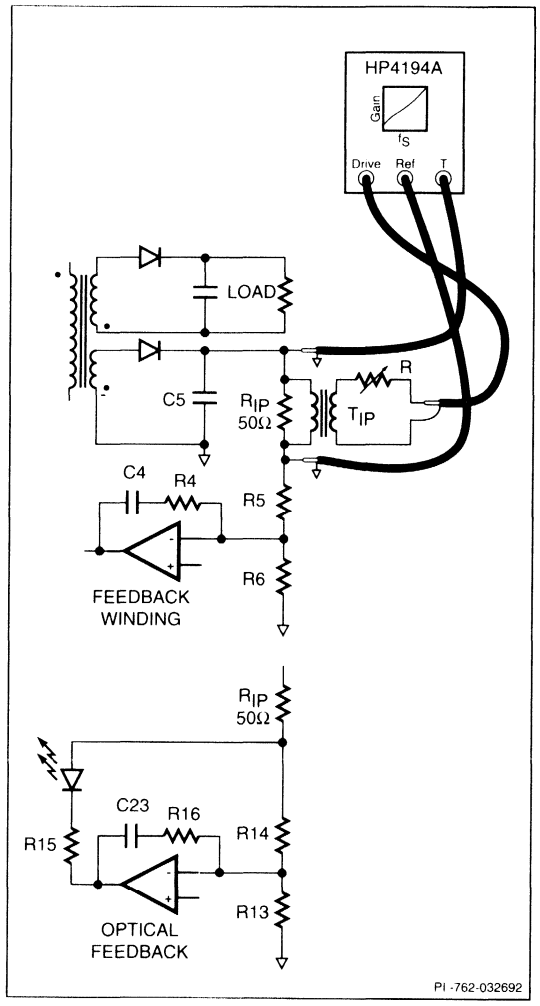

Figure 19.

Connect the output voltage return to the primary return with a short wire when measuring secondary referenced control loops. This will limit ground loops and reduce noise pickup in the instrumentation.

Optocoupler feedback circuits with postfilters require special attention. The post filter does not contribute significantly to the loop gain and phase response but interferes with the measurement. Temporarily connect the resistor divider to the input side of the post filter (or remove the postfilter completely) when making control loop gain/phase measurements.

Verification

There are some subtle issues that must be considered when making loop gain measurements. The most convenient points for measuring certain gain terms are inaccessible for direct measurement. Gain and phase response for these terms must be implied from measurements at accessible locations.

Power Path

Error Amplifier Output Impedance

Some products (SMP3, SMP110, SMP120, SMP210, SMP400) have a level shifting buffer that actually drives the EAO pin as shown in Figure 16. The buffer output impedance R_{ZO} is effectively between the EAO pin and the control voltage to the modulator. The power path frequency response can only be measured from the EAO pin of the power IC to the output voltage Vo (nodes 25 to 8). The measured power path gain will be higher at high frequency by a factor K_{ZO} depending on R_{ZO} and R4. The low frequency value is unity. The gain response breaks upward at a corner frequency defined by zero f_{ZZ} and breaks back to the flat gain f_{ZP} at a corner frequency defined by pole K_{ZP}:

$$K_{ZO} = \frac{(R_{ZO} + R_4)}{R_4} = \frac{(1.5k\Omega + 1.8k\Omega)}{1.8k\Omega} = 1.83 \text{ or } 5.26dB$$

$$f_{ZZ} = \frac{1}{2\pi \times (R_{ZP} + R_4) \times C_4}$$

$$= \frac{1}{2\pi \times (1.5k\Omega + 1.8k\Omega) \times 10nF} = 4.82 \text{ kHz}$$

$$f_{ZP} = \frac{1}{2\pi \times R_4 \times C_4} = \frac{1}{2\pi \times 1.8k\Omega \times 10nF} = 8.84 \text{ kHz}$$

The gain plots in Figure 20 show the real power path gain (nodes 13 to 8), the measured power path gain (nodes 25 to 8), and the measured power path gain with capacitor C4 changed to 1 µF.

Changing capacitor C4 to a large value temporarily will flatten out the power path gain response at a lower frequency and make it easier to extract the effective value for output resistance R_{E1}.

Output Resistance R_{E1}

Output resistance R_{E1} is extracted from the power path gain and phase response. Iteration with larger or smaller values for R_{E1} using SPICE will match the measured response. Increasing R_{E1} will flatten out the phase shift and move the first low pass filter corner frequency to lower values. Underdamped power stages will see reduced peaking. Decreasing R_{E1} has the opposite effect.

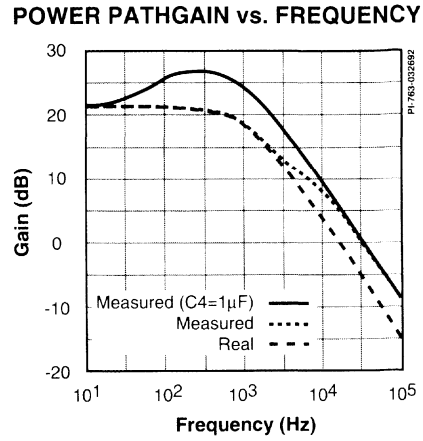

Figure 20.

FeedBack Winding

The feedback winding gain term cannot be directly verified because the V_e' voltage (node 23) is inaccessible. Trying to measure from V_O (node 8) to the feedback voltage (node21) will give erroneous measured results.

The best way to deduce feedback winding frequency response is to verify the power path and error amplifier frequency response and subtract graphically from the overall loop frequency response.

Feedback Resistance R_{E2}

Feedback resistance R_{E2} can be extracted from the loop gain and phase response. Iteration with larger or smaller values for R_{E2} using SPICE will match the measured response. Increasing R_{E2} will increase the high frequency phase shift (which is a more sensitive indicator than gain response).

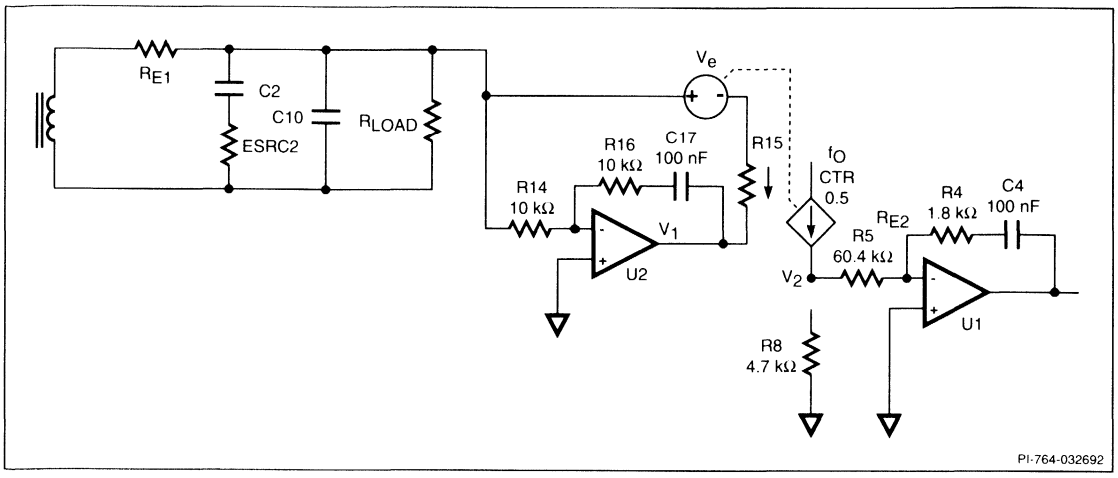

Figure 21.

Optocoupler Feedback

The optocoupler feedback circuit with LC postfilter previously shown in Figure 10 can be represented by the model in Figure 21. The error amplifier (U2) is physically located on the secondary side. For products not optimized for optocoupler feedback (PWR-SMP3, 110, 120, 210, 400) the amplifier internal to the power supply IC is connected as an inverting amplifier. The internal amplifier cannot be bypassed because of the buffer between the EAO pin and the modulator input signal. The dependent current-controlled current generator f_O models the current transfer ratio (CTR) of the optocoupler. The independent voltage source V_O is used as an ammeter by SPICE to measure the control current for f_O. The output current generates a voltage across resistor R8 which is then applied to the inverting amplifier within the power supply IC.

This circuit is characterized by a flat high frequency gain term K_O defined by optocoupler CTR (Current Transfer Ratio) and the high frequency gains of the error amplifier connection and inverting amplifier connection:

$$K_O = CTR \times \frac{R8}{R15} \times \left(1 + \frac{R16}{R14}\right) \times \frac{R4}{R5}$$

$$= 0.5 \times \frac{4.7k\Omega}{270\Omega} \times \left(1 + \frac{10k\Omega}{10k\Omega}\right) \times \frac{1.8k\Omega}{640k\Omega} = 0.519 \text{ or } -5.7dB$$

At high frequency the optocoupler is directly driven because the "1+" term error amplifier gain function has rolled off to a low value.

The error amplifier and optocoupler combination has a gain response that decreases at a 20 dB/decade rate until reaching a zero corner frequency f_{EZ} defined by resistors R16 and C17:

$$f_{EZ} = \frac{1}{2\pi \times R16 \times C17} = \frac{1}{2\pi \times 10k\Omega \times 100nF} = 159 \text{ Hz}$$

The LC postfilter usually has little effect on the overall error amplifier gain for two reasons: the LC corner frequency is usually much higher than f_{EZ} and the filter can only roll off the low gain even further.

The inverting amplifier has a gain response that decreases at a 20 dB/decade rate until reaching a zero corner frequency f_{IZ} defined by resistors R4 and C4:

$$f_{IZ} = \frac{1}{2\pi \times R4 \times C4} = \frac{1}{2\pi \times 1.8k\Omega \times 100nF} = 884 \text{ Hz}$$

The effective gain and phase response is shown in Figure 22.

For products optimized for use with optocouplers refer to the appropriate data sheet and evaluation board documentation for further information.

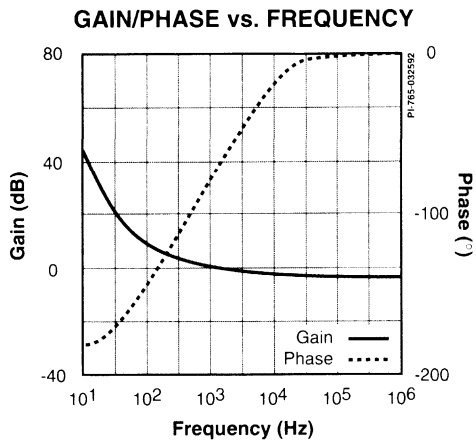

Figure 22.

References

1 B.R. Leman, "Regulated Flyback Converter with Spike Suppressing Coupled Inductors", US Patent #5,008,794, April 16, 1991

2 R.D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching Converter Power Stages", IEEE Power Electronics Specialists Conference, June 1976, pp18-34

3 PSPICE from MicroSim Corporation

4 Analog Workbench from Cadence Design Systems, Inc. (formerly Valid Logic Systems (formerly Analog Design Tools))

Power Capability of the PWR-SMP Family

APPLICATION NOTE AN-9

Each PWR-SMP device can deliver a variety of power levels depending on design factors which include switching frequency, effective minimum DC input voltage, MOSFET switch peak drain current, current waveform shape, parasitic drain capacitance, actual local ambient temperature, and effective thermal impedance. The analysis procedure presented here will show how to determine output power, power dissipation, efficiency, and junction temperature for the PWR-SMP family of devices.

Two key transformer parameters are also extracted during this analysis. Primary inductance and primary winding to secondary winding turns ratio, which are essential information for specifying the power transformer (see DA-3 and AN-7) are convenient to calculate here. The input capacitor which stores energy between the peaks of the AC input voltage is also determined during this analysis.

The analysis will proceed as follows:

- Choose the PWR SMP device and switching frequency
- Determine the MOSFET current magnitude and shape
- Calculate DC (forward) power losses in the switch
- Calculate AC (switching) power losses in the switch
- Calculate linear regulator bias power in the IC
- Calculate power supply efficiency
- Estimate maximum device junction temperature

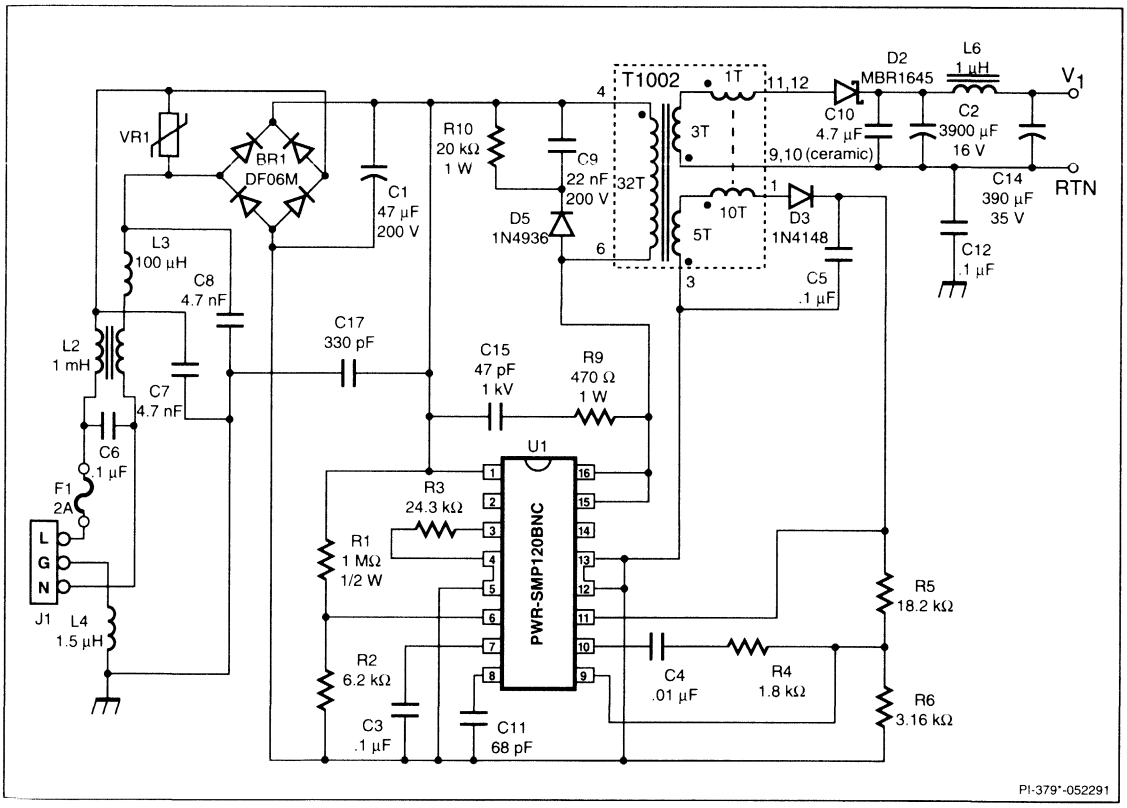

Figure 1. Schematic Diagram of the Example Power Supply Circuit.

Iteration may be necessary to settle on a final solution. If the junction temperature is too high for the desired output power level one or more of the following actions will be required:

- Reduce the switching frequency
- Operate from a higher minimum DC input voltage
- Choose a current waveform with lower RMS value
- Improve thermal impedance with a heat sink
- Use a higher power PWR-SMP device

This procedure can be entered quite easily into a spreadsheet program on a personal computer. Iterations can be reduced to a few keystrokes for evaluating different approaches or operating conditions.

A 15 watt, 110 VAC power supply application will be used to illustrate the techniques presented. A demonstration power supply (PWR-EVAL3) based on the PWR-SMP120 and the T1002 standard transformer will serve as an example in the appendix section of this design aid. The schematic is given in Figure 1.

General Description

Flyback power supplies operate by alternately storing energy in the core of the power transformer core when the MOSFET switch is on and releasing energy to the load when the switch is off. While the switch is on transformer primary current (and MOSFET drain current) ramps up linearly from a starting value (I_S) to a final peak value (I_{PK}) which slowly builds a magnetic field in the transformer core. Figure 2 shows three typical trapezoidal drain current waveforms with period (t), on time (t_{on}), and off time (t_{off}).

The drain current waveform has a peak, an average, and an RMS value. Each plays a different role in power supply behavior. The maximum value of the peak current is fixed by the PWR SMP device used. The average value determines the output power. The RMS value is used to calculate the DC or forward loss in the PWR SMP device.

When the switch turns off drain current drops abruptly to zero, concluding the energy storing part of the cycle. Secondary current jumps to a peak value and linearly ramps down as energy is delivered to the load by the decaying magnetic field in the transformer core. The energy stored in the transformer core may or may not be completely delivered to the load each cycle depending on whether the magnetic field (and secondary current) decays all the way to zero. If secondary current ramps down to zero there will be no magnetic field or energy left in the core which defines "discontinuous mode". The magnetic field did not "continue" into the start of the next switching cycle. If secondary current ramps down to a final value greater than zero a magnetic field and stored energy will still be left in the core which defines "continuous mode". Continuity of the magnetic

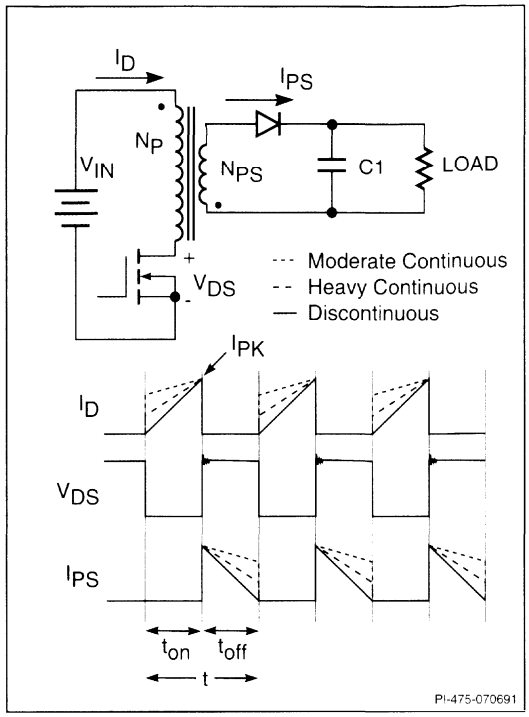

Figure 2. Current Waveforms for Continuous and Discontinuous Conduction.

field in a flyback converter is analogous to current continuity in the buck-boost converter from which it was derived.

Examples of three different waveforms given in Figure 2 illustrate discontinuous, moderate continuous, and heavy continuous operation. Note that the current in the MOSFET switch will have an initial value (I_S) in the continuous mode of operation but starts at zero ($I_S = 0$) in the discontinuous mode.

Discontinuous operation results in the smallest transformer (smallest primary inductance) but cannot deliver as much power as the continuous mode. The average value of the drain current is lowest while the RMS value is highest for a given peak current and results in highest DC or forward losses.

Heavy continuous operation has a drain current waveform with the lowest RMS value and highest effective average or DC current value and delivers the highest power to the load for a given peak current. Lower peak currents can be selected which reduce forward losses but at the expense of increased transformer size (higher primary inductance). A good switching power supply design balances these factors for an optimum implementation.

Device and Frequency Selection

The data sheet for each PWR-SMP device contains the output power rating for a typical open frame power supply operating at room temperature. A power versus frequency curve can also be found which indicates the output power limit that can be expected as a function of frequency with a 25°C ambient, 100°C case temperature, and no heat sink. Higher effective ambient temperatures require either reducing the amount of output power or the addition of a heat sink. The PWR-SMP120 power versus frequency curve is shown in Figure 3.

The device can dissipate a fixed amount of total power based on the allowable temperature rise and thermal impedance. The total power (P_T) is actually the sum of AC and DC power losses. AC power losses (P_{AC}) increase with switching frequency and input voltage but are relatively independent of the output power level. DC power losses (P_{DC}) increase with the output power level and decrease with input voltage (V_{IN}) (due to lower duty cycle) but are relatively independent of switching frequency (eq 1).

$$P_T = P_{AC}(f, V_{IN}) + P_{DC}(P_O, V_{IN}) \quad (1)$$

Worst case total power losses usually occur at low line operation and are dominated by forward losses. At higher switching frequencies the increased AC loss must be balanced with a reduced DC loss to maintain the same total losses (P_T) and maximum junction temperature. The power versus frequency curve shows the relationship between AC and DC losses for a fixed low line input voltage V_{IN}. The highest switching frequency capable of providing the desired power level should be selected in order to minimize the size of the energy storage components, especially the power transformer.

The curve in Figure 3 indicates that a typical power supply operating providing 15 watts at 25°C ambient can switch at up to 700 kHz. Operating at greater than 25°C ambient temperature will require reducing AC power loss by using a lower switching frequency. Start with a lower switching frequency (such as 250 kHz), analyze losses and junction temperature, and iterate if necessary to the final switching frequency.

Linear Regulator Losses

Each device in the PWR-SMP family of products has two linear regulators: a high voltage linear regulator operating from rated DC input voltage and a low voltage linear regulator operating from a nominal 8.5 volt feedback voltage. During normal operation the high voltage regulator is cut off dissipating negligible amounts of power. The low voltage regulator dissipates small amounts of power (P_{LR}) determined by the feedback voltage and the bias current.

OUTPUT POWER vs. FREQUENCY

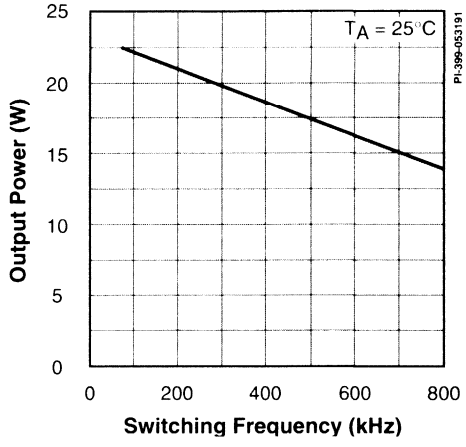

Figure 3.

Total Device Power Losses

Total device power loss is the sum of AC loss, DC loss, and linear regulator losses at each of the DC input voltages (eq 2). The highest total power loss is then used to calculate junction temperature.

$$P_T = P_{AC} + P_{DC} + P_{LR} \quad (2)$$

Efficiency

Power supply efficiency depends not only on the losses in the integrated circuit, but in other components as well. Two additional power loss terms can be defined for the output rectifier (P_R) and transformer (P_X). Efficiency (η) is determined by simply dividing the output power by the total power lost in the power supply (eq 3).

$$\eta = \frac{P_O}{P_T + P_X + P_R} \quad (3)$$

Thermal Impedance

The concept of thermal impedance is used to estimate the junction temperature of a semiconductor device as a function of the power level dissipated by that device. The product of thermal impedance (Θ) and dissipated power (P_D) is the rise in temperature between the semiconductor junction and a predetermined reference point (4).

$$T_{RISE} = P_D \times \Theta \quad (4)$$

Thermal impedance can be defined three different ways: Junction to Ambient, Junction to PC board, and Junction to Case. Units for thermal impedance are degrees Centigrade per watt (°C/W).

Junction to Ambient thermal impedance (Θ_{JA}) is used to estimate the temperature rise from the semiconductor junction to the local ambient air temperature. (Θ_{JA}) is measured with the PWR-SMP device soldered into a PC board with the COM pins connected to a primary referenced copper plane (refer to DA-2 on PC layout). Heat flows from the device junction to the stamped IC leadframe, down the "Batwing" pins (4, 5, 12, 13) to the PC board, and out to the ambient air by natural convection. The effective value of junction to ambient thermal impedance can vary from one application to the next depending on the extent of the ground plane, size of the PC board, and the heating effects of other power components (such as the power transformer and output rectifier). Typical junction to ambient thermal impedance is 43°C/W when there are no other power components heating the PC board.

For applications with other power components heating the PC board a different thermal impedance is used. Junction to PC board thermal impedance (Θ_{JPCB}) is used to estimate the temperature rise from the semiconductor junction to the PC board. Heat flows through the pins of the PWR-SMP device to the PC board as described before. Typical junction to PC board thermal impedance (Θ_{JPCB}) is 15°C/W. The PC board temperature measured between the batwing pins (4, 5, 12, 13) is used as the reference point. This temperature is measured with the power supply operating at maximum specified ambient temperature, maximum load, and low line input voltage. The thermal environment (enclosed in a box, natural convection, forced air, etc.) should closely approximate the actual application.

Heat sinks should be used in applications requiring the highest output power or operation in the highest ambient temperature. Junction to Case thermal impedance (Θ_{JC}) is used to estimate the temperature rise from the semiconductor junction to a heat sink attachment point on the power supply IC. The heat sink attachment point is shown in Figure 4. Typical junction to case thermal impedance (Θ_{JC}) is 6°C/W. Heat sinks that attach either mechanically or by soldering to the attachment points deliver the best performance with the Batwing Power DIP package. The Staver[1] heat sink model V8-3 made of tin plated copper with thermal impedance (Θ_{CA}) of 20°C/W is a good example. The heat sink solders directly to the proper attachment points of the IC. Another attachment method uses a slot in the PC board into which both the IC pins and heat sink tabs are soldered. Heat sinks which attach to the plastic case are not recommended. The heat conduction path is from the device junction through the leadframe to the heat sink attachment point, up through the heat sink, and out to the ambient air by natural conduction.

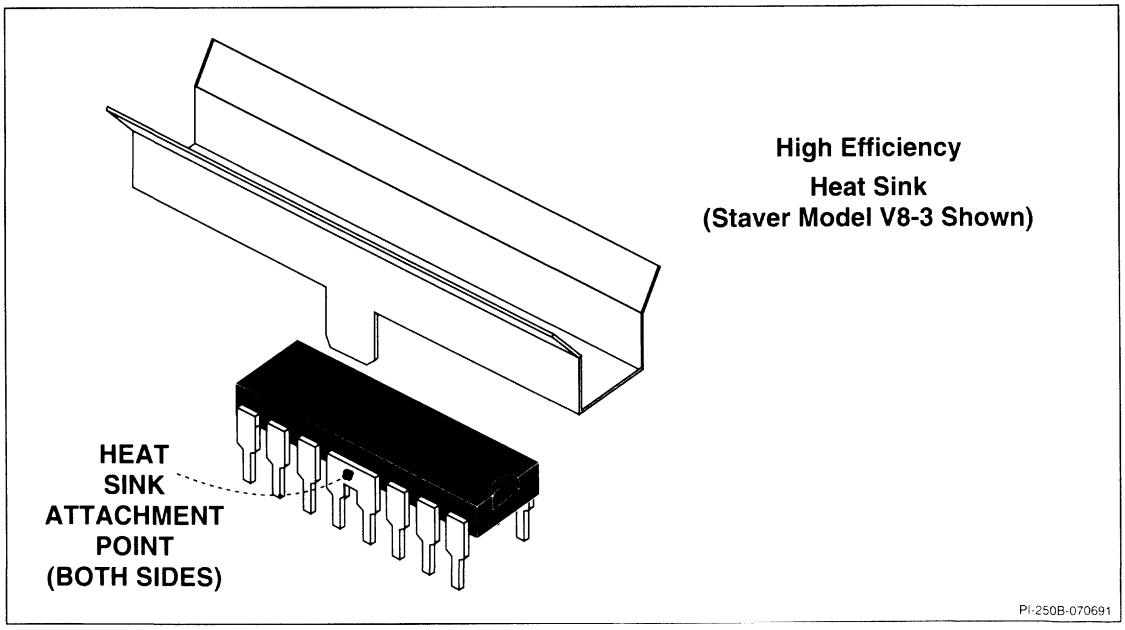

Figure 4. Attaching a Heatsink to the Package.

APPENDICES

APPENDIX A:
Calculation of Drain Current Parameters and DC (Conduction) Losses

The DC or forward losses are simply I^2R losses caused by drain current flowing through the effective resistance between the drain and source of the MOSFET switch. Estimating the DC loss requires calculating the effective RMS value of the drain current waveform. The drain current waveform (and DC loss) changes with increasing input voltage. The procedures given here show how to calculate the RMS value of the drain current waveform (and DC loss) at low line. Losses at high line are then calculated with a simple extension of the low line procedure.

At Low Line Input Voltage:

1) Estimate efficiency and calculate input power
2) Establish minimum DC input voltage and input capacitor
3) Select peak drain current and calculate $R_{DS(ON)}$
4) Determine maximum duty cycle from data sheet
5) Estimate power losses in other components
6) Determine current waveform shape, average and RMS value
7) Calculate low line DC loss
8) Calculate transformer primary inductance and turns ratio

Efficiency and Input Power

Input power (P_{IN}) can be determined from the output power (P_O) and an estimate of power supply efficiency (η) (eq 5). The efficiency number can be refined after the first pass through the analysis for successive iterations.

$$P_{IN} = \frac{P_O}{\eta} \qquad (5)$$

Effective DC Input Voltage and Input Capacitance

In off-line applications AC input voltage is rectified and filtered to provide a high voltage DC bus with a superimposed ripple voltage (V_R) at twice the line frequency as shown in Figure 5. Peak to peak ripple voltage is usually kept between 20 and 40 volts. Capacitor C1 is charged to the peak value of the AC input voltage waveform (V_{MAX}) (eq 6). The capacitor discharges slowly for approximately 40% of the AC line cycle to a minimum DC voltage (V_{MIN}) (eq 7). During this time energy stored in the capacitor is delivered to the power supply input.

$$V_{MAX} = \sqrt{2} \times V_{AC} \qquad (6)$$

$$V_{MIN} = V_{MAX} - V_R \qquad (7)$$

The value of capacitor C1 can be calculated if the input power is known. Capacitor C1 is then found from the input power, maximum voltage, minimum voltage, and line frequency (f_{AC}) (eq 8).

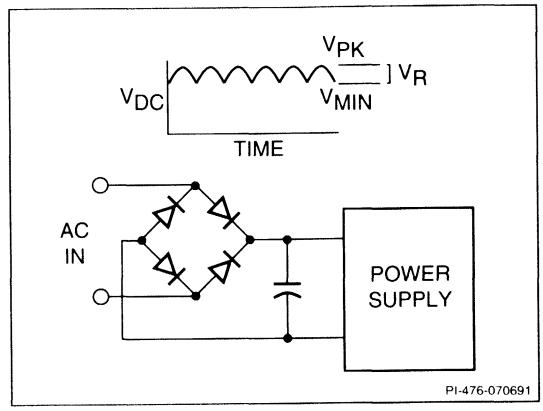

Figure 5. Input Voltage Relationships.

$$C1 = \left(\frac{2 \times P_{IN}}{\left(V_{MAX}^2 - V_{MIN}^2 \right)} \right) \times \frac{0.4}{f_{AC}} \qquad (8)$$

Peak Current and $R_{DS(ON)}$

Peak current can be selected at any level up to the current limit value. For devices without internal current limit (such as the PWR-SMP110) the peak current limit will be determined by the power dissipation in the application. The minimum On State Current value given in the specification for each device represents a practical limit on the peak current.

The effective voltage across the transformer primary is actually the difference between the DC input voltage and the Drain-Source voltage of the MOSFET switch. Significant errors can result if the voltage drop across the switch as a function of drain current is not taken into account. Figure 6 shows a typical VI characteristic (drain-source voltage versus drain current) for the PWR-SMP120. This curve can be found in the data sheet for each member of the PWR-SMP family of products. The nonlinear nature of the voltage-current relationship has advantages and disadvantages. The disadvantage is slightly higher apparent "on resistance" at higher drain currents. The advantage is that drain current never exceeds a maximum value which improves device reliability under fault conditions. Use this curve to predict the Drain-Source voltage Vds at specific values of drain current.

Finding DC power loss requires an estimate of power MOSFET $R_{DS(ON)}$. An approximate value for the effective $R_{DS(ON)}$ is simply the ratio of the drain source voltage (from the VI curve in Figure 6) and peak drain current (eq 9).

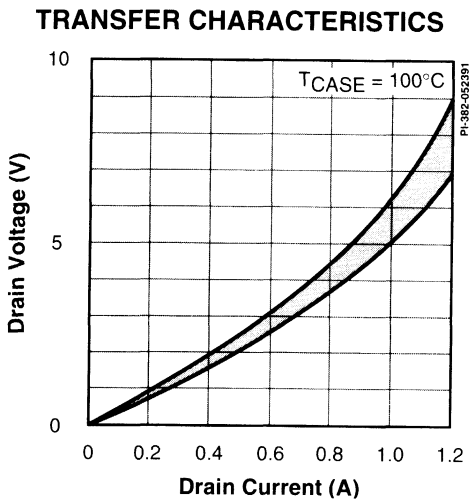

Figure 6.

$$R_{DS(ON)} = \frac{V_{DS}}{I_{PK}} \quad (9)$$

Effective Maximum Duty Cycle

The maximum duty cycle (D) is a slight function of frequency in the PWR-SMP product line. Maximum duty cycles of 50% are typical for lower frequency operation while 40% is normal at higher frequencies. Refer to the data sheet for maximum duty cycle for the selected device.

Estimated External Component Power Loss

The output power is equal to the difference between the input power and the losses in the power supply. Losses occur primarily in the power supply IC, output rectifier (P_D), and power transformer (P_X). It is useful to define an "efficiency" η_X (eq 10) that excludes the losses in the power supply IC, which will be determined later.

$$\eta_X = \frac{P_O}{P_O + P_D + P_X} \quad (10)$$

Average Drain Current, Waveshape, and RMS Current

The average drain current (I_{AVG}) can now be calculated from P_O, V_{MIN}, V_{DS}, I_{PK}, and η_X (eq 11).

$$I_{AVG} = \frac{P_O}{\left(\eta_X \times \left(V_{MIN} - V_{DS}\right)\right)} \quad (11)$$

The drain current waveshape can be split into two components as shown in Figure 7; a pulse current (I_{PULSE}) with a superimposed ripple current (I_R). Pulse current is defined as the quotient of average current and maximum duty cycle (eq 12). Ripple current is derived from pulse current and peak drain current (eq 13). Waveshape factor (K), which defines the relative

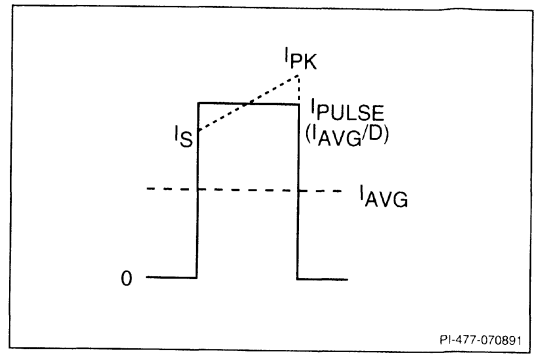

Figure 7. Relationship of Current Components.

"squareness" of the drain current waveform, can be defined as the ratio of ripple current to the peak current (eq 14).

$$I_{PULSE} = \frac{I_{AVG}}{D} \quad (12)$$

$$I_R = 2 \times \left(I_{PK} - I_{PULSE}\right) \quad (13)$$

$$K = \frac{I_R}{I_{PK}} \quad (14)$$

DC losses can be calculated from the RMS current (I_{RMS}). I_{RMS} is a function of peak drain current, waveshape factor K, and maximum duty cycle D (eq 15).

$$I_{RMS} = I_{PK} \times \sqrt{D \times \left(\frac{K^2}{3} - K + 1\right)} \quad (15)$$

RMS current normalized to peak drain current as a function of form factor and maximum duty cycle is given in Figure 8. Note that smaller values of K correspond to a heavier continuous mode operation and higher output power capability. Discontinuous operation has a K of 1. For a given duty cycle and waveshape factor, determine the normalized RMS current factor (F_{RP}) and multiply by peak current (eq 16).

$$I_{RMS} = F_{RP} \times I_{PK} \quad (16)$$

Low Line DC Losses

The DC power loss is then simply the product of $R_{DS(ON)}$ and the square of the RMS current (eq 17).

$$P_{DC} = I_{RMS}^2 \times R_{DS(ON)} \quad (17)$$

Highest DC loss occurs at low line and will be used later for estimating maximum junction temperature. In some cases the forward loss must be calculated for higher DC input voltages. This requires the calculation of the transformer primary inductance (L_p).

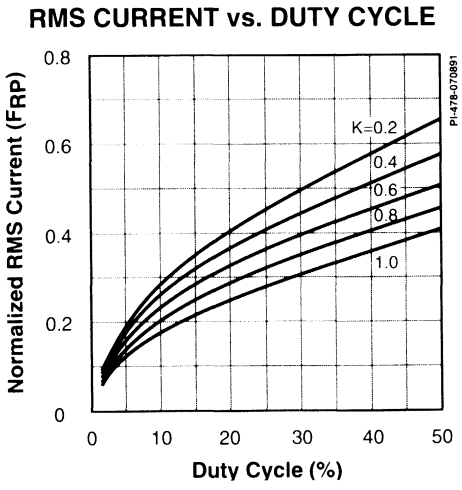

Figure 8.

Transformer Primary Inductance and Turns Ratio

Transformer primary inductance can be calculated from V_{MIN}, V_{DS}, I_R, D, and f_S (eq 18).

$$L = (V_{MIN} - V_{DS}) \times \left(\frac{D}{f_S \times I_R} \right) \quad (18)$$

AC or switching loss analysis requires the calculation of the transformer primary to secondary turns ratio [N_P/N_{PS}] to determine how the output voltage reflects back to the primary. The turns ratio is found from V_{MIN}, V_{DS}, D, and output diode drop (V_D), and V_O (eq 19).

$$\frac{N_P}{N_{PS}} = \frac{D}{1-D} \times \left(\frac{V_{MIN} - V_{DS}}{V_O + V_D} \right) \quad (19)$$

DC Losses at Higher DC Input Voltages

Average drain current, peak drain current, and duty cycle all change as the DC input voltage increases. New values for these parameters must be determined for estimating DC losses at other operating conditions. These new values can be predicted using an extension of the low line procedure.

Additional steps for higher DC input voltage conditions:

1) Determine new DC input voltage
2) Determine new average drain current
3) Determine new duty cycle
4) Determine shape of drain current waveform
5) Determine RMS value of Drain current waveform
6) Determine new $R_{DS(ON)}$
7) Calculate DC losses at desired DC input voltage
8) Repeat for each new DC input voltage

New DC Input Voltage

The new DC maximum input voltage (V_{MAX}') is derived from a new AC input voltage (V_{AC}') (eq 20). This voltage will also have a ripple voltage (V_R') and a minimum DC value (V_{MIN}'). V_{MIN}' is found from input power (P_{IN}), the capacitance value C1 previously found, new maximum input voltage (V_{MAX}'), and line frequency (f_{AC}) (eq 21). The average DC voltage value (V_{DC}') of the new maximum and minimum voltages should be used for subsequent power calculation (eq 22).

$$V_{MAX}' = \sqrt{2} \times V_{AC}' \quad (20)$$

$$V_{MIN}' = \sqrt{V_{MAX}'^2 - \left(\frac{2 \times P_{IN}}{C1} \times \frac{0.4}{f_{AC}} \right)} \quad (21)$$

$$V_{DC}' = \frac{V_{MAX}' + V_{MIN}'}{2} \quad (22)$$

New Average Drain Current

Switching power supplies draw a constant amount of input power over the entire input voltage range (assuming constant efficiency). As the input voltage increases, the average input current decreases to maintain the same power level. New average current (I_{AVG}') is calculated from VIN' (eq 23) with all other parameters the same as before:

$$I_{AVG}' = \frac{P_O}{\eta_X \times (V_{DC}' - V_{DS})} \quad (23)$$

New Duty Cycle

The duty cycle decreases with increasing input voltage. The difference voltage (ΔV) between V_{DC}' and V_{MIN}' (eq 24) together with maximum duty cycle (D) are used to determine the new duty cycle (D') (eq 25).

$$\Delta V = V_{DC}' - V_{MIN}' \quad (24)$$

$$D' = \frac{V_{MIN}' \times D}{(\Delta V \times (1-D)) + V_{MIN}'} \quad (25)$$

New Current Waveform Shape

Ripple current (I_R') is calculated from V_{DC}', V_{DS}, D', f_S, L_P (eq 26).

$$I_R' = \frac{(V_{DC}' - V_{DS}) \times D'}{f_S \times L_P} \quad (26)$$

New RMS Current Value

The new peak current (I_{PK}') can be found from D', I_R', and I_{AVG}' (eq 27).

$$I_{PK}' = \frac{I_{AVG}'}{D'} + \frac{I_R'}{2} \quad (27)$$

4

The new form factor (K') is found from I_R' and I_{PK}' (eq 28).

$$K' = \frac{I_R'}{I_{PK}'} \quad (28)$$

The new RMS current (I_{RMS}') can be found by using equation 14 or using the curves in Figure 7.

New ON Resistance

The new on resistance ($R_{DS(ON)}$') is found from V_{DS}' and I_{PK}'. Use I_{PK}' and the VI characteristic curve (Figure 5) to determine a new drain-source voltage (V_{DS}'). $R_{DS(ON)}$' is simply the quotient of V_{DS}' and I_{PK}' (eq 29).

$$R_{DS(ON)}' = \frac{V_{DS}'}{I_{PK}'} \quad (29)$$

New DC Power Loss

The new DC power (P_{DC}') is simply the product of $R_{DS(ON)}$' and the square of I_{RMS}' (eq 30).

$$P_{DC}' = I_{RMS}^2 \times R_{DS(ON)}' \quad (30)$$

Example:

Power Supply Parameters:

Input:	80 to 140 VAC, 60 Hz
Output:	5 Volts, 15 Watts
Other parameters:	
Hi Voltage DC Bus Ripple:	40 Volts, peak to peak
Initial Efficiency Estimate:	70% (0.7)

Low Line DC Loss Calculation

$$P_{IN} = \frac{15W}{0.7} = 21.4W$$

$$V_{MAX} = \sqrt{2} \times 80V = 113V$$

$$V_{MIN} = 113V - 40V = 73V$$

$$C1 = \left(\frac{2 \times 21.4W}{113^2 - 73^2}\right) \times \frac{0.4}{60} = 38\mu F$$

(Typical capacitor tolerances of +/- 20% require selection of a higher nominal value: 47 µF)

The PWR-SMP120 peak drain current is 900 mA minimum. For lowest forward losses, start with a lower value (660 mA in this example) for the first pass through the analysis. Adjust this value through iteration if necessary to achieve desired output power and junction temperature.

Find VDS from the VI curve in Figure 6. For a drain current of 660 mA, V_{DS} is 3.8 volts.

For a V_{DS} of 3.8 volts and I_{PK} of 660 mA on resistance ($R_{DS(ON)}$) is found to be 5.8 Ω.

$$R_{DS(ON)} = \frac{3.8V}{660mA} = 5.8\Omega$$

Refer to the PWR-SMP120 data sheet for maximum duty cycle (D) as a function of frequency. For 250 kHz, the maximum duty cycle is 45%.

The output diode loss (P_D) is typically 10% of the output power (P_O), while transformer loss (P_X) is typically 5% of the output power.

$$P_D = 0.1 \times 15W = 1.5W$$

$$P_X = 0.05 \times 15W = 0.75W$$

$$\eta_X = \frac{15W}{(15W + 1.5W + 0.75W)} = 0.87$$

$$I_{AVG} = \frac{15W}{(0.87 \times (73 - 3.8))} = 249mA$$

$$I_{PULSE} = \frac{249mA}{0.45} = 553mA$$

$$I_R = 2 \times (660mA - 553mA) = 214mA$$

$$K = \frac{214mA}{660mA} = 0.324$$

$$I_{RMS} = 660mA \times \sqrt{0.45 \times \left(\frac{0.324^2}{3} - 0.324 + 1\right)} = 373mA$$

$$P_{DC} = (382mA)^2 \times 5.8\Omega = 808mW$$

$$L = (73V - 3.8V) \times \left(\frac{0.45}{250kHz \times 214mA}\right) = 582\mu H$$

$$\frac{N_P}{N_{PS}} = \left(\frac{0.45}{(1 - 0.45)}\right) \times \frac{(73V - 3.8V)}{(5.0V + 0.4V)} = 10.5$$

High Line DC Loss Calculation

$$V_{MAX}' = \sqrt{2} \times 140V = 198V$$

$$V_{MIN}' = \sqrt{198^2 - \left(\left(\frac{2 \times 21.4}{47\mu F}\right) \times \frac{0.4}{60}\right)} = 182V$$

$$V_{DC}' = \frac{(198V + 182V)}{2} = 190V$$

$$I_{AVG}' = \frac{15W}{(0.87 \times (190 - 3.8))} = 97mA$$

$$\Delta V = 190V - 73V = 117V$$

$$D' = \frac{73V \times 0.45}{(117V \times 1 - 0.45) + 73V} = 0.239$$

$$I_R' = (190V - 3.8V) \times \frac{0.239}{(250kHz \times 670\mu H)} = 249mA$$

$$I_{PK}' = \left(\frac{97mA}{0.239}\right) + \left(\frac{249mA}{2}\right) = 530mA$$

$$K' = \frac{249mA}{530mA} = 0.470$$

$$R_{DS(ON)}' = \frac{3.0V}{530mA} 5.66\Omega$$

$$I_{RMS}' = 530mA \times \sqrt{0.239 \times \left(\frac{0.478^2}{3} - 0.478 + 1\right)} = 200mA$$

$$P_{DC}' = (200mA)^2 \times 5.66\Omega = 226mW$$

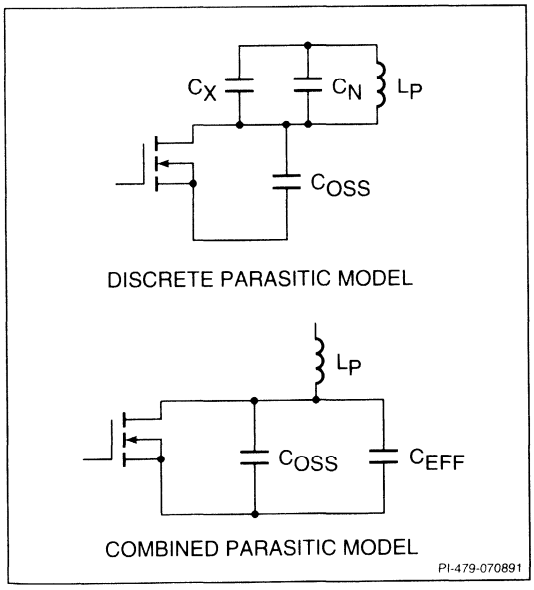

Figure 9. Parasitic Capacitance Terms.

APPENDIX B:
Calculation of AC (Switching) Losses

Switching losses in the MOSFET switch are due to the equivalent output capacitance present at the drain node. Figure 9 shows three different capacitance terms which include the MOSFET output capacitance (COSS), power transformer capacitance (C_X) and effective capacitance (C_N) of the clamp/damping network. These terms can be represented by the parallel combination of C_{OSS} and linear capacitor C_{EFF}, which combines C_N and C_X (eq 31)

$$C_{EFF} = C_N + C_X \quad (31)$$

These capacitance terms store energy each cycle by charging up to significant voltage levels when the MOSFET switch is turned off. The energy is dissipated in the IC when the MOSFET switch is turned on. The AC loss (P_{AC}) is the product of stored energy (per cycle) and switching frequency as shown (eq 32).

$$P_{AC} = E \times f_S \quad (32)$$

The energy (E_{OSS}) stored in the MOSFET output capacitance C_{OSS} can be found from the stored energy curve given for each member of the PWR-SMP family of devices. The curve for the PWR-SMP120 is given in Figure 10. The drain voltage must first be calculated from the input voltage and reflected output voltage. Reflected output voltage (V_O') is equal to power supply output voltage (V_O) multiplied by transformer turns ratio (N_P/N_{PS}) (eq 33). The voltage present on the drain capacitance terms (V_C) is the sum of the average DC input voltage (found from V_{MAX} and V_{MIN}) and V_O' (eq 34). The energy (E_{EFF}) stored each cycle in the linear effective capacitance (C_{EFF}) can be found from equation 35.

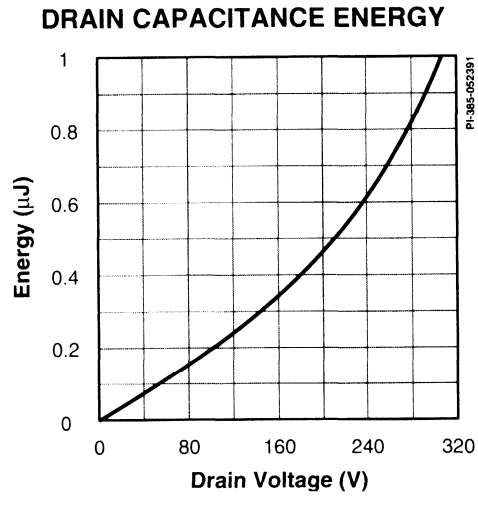

Figure 10.

$$V_O' = (V_O + V_D) \times \frac{N_P}{N_{PS}} \quad (33)$$

$$V_C = \frac{(V_{MAX} + V_{MIN})}{2} + V_O' \quad (34)$$

$$E_{EFF} = 0.5 \times C_{EFF} \times V_C^2 \quad (35)$$

Total MOSFET switching power loss (P_{AC}) is the sum of two energy terms (E_{OSS}) and (E_{EFF}) multiplied by the switching frequency (f_S) (eq 36).

$$P_{AC} = (E_{OSS} + E_{EFF}) \times f_S \quad (36)$$

Example:

Power Supply Parameters:

$C_N = 47$ pF $\qquad C_X = 13$ pF

Low Line AC Loss Calculation

$$C_{EFF} = 47pF + 13pF = 60pF$$

$$V_O' = (5.0V + 0.4V) \times 10.5 = 56.6V$$

$$V_C = \frac{(113V + 73V)}{2} + 56.6V = 149.6V$$

From the energy curve in Figure 10, E_{OSS} is 320 nJ. For a C_{EFF} of 60 pF, E_{EFF} is found to be 671 nJ.

$$E_{EFF} = 0.5 \times 60pF \times V_C^2 = 671nJ$$

$$P_{AC} = (671nJ + 320nJ) \times 250kHz = 246mW$$

High Line AC Loss Calculation

For capacitance voltage (V_C) of 247 volts, E_{EFF}' is found to be 1830 nJ. The high line AC losses are found to be 505 mW.

$$V_C' = \frac{(198V + 182V)}{2} + 56.6V = 247V$$

$$E_{EFF}' = 0.5 \times 60pF \times (247V)^2 = 1830nJ$$

The energy (E_{OSS}') stored in the MOSFET output capacitance (C_{OSS}) is found from Figure 9 to be 190 nJ.

$$P_{AC}' = (1830nJ + 190nJ) \times 250kHz = 505mW$$

APPENDIX C:
Calculation of Linear Regulator Losses

Linear regulator power losses (PLR) are quite simple to calculate. The power dissipated is equal to the voltage (V_{BIAS}) multiplied by the bias current (I_{BIAS})] (eq 37). During normal operation bias is provided by the feedback voltage derived from a transformer winding.

$$P_{LR} = V_{BIAS} \times I_{BIAS} \quad (37)$$

During fault conditions (such as current limit or over temperature) the feedback voltage is not available. In this case the bias voltage is the high voltage DC input which can cause significant power dissipation. In some cases the bias power may actually be high enough to trip the over temperature protection and "latch" in the off mode.

Example: during normal operation with a feedback voltage of 8.5 volts at pin 11 and a bias current of 5 mA the power dissipation (P_{LR}) is 42.5 mW. During an overtemperature fault condition at high line (198 volts at pin 1) with the same bias current, P_{LR} is 990 mW.

APPENDIX D:
Total Device Power and Efficiency

Total device power is the sum of AC, DC, and linear regulator losses (eq 38).

$$P_T = P_{AC} + P_{DC} + P_{LR} \quad (38)$$

Total power supply input power is the sum of PWR-SMP device total power loss (P_T), diode power loss (P_D), and transformer power loss (P_X) (eq 39).

$$P_{IN} = P_T + P_D + P_X \quad (39)$$

Power supply efficiency (η) is found by dividing the output power (P_O) by the input power (P_{IN}) (eq 40).

$$\eta = \frac{P_O}{P_{IN}} \quad (40)$$

Example:

For low line conditions, DC losses are 808 mW, AC losses are 205 mW, and linear regulator losses are 42.5 mW. The total low line loss is found to be 1.056 Watts. For high line conditions, DC losses are 226 mW, AC losses are 505 mW, and linear regulator losses are 42.5 mW. The total high line loss is 774 mW. Use the low line loss for the junction temperature analysis. Efficiency is found to be 82%.

Note that this efficiency is quite a bit better than the original estimate of 70%. Another iteration through the analysis will improve the overall accuracy.

APPENDIX E:
Calculation of Junction Temperature

For applications where other components are not heating the PC board, the junction temperature (T_J) is estimated from the total power dissipated in the package (P_T), the ambient temperature (T_A), and the junction to ambient thermal impedance (Θ_{JA}) of the application (eq 41).

$$T_J = T_A + (P_T \times \theta_{JA}) \quad (41)$$

For applications where other components are heating the PC board, T_J is estimated from P_T, the PC board temperature (T_{PCB}), and the junction to PC board thermal impedance (Θ_{JPCB}) of the application (eq 42).

$$T_J = T_{PCB} + (P_T \times \theta_{JPCB}) \quad (42)$$

For applications with a heat sink dissipating power to the ambient air, the new junction to ambient thermal impedance (Θ_{JA}) is the sum of junction to case, case to heat sink, and heat sink to ambient thermal impedances (43).

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (43)$$

It is important to note that the case to heat sink thermal impedance is negligible.

Example #1: IC Through PC Board to Ambient
For a 45°C effective ambient temperature, a total device power dissipation of 1.056 watts, and a junction to ambient thermal impedance of 43°C/W (no heat sink), the junction temperature will be 90.4°C.

$$T_J = 45°C + (1.056W \times 43°C / W) = 90.4°C$$

Example #2: IC to PC Board
For a measured PC board temperature of 70°C, a junction to PC board thermal impedance of 15°C/W, and a total device dissipation of 1.056 watts, the junction temperature is found to be 86°C.

$$T_J = 70°C + (1.056W \times 15°C / W) = 86°C$$

Example #3: IC Through Heat Sink to Ambient
For a junction to case thermal impedance of 6°C/W and heat sink to ambient thermal impedance of 20°C/W the new junction to ambient thermal impedance is 26°C/W. For a total device dissipation of 1.056 watts and ambient temperature of 45°C, the junction temperature is found to be 72.5°C.

$$Q_{JA} = 6°C / W + 20°C / W = 26°C / W$$

$$T_J = 45°C + (1.056W \times 26°C / W) = 72.5°C$$

References

(1)Staver Company, Inc.; 41 Saxon Avenue, Bay Shore, NY 11706; 516-666-8000

Function and Application of the PWR-INT200-202

APPLICATION NOTE AN-10

POWER INTEGRATIONS, INC.

Introduction

The PWR-INT200/201/202 comprise a family of devices designed to drive N-channel MOSFET transistors in a half bridge configuration. High-voltage integrated technology is combined with noise immune circuitry and novel encoding/decoding techniques to implement a cost-effective and reliable half bridge driver. A simple two chip set and minimal external components are used to drive both the high-side and low-side power MOSFET switches in bridge configurations. No external level shifting circuitry, transformers, or optocouplers are required. Applications include electronically commutated motors, electronic ballasts, and uninterruptible power supplies.

PWR-INT200 Features

The PWR-INT200 low-side driver (See Figure 1) contains the following functions:

- Schmidtt trigger logic inputs
- Logic and drive for the low-side MOSFET switch
- Proprietary differential, high-voltage level shift circuitry to send commands to the high-side driver
- Simultaneous conduction lockout circuit to prevent one driver from being turned on while the other driver is on
- Delay block to ensure that low-side and high-side driver outputs do not overlap unintentionally
- V_{DD} undervoltage lockout
- Linear regulator to bias the internal 5 volt logic

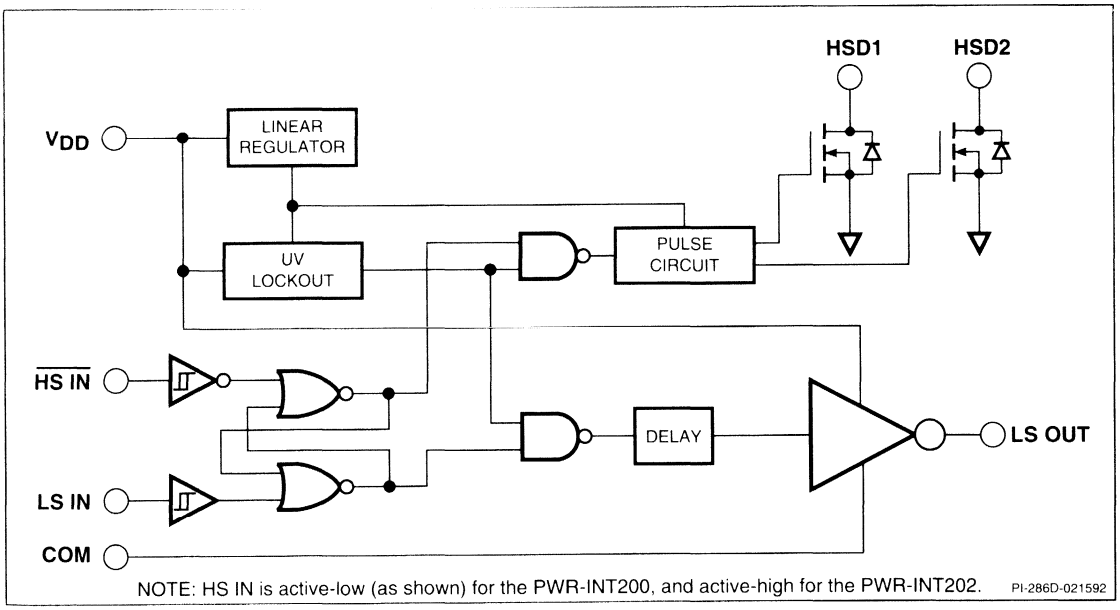

Figure 1. Functional Block Diagram of the PWR-INT200/PWR-INT202 Low-side Drivers.

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PWR-INT201 Features

The PWR-INT201 high-side driver (See Figure 2) controls the high-side or floating MOSFET switch and contains the following functions:

- Receiver to interface with the HSD1 and HSD2 outputs from the low-side driver
- Discriminator to extract the signal commands
- Logic and drive for the high-side MOSFET switch
- Delay block to ensure that low-side and high-side driver outputs do not overlap unintentionally
- V_{DDH} undervoltage lockout
- Linear regulator to bias the internal 5 volt logic

The PWR-INT201 is always used with either the PWR-INT200 or PWR-INT202 low-side driver.

A three phase brushless DC motor example is shown in Figure 3 to illustrate the use of the PWR-INT200/201. The LS IN signal directly controls MOSFET Q1. The $\overline{\text{HS IN}}$ signal causes the low-side driver to send command signals to the high-side driver which then turns Q2 on or off as required. The PWR-INT200 low-side driver will ignore input signals that command both Q1 and Q2 to conduct at the same time since that would effectively short the HV+ bus to the HV- bus. Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations are controlled by resistors R1 and R2. The body diodes associated with Q1 and Q2 conduct winding current during the inductive kick that occurs immediately after either Q1 or Q2 are turned off.

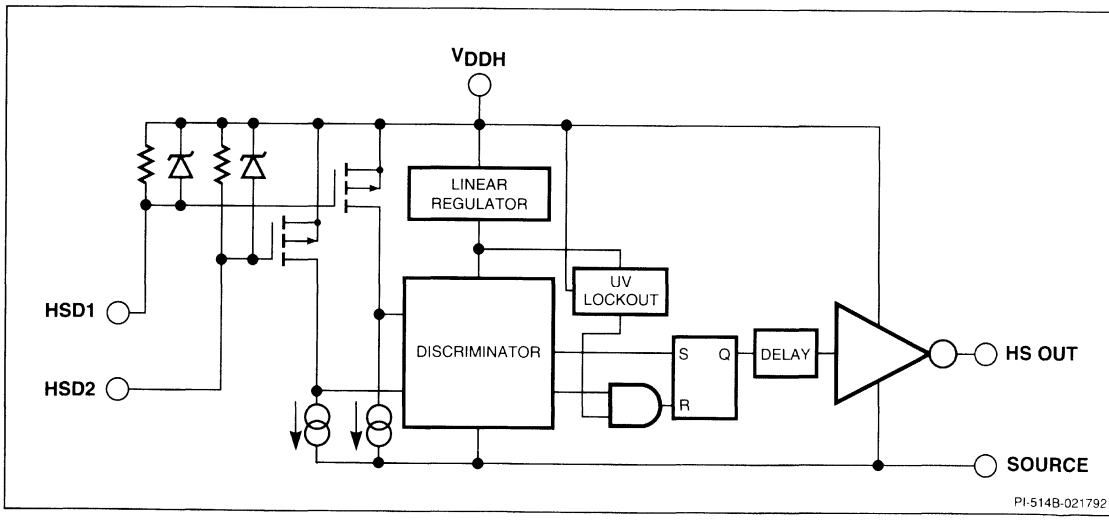


Figure 2. Functional Block Diagram of the PWR-INT201 High-side Driver.

PWR-INT202 Features

The PWR-INT202 low-side driver is used with the PWR-INT201 high-side driver to drive loads which require a high-side current sourcing switch with a low-side current sinking switch. The only differences between the PWR-INT202 and PWR-INT200 low-side drivers are the absence of the simultaneous lockout circuit, and the polarity of the HS IN pin.

The switched reluctance motor example shown in Figure 4 illustrates an application requiring both power MOSFET switches to be conducting at the same time. Diodes D2 and D3 conduct winding current during the inductive kick that occurs immediately after Q1 and Q2 are turned off.

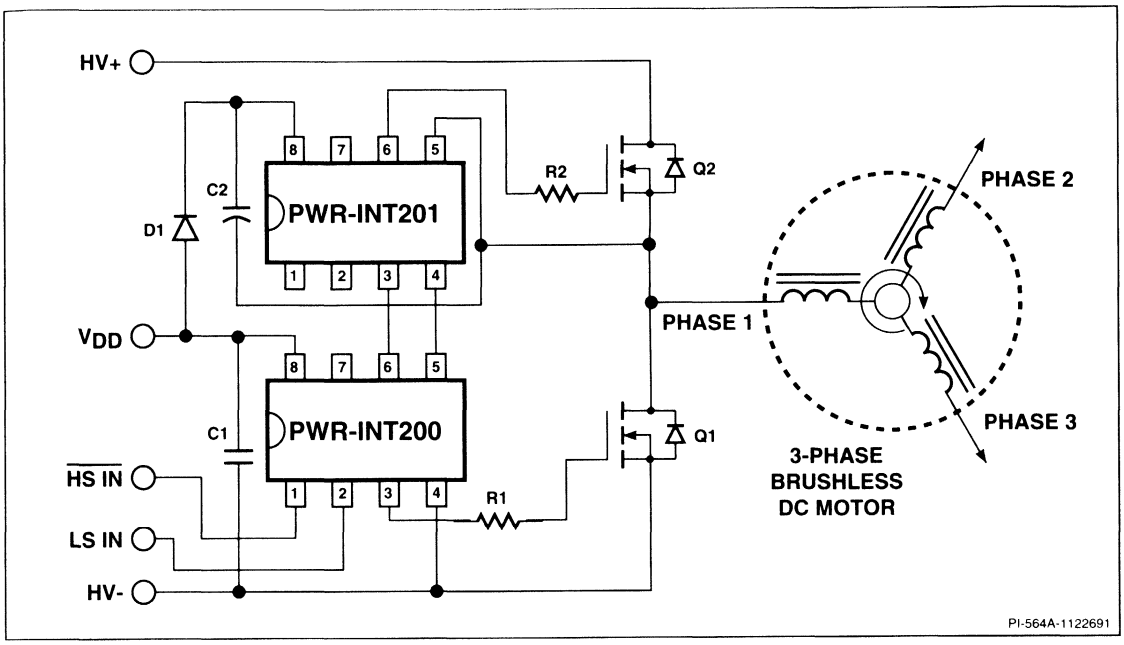


Figure 3. Using the PWR-INT200 and PWR-INT201 to Drive a 3-phase Brushless DC Motor.

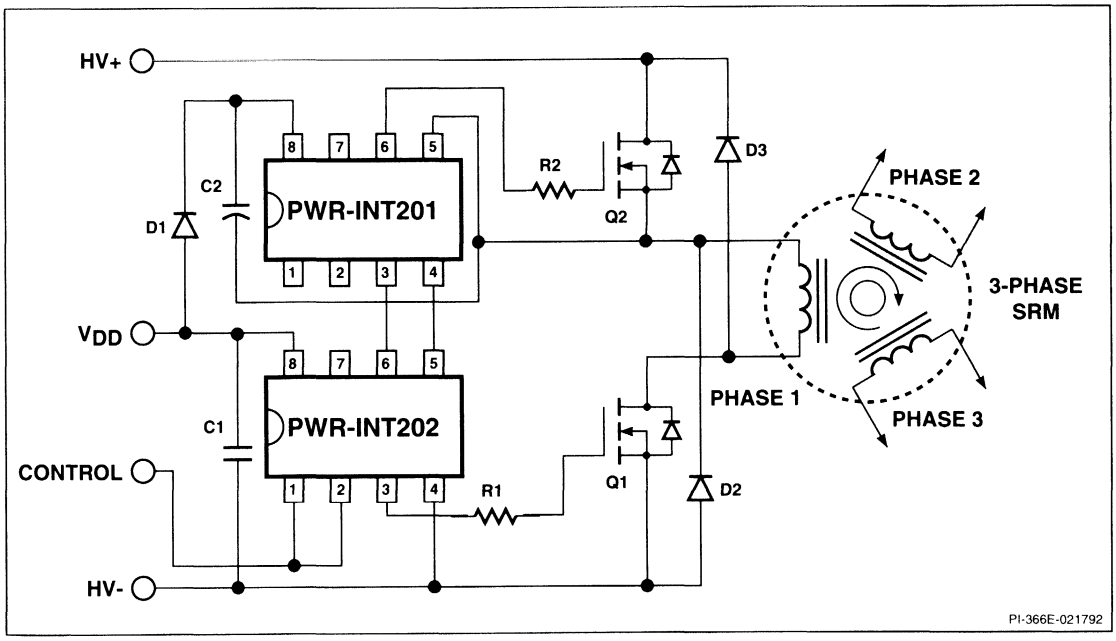


Figure 4. Using the PWR-INT202 and PWR-INT201 to Drive a 3-phase Switched Reluctance Motor.

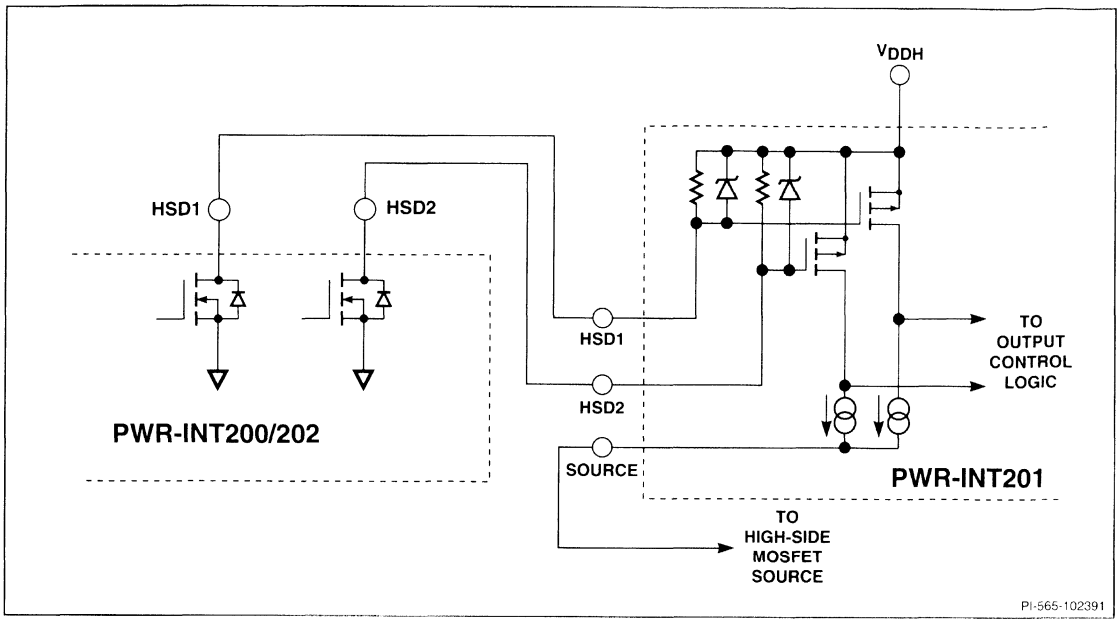


Figure 5. Key Components in the Low-side to High-side Interface.

General Circuit Operation

In Figures 3 and 4, low-side MOSFET switch Q1 will follow the level of the LS IN logic signal. High-side MOSFET switch Q2 will latch on and off with the edge of the $\overline{\text{HS IN}}$ (PWR-INT200) or HS IN (PWR-INT202) logic signals. The latch is required in the high-side driver because of pulsed communication over the high-voltage level shifting circuitry.

Low-side to High-side Interface

The PWR-INT200 and PWR-INT202 communicate with the PWR-INT201 using MOSFET level shifting transistor switches as shown in Figure 5. These MOSFET switches carry either a 600 or 800 Volt breakdown voltage rating for reliable operation from rectified sources as high as 277 VAC.

The level shifting transistors drive a minimum current pulse of 6 mA (typically 25 mA) for 75 ns. Two pulses are sent via HSD1 to turn on the high-side driver while one pulse is sent over HSD2 to turn the high-side driver off. Current in HSD1 and HSD2 is limited by the saturation characteristic of the MOSFET transistors. Drain voltage is typically within 5 volts of the bootstrap supply floating with the source of the high-side MOSFET switch.

Drive Capability

The driver outputs have been designed to drive capacitive loads such as the gates of N-channel power MOSFETs. The HS OUT and LS OUT drivers can source 150 mA and sink 300 mA of short-circuit current. When turned on, the outputs will pull the MOSFET gate up to the supply (V_{DD} or V_{DDH}), which can be as high as 15 V.

Simultaneous Conduction Lockout

The PWR-INT200/201 chip set has uses a latch to prevent both low-side and high-side MOSFET switches from being on at the same time. The turn on of the low-side is inhibited until the positive edge of the high-side control signal $\overline{\text{HS IN}}$ has occurred. The turn on of the high-side is inhibited until the negative edge of the low-side control signal LS IN has occurred.

Figure 6 shows a test circuit with LS IN connected to $\overline{\text{HS IN}}$. In this configuration the rising edge (on) of each driver output will never occur prior to the falling edge (off) of the other output. The asymmetric current drive (2:1 ratio of turn-off current to turn-on current) also helps prevent simultaneous conduction by turning each MOSFET off faster than it turns on. It should be noted that delays caused by external networks between the driver and MOSFET may impose additional constraints on the timing of the logic inputs. Both high-side and low-side delays should be kept as balanced as possible.

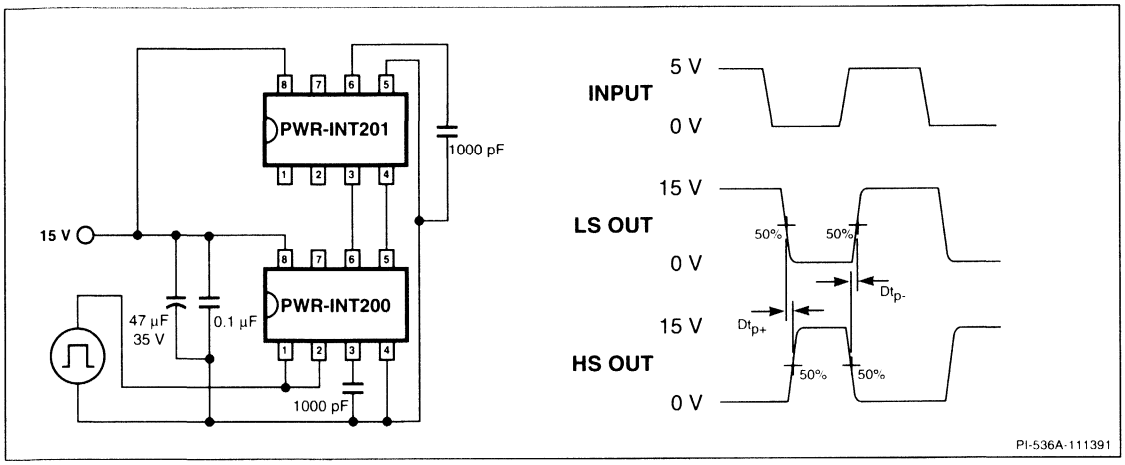


Figure 6. Dead Time Test Circuit.

Built-in Delays

Built-in delays ensure that the low-side and high-side driver outputs do not overlap unintentionally. Driver switching is delayed until pulsed current communication is completed, to minimize the effects of switching noise. The asymmetric delays in both the PWR-INT201 high-side driver and PWR-INT200 low-side driver ensure that both drivers are not on at the same time when both logic inputs are connected together.

A high level on LS IN and $\overline{\text{HS IN}}$ commands the low-side driver to turn on and the high-side driver to turn off. The low-side gate driver turns on following a programmed delay of 500 ns. This delay is greater than the propagation delay required to communicate to the high-side driver (200 ns typical). There is no additional programmed delay in the high-side driver. The high-side driver turns off before the low-side driver turns on.

A low level on LS IN and $\overline{\text{HS IN}}$ commands the low-side driver to turn off and the high-side driver to turn on. The low-side driver turns off following a programmed delay of 400 ns. The high-side driver is turned on following the propagation delay required for communication (400 ns typical) and an additional programmed delay of 300 ns. The low-side driver turns off before the high-side driver turns on.

Bootstrap Bias Circuit

Powering the PWR-INT201 high-side driver requires only a diode and capacitor as shown in Figures 3 and 4. When the low-side external MOSFET switch is on, D1 becomes forward biased, charging the capacitor to V_{DD}. When the high-side driver is turned on the diode is reverse biased and the capacitor provides bias power.

Bootstrap capacitor C2 must deliver sufficient gate charge to turn on external MOSFET Q2 and provide PWR-INT201 bias current over the expected time interval with minimal voltage decay or sag. The amount of total charge (ΔQ) delivered for a change in capacitor voltage (ΔV) is given by equation 1. The amount of charge Q_{DDH} associated with the biasing of the high-side driver is simply the product of bias current (I_{DDH}) and the on time $T_{HS(ON)}$ as shown in equation 2. MOSFET data sheet gate charge curves are used to estimate the required gate charge (Q_G). The total ΔQ is the sum of Q_G and Q_{DDH} as shown in equation 3. Equations 1-3 are combined and rearranged to solve for the minimum value of bootstrap capacitor C2 as shown in equation 4.

$$\Delta Q = C_2 \times \Delta V \quad (1)$$

$$Q_{DDH} = I_{DDH} \times T_{HS(ON)} \quad (2)$$

$$\Delta Q = Q_G + Q_{DDH} \quad (3)$$

$$C_2 = \frac{Q_G + Q_{DDH}}{\Delta V} \quad (4)$$

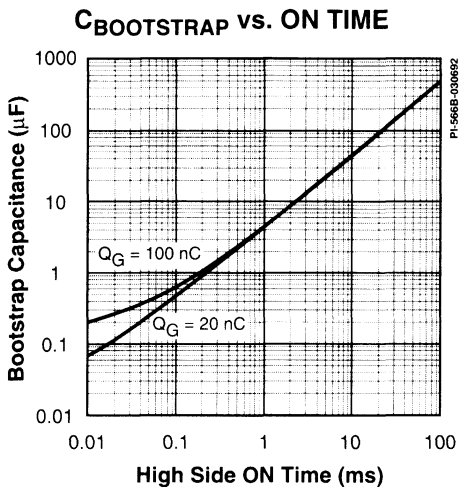


Figure 7.

C2 must be recharged through diode D1 from a low impedance voltage source. Most applications have a low impedance source available, but for some applications it may be necessary to select a bypass capacitor C1 large enough (typically a factor of 10 larger) to transfer sufficient charge to C2 without decay or sag.

V_{DD} Undervoltage Lockout

Undervoltage lockout sets the drive output to zero volts if there is not sufficient voltage to completely turn on the external power MOSFET. This prevents the power MOSFET switches from being partially turned on due to a fault or low line condition elsewhere in the system. The undervoltage lockout voltage is typically 9.25 V with hysterisis of 250 mV.

On the PWR-INT201 high-side driver undervoltage lockout will turn off the high-side MOSFET switch if the bootstrap capacitor discharges below the threshold voltage. This could happen during starting or low speed operation if the bootstrap capacitor is not large enough or charged frequently enough. The high-side driver will only turn on again if the bootstrap capacitor is properly charged and a new command to turn on from the low-side driver is received via HSD1.

Maximum Frequency Operation

The frequency of operation is limited by power dissipation within the low-side driver package and ambient temperature. Power dissipation within the package is the sum ofbias power and two frequency dependent effects: the power dissipated by the high voltage transistors communicating with the high-side driver, and the power associated with charging and discharging the gate of the external MOSFET switch.

Power dissipation due to communication with the high-side driver (P_{HSD}) is given by equation 5 where V_{IN} is the high voltage DC rail, I_{HSD} is the maximum current for the HSD output, $T_{HSD(ON)MAX}$ is the maximum pulse width, and f is the switching frequency. Note that three pulses are required each cycle.

$$P_{HSD} = 3 \times V_{IN} \times I_{HSD} \times T_{HSD(ON)MAX} \times f \qquad (5)$$

Power dissipation due to charging and discharging the gate of the external MOSFET switch (P_Q) is given by equation 6 where Q_G is the total gate charge required to drive the MOSFET to the final gate voltage V_{GS}.

$$P_Q = Q_G \times V_{GS} \times f \qquad (6)$$

Maximum allowed power dissipation (P) is given by equation 7 where T_j is the maximum allowable junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal impedance.

$$P = \frac{T_j - T_A}{\theta_{JA}} \qquad (7)$$

Rearranging these equations and solving for frequency produces equation 8. This equation is graphed in Figure 8 for T_j of 125°C, T_A of 25°C, θ_{JA} of 100°C/W (PDIP) and 120°C/W (SOIC), V_{GS} of 16.5 V, I_{HSD} of 30 mA, I_{DD} of 3 mA, and $T_{HSD(ON)MAX}$ of 156 ns.

$$f = \frac{P - (V_{DD} \times I_{DD})}{(3 \times V_{IN} \times I_{HSD} \times T_{HSD(ON)MAX}) + (Q_G \times V_{GS})} \qquad (8)$$

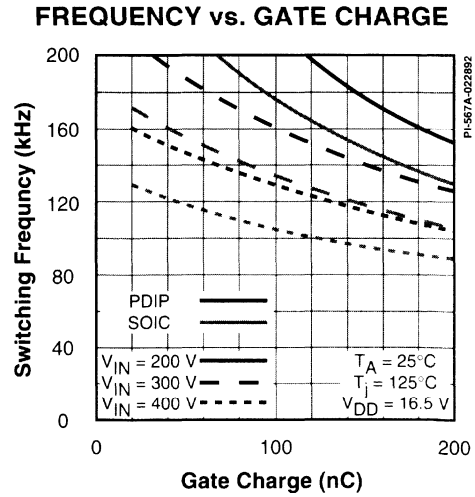


Figure 8.

Selecting Gate Drive Networks

Most applications will benefit from additional impedance inserted between the driver output and the gate of each external MOSFET. Selecting impedance magnitude and network topology requires an analysis of the input or Gate-to-Source and Miller or Gate-to-Drain capacitance of the external MOSFET. The actual current versus voltage characteristic of the driver must also be taken into account.

MOSFET Parasitic Capacitance

Capacitance and gate charge curves for a typical 500 V, 10 Ω power MOSFET switch are shown in Figure 9. MOSFET manufacturers typically measure the capacitance terms at 1 MHz with gate to source DC voltage at 0 V while the drain to source voltage is swept out to 40 or 50 V. The three basic capacitance terms for a power MOSFET are shown in Figure 10. It is not possible to determine the capacitance between any two terminals without compensating for the other two capacitive terms. Manufacturers measure the effective capacitance between the three pairs of terminals and assign the following descriptions:

Input Capacitance (C_{ISS})

$$C_{GS} + C_{GD} \text{ with } C_{DS} \text{ shorted} \qquad (9)$$

Output Capacitance (C_{OSS})

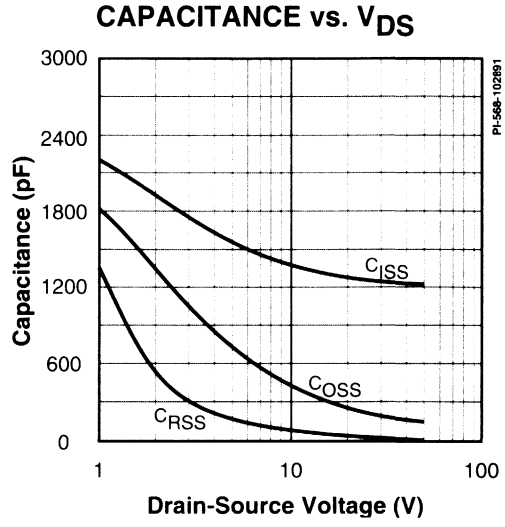
$$C_{DS} + \left(\frac{C_{GS} \times C_{GD}}{(C_{GS} + C_{GD})} \right) \qquad (10)$$

Reverse Transverse Capacitance (C_{RSS})

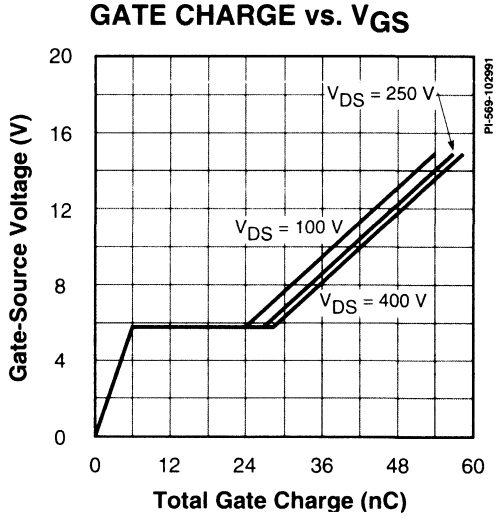
$$C_{GD} \qquad (11)$$

Note that the capacitance terms C_{ISS}, C_{RSS}, and C_{OSS} are nonlinear (their value changes with applied drain-to-source voltage). For analyzing MOSFET gate drive circuitry the gate charge curve is more useful. This curve is generated with the test circuit shown in Figure 11.

The performance of the gate charge test circuit in Figure 11 is interpreted in the following manner. A fixed gate drive current I_G is driven into the gate of the MOSFET. The gate voltage rises linearly due to the constant current charging of C_{ISS} up to the MOSFET threshold voltage (typically 5.5 V). The time taken to charge C_{ISS} to the threshold voltage is actually the turn on delay between the drive signal and when switching begins. As the MOSFET switches the gate current is diverted from C_{ISS} to charge the Miller capacitance C_{RSS}. The gate voltage stays flat as the drain voltage changes from the off value (100 - 400 V) to the on value (near 0 V). The time taken to charge C_{RSS} corresponds to the switching time of the MOSFET. After switching is completed, the input capacitance C_{ISS} is again charged linearly to the final gate voltage. The time taken to charge C_{ISS} from the threshold voltage to the final gate voltage



(a)



(a)

Figure 9.

corresponds to an overdrive delay after turn on. The time taken to discharge C_{ISS} from an initial voltage value equal to V_{DD} down to the threshold voltage corresponds to a turn off delay.

The effective C_{ISS} is proportional to the slope ($C_{ISS} = \Delta Q/\Delta V$) of these curves in the turn on delay and turn off delay regions. Note

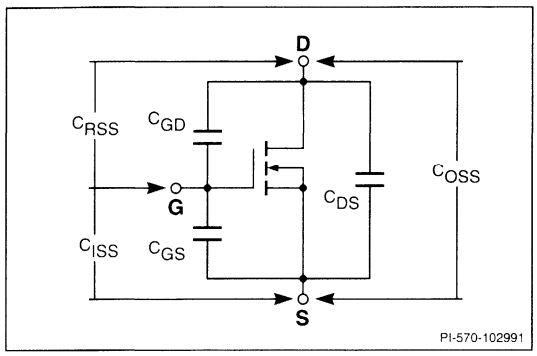


Figure 10. MOSFET Parasitic Capacitance Model.

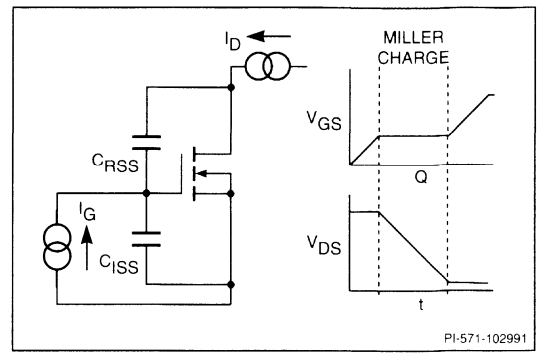


Figure 11. MOSFET Gate Turn-on Characteristic.

that the slope of the curves in the turn on delay region and turn off delay region are different, leading to two different values for C_{ISS}. In the following analysis the two values for C_{ISS} are described as C_{ISS1} for the turn on delay region, and C_{ISS2} for the turn off delay region. The reverse transfer capacitance will be denoted as C_{RSS1} below drain voltages of 50 V and will be taken from the data sheet with a V_{DS} of 0 volts. The reverse transfer capacitance at higher voltages will be denoted C_{RSS2}, and can be calculated from the incremental gate charge (ΔQ) required to charge from 100 to 400 V (ΔV). These capacitance terms are tabulated in Table 1 for a variety of 500 V MOSFETs.

PART #	IRF820	IRF830	IRF840	IRFP450	IRFP460
$R_{DS(ON)}$	3Ω	1.5Ω	0.85Ω	0.4Ω	0.27Ω
C_{ISS1}	363	550	1090	2400	3333
C_{ISS2}	944	1474	3156	6200	11,110
C_{RSS1}	360	675	1350	3400	6000
C_{RSS2}	6.7	8.3	13.3	20	33

Table 1. Typical MOSFET Capacitance Values.

Driver Current/Voltage Characteristic

The CMOS gate driver has an output current capability that depends on the output voltage as shown in Figure 12. This characteristic has been simplified into two regions: a linear region represented by the driver output impedance, and a constant region determined by the saturation characteristic of the CMOS driver output. The slopes of the curves represent output impedances of 50 Ω for turn on and 25 Ω for turn off.

During turn on the drive voltage must transition from 0 V through the MOSFET threshold voltage region (2 to 5 volts) to the final value of 10-15 V. Note that in the vicinity of the threshold voltage, the source current is limited by the constant or saturation region of the driver. Turn on and slew rate analysis will be slightly different depending on the value of the external impedance. A current source model should be used for external impedances of less than 50 Ω. A simple resistive model should be used for impedances of 50 Ω or greater.

During turn off, the drive voltage must transition from 10-15 V back down through the MOSFET threshold voltage region to the final value of 0 V. Note that in the vicinity of the threshold voltage, the sink current is limited by the output impedance or linear region of the driver. The simple resistive model can be used for turn off (including slew rate) for all values of external gate resistance.

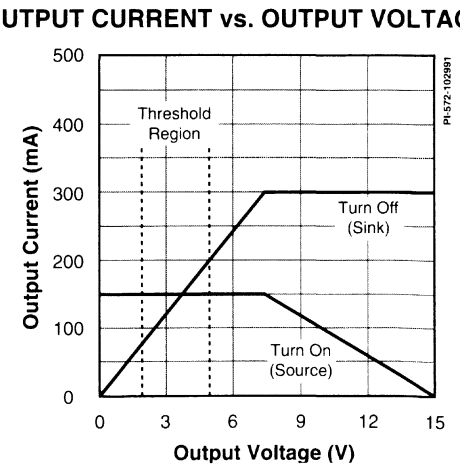


Figure 12.

Resistive Gate Drive Network

Current Source Model for Turn-on Delay

For external impedances of less than 50 Ω, the turn on delay is determined by the rate at which the current source can charge the input capacitance C_{ISS1} of the MOSFET, as shown in equation 12. This equation is plotted in Figure 13 for various MOSFET switches with $V_{GS(th)}$ of 5.5 V and I_{SOURCE} of 150 mA.

$$t_{d(on)} = \frac{C_{ISS1} \times V_{GS(th)}}{I_{SOURCE}} \qquad (12)$$

Effect on Turn-on and Turn-off Delays

The resistance between the driver output and MOSFET gate combined with C_{ISS1} creates a simple RC circuit. The effective resistance is the sum of the output impedance R_O of the driver and external gate resistor R_G. During turn on, the delay time $t_{d(on)}$ required to charge C_{ISS1} from 0 to $V_{GS(th)}$ is given in equation 13. This equation is plotted in Figure 14 for various gate resistors and MOSFET switches with R_O of 50 Ω, V_{DD} of 15 V, and $V_{GS(th)}$ of 5.5 V.

$$t_{d(on)} = -(R_O + R_G) \times C_{ISS1} \times \ln\left(1 - \left(\frac{V_{GS(th)}}{V_{DD}}\right)\right) \qquad (13)$$

During turn off, the time delay $t_{d(off)}$ required to discharge C_{ISS2} from the initial value (V_{DD}) down to $V_{GS(th)}$ can be calculated using equation 14. This equation is plotted in Figure 15 for various gate resistors and MOSFET switches with R_O of 25 Ω, V_{DD} of 15 V, and $V_{GS(th)}$ of 5.5 V.

$$t_{d(off)} = -(R_O + R_G) \times C_{ISS2} \times \ln\left(\frac{V_{GS(th)}}{V_{DD}}\right) \qquad (14)$$

Two different effects each tend to make $t_{d(off)}$ longer than $t_{d(on)}$. First, the MOSFET threshold voltage is typically one third the gate drive voltage V_{DD} (i.e., 5.5 V $V_{GS(th)}$, 15 V V_{DD}), which takes less time to charge up from 0 than to discharge down from V_{DD}. Second, C_{ISS1} is significantly smaller than C_{ISS2}. To counteract these two effects, the driver outputs have been designed with an asymmetric output impedance so that $R_{O(on)}$ is twice the resistance of $R_{O(off)}$.

It should be noted that the series gate resistor will reduce the benefits of the asymmetric output impedance. A method to avoid this problem will be given later.

Effect on Slew Rate

During the MOSFET switching transition, the gate drive current discharges the reverse transfer, or Miller capacitance, C_{RSS} as shown in Figure 16. The voltage at the gate remains constant, meaning that no current goes toward discharging C_{ISS}. The voltage across the effective gate resistance is also constant, defining the gate current I_G as shown in equation 15. The slew rate $\Delta V_{DS}/\Delta t$ for the drain voltage is given by equation 16 and

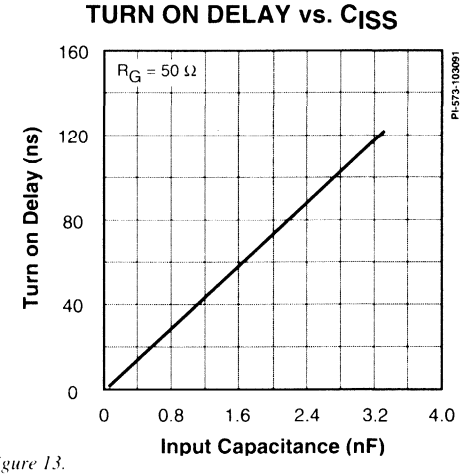


Figure 13.

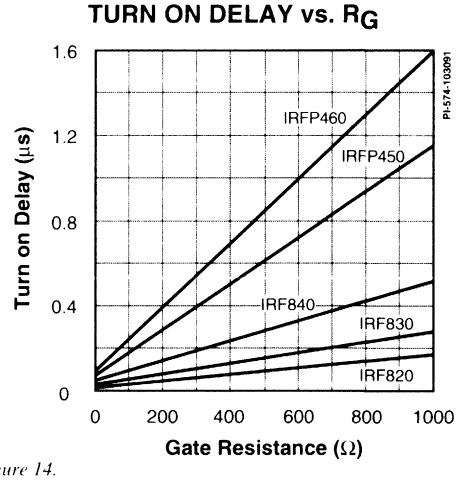


Figure 14.

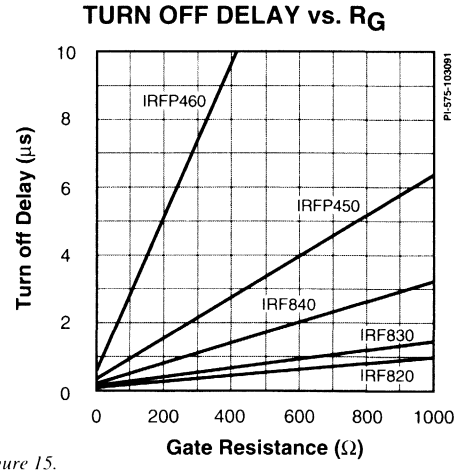


Figure 15.

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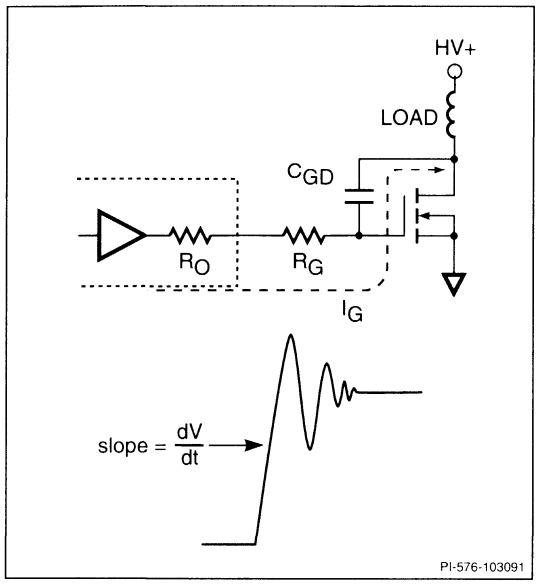

Figure 16. Charging the Miller Capacitance.

can be controlled by the resistor value selected for R_G (for resistors of 50 Ω or greater). Equation 15 is plotted in Figure 17 for various resistors (50 Ω and above) and MOSFETs with R_O of 50 Ω and V_{DD} of 15 V. For turn on slew rate with external impedance of less than 50 Ω, equation 16 is plotted in Figure 18 for various MOSFETs with I_G of 150 mA.

$$I_G = \frac{V_{DD}}{(R_O + R_G)} \quad (15)$$

$$\frac{\Delta V_{DS}}{\Delta t} = \frac{I_G}{C_{RSS2}} \quad (16)$$

Actual slew rates may be lower due to load parasitic capacitance connected to the drain or source of the external MOSFET.

Ringing Waveform Considerations

Ringing can occur on the high voltage AC waveform due to parasitic inductance L_{STRAY} and capacitance C_{STRAY} terms as shown in Figure 19. Waveforms with peak voltages of 100 V and ringing frequencies of 1 MHz are not uncommon. Higher slew rates tend to cause higher peak voltages in the ringing waveform. This AC waveform can couple back through MOSFET capacitors directly into the output of the driver, which may cause voltage excursions above V_{DD} and below COM in excess of recommended specifications. This circuit can be reduced to a Thevinin equivalent circuit shown in Figure 19 by recognizing that C_{RSS} and C_{ISS} form a capacitive divider. The magnitude of the ringing current I_r flowing through the output impedance R_O, given by equation 17, where V_{pk} is the peak of the ringing voltage and f_r is the ringing frequency. This

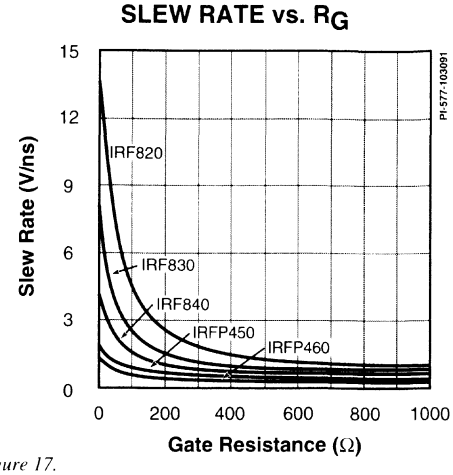

Figure 17.

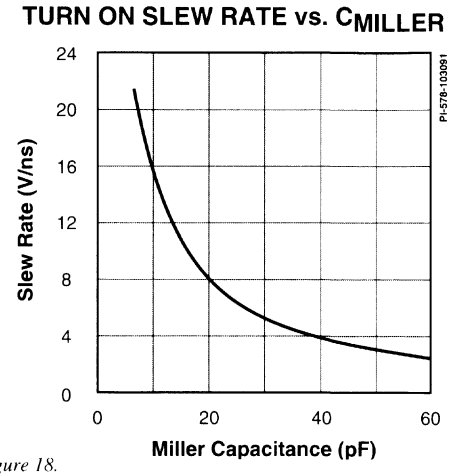

Figure 18.

calculation should be performed at both the turn on and turn off transition to verify that the gate drive output voltage does not exceed either the maximum or minimum voltage rating. Note that with the MOSFET off, C_{ISS1} and C_{RSS2} should be used, and when the MOSFET is on, C_{ISS2} and C_{RSS1} should be used. The current flowing through R_O generates a voltage V_r as shown in equation 18. R_O is typically 50 Ω when the driver is on and 25 Ω when the driver is off. The voltage across R_O must be kept below 300 mV and can be controlled by the value of R_G.

$$I_r = V_{pk} \times \frac{\frac{C_{RSSY}}{(C_{ISSX} + C_{RSSY})}}{\sqrt{(R_O + R_G)^2 + \left(\frac{1}{2\pi \times f_r \times C_{ISSX}}\right)^2}} \quad (17)$$

$$V_r = I_r \times R_O \quad (18)$$

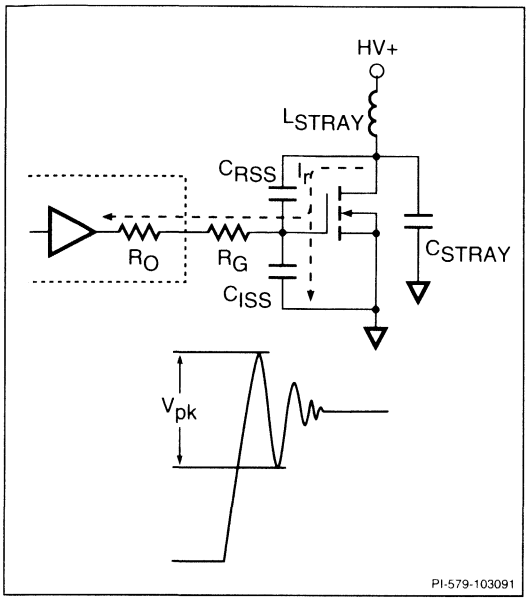

Figure 19. Ringing Caused by Parasitic Elements.

Example: During turn off transition for a low-side switch with a peak ringing voltage of 100 V, ringing frequency of 1 MHz, C_{ISS1} of 1090 pF, C_{RSS2} of 13.3 pF, output impedance of 25 Ω, and series resistance of 470 Ω, the effective ringing current will be 5.7 mA. The effective voltage across the driver output impedance is 58.4 mV.

Asymetric Gate Drive and Diode Clamping

It may be necessary to turn the MOSFET on with one series gate impedance and turn it off with a lower gate impedance to guarantee that no shoot-through occurs during transitions. The network shown in Figure 20 charges the two MOSFET switches through gate resistors R1 and R2, while discharging through the parallel combinations of R1||R3 and R2||R4. Diodes D6 and D9 block during turn on and conduct during turn off. This approach allows complete control of the slew rate and delays associated with turning the MOSFET switches on and off.

Under some conditions the gate resistance required to reduce the peak ringing current I_r may not produce a high enough slew rate. Schottky clamp diodes D4, D5, D7, and D8 can be added to prevent ringing-induced excursions of the driver output, while maintaining low enough gate resistance for high slew rates.

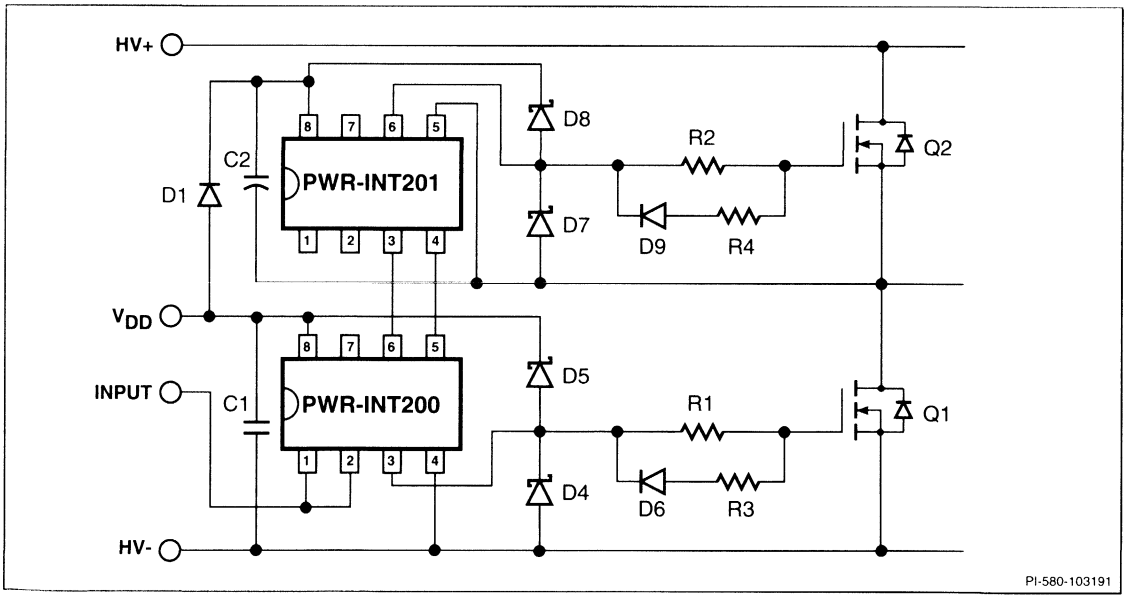

Figure 20. Asymmetric Gate Drive Circuit with Schottky Clamps for Output Noise Protection.

MOSFET Switch Timing Issues

External Gate Drive Delays

The PWR-INT200/201 simultaneous conduction lockout feature has been designed to prevent both drivers from being on at the same time. Nonetheless, circuit delays external to the PWR-INT200/201 may allow both external MOSFET switches to be on at the same time. If $t_{d(on)}$ is smaller than $t_{d(off)}$, a delay must be programmed at the logic inputs to ensure that both MOSFET switches will not be on at the same time. Dead time required by the application can also be included in this programmed delay. The minimum programmed delay t_p to be applied to the logic inputs is simply the difference between $t_{d(off)}$ and $t_{d(on)}$, added to any additional system dead time t_{dt} as shown in equation 19. If $t_{d(on)}$ is greater than $t_{d(off)}$, the programmed delay should be equal to the dead time t_{dt} as shown in equation 20.

$$t_p = t_{dt} + (t_{d(off)} - t_{d(on)}) : \; t_{d(off)} > t_{d(on)} \qquad (19)$$

$$t_p = t_{dt} : t_{d(off)} \leq t_{d(on)} \qquad (20)$$

The relationship of these signals is shown in Figure 21. Note that the rising edge of LS IN is delayed by the time t_p from the rising edge of $\overline{\text{HS IN}}$, while the falling edge of $\overline{\text{HS IN}}$ is delayed by time t_p from the falling edge of LS IN.

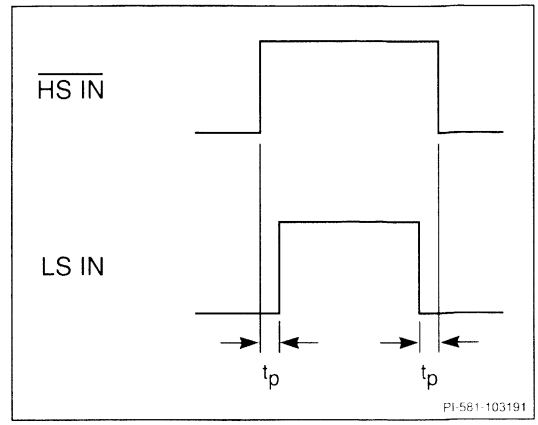

Figure 21. Programmed Delay Time for PWR-INT200/201.

Ensuring Proper Bootstrap Operation

In some bridge applications, the high-side MOSFET switch must be on for long intervals. One example is a bridge driven DC motor where the high-side switch may be turned on or off only when motor direction is changed. Another example is the self commutated brushless DC motor where the on-times of each switch depend on motor speed during start and low speed operation. In these applications, a simple bootstrap capacitor may be too large to be practical. Other techniques must be considered.

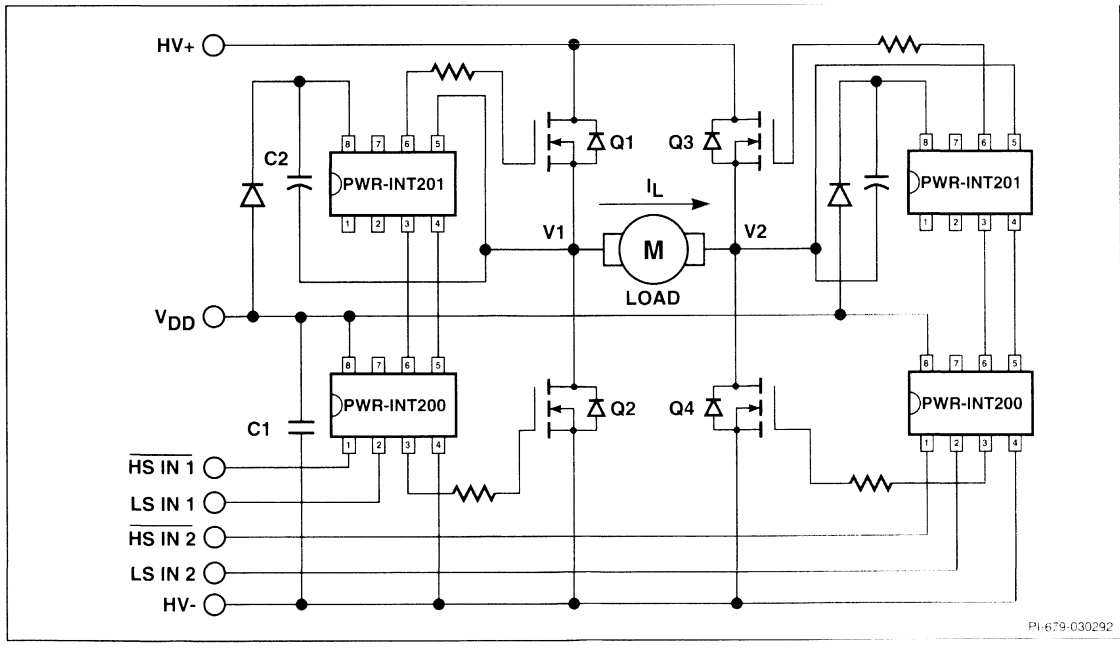

Figure 22. Full Bridge Motor Drive Circuit.

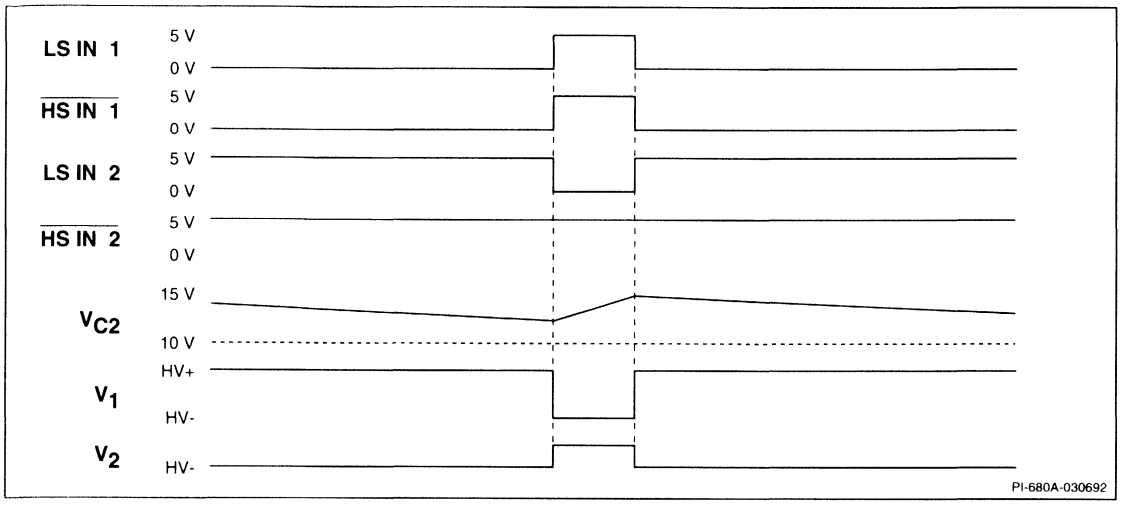

Figure 23. Timing Diagram for Charging the Bootstap Capacitor in an H-Bridge Configuration.

One possibility is to modulate the switches with a short pulse sufficient to charge the bootstrap capacitor during starting and low speed operation. A bridge driven DC motor is shown in Figure 22 and the logic signals are given in Figure 23. Assuming that Q1 and Q4 are turned on while Q2 and Q3 are turned off, bootstrap capacitor C2 discharges during the long time interval. Q1 and Q4 can be turned off for a short interval while Q2 is turned on to charge C2. When C2 is charged, Q2 is turned off while Q1 and Q4 are turned back on. This technique can also be adapted to three phase brushless DC motors. The short bootstrap charging interval should not effect motor operation significantly due to the inertia of the rotor. Note that motor back EMF voltage will appear at the free node (V2) while C2 is being charged.

Various charge pump circuits are possible which use AC waveforms to charge the bootstrap capacitor. These circuits are application specific and can generate excessive current spikes during commutation if care is not taken.

Another alternative is to add transformer windings to an existing supply to create floating voltage sources for each of the high-side drivers. The circuit shown in Figure 25 uses a Power Integrations PWR-SMP210 to create a 15 V power supply for the controller and low-side drivers as well as three floating sources for the high-side drivers. This circuit can supply up to 5 W from a rectified universal input (85 to 265 VAC).

In PWR-INT201/202 applications (such as switched reluctance motor drives) both switches are turned on at the same time and turned off at the same time. The voltage across the load reverses due to inductive energy storage, causing the source of the high-side MOSFET to go below ground. This voltage reversal also

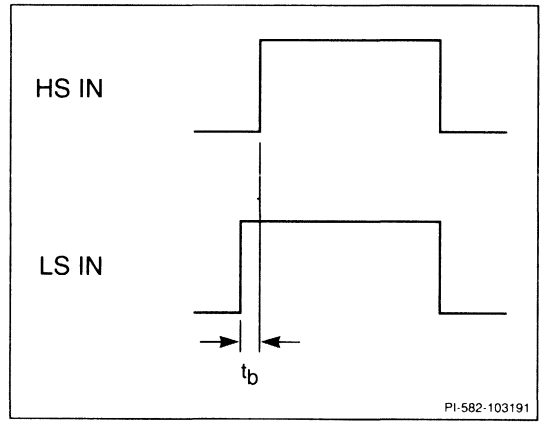

Figure 24. Bootstrap Charging Time for PWR-INT202/201.

serves to recharge the bootstrap capacitor. However, during the first few cycles of operation there is no inductive kick, and the bootstrap capacitor may not properly charge. The solution is to turn on the low-side MOSFET slightly before the high-side MOSFET each cycle for an amount of time t_b sufficient to charge the bootstrap capacitor as shown in of Figure 24.

In some cases the inductive energy storage in the load may be too low to cause the voltage reversal necessary to charge the bootstrap capacitor. An external transistor circuit can be added to ensure that the bootstrap capacitor is properly charged as shown in Figure 27. Q4 turns on when Q1 turns off to pull the source of Q2 to ground, which effectively charges bootstrap capacitor C2.

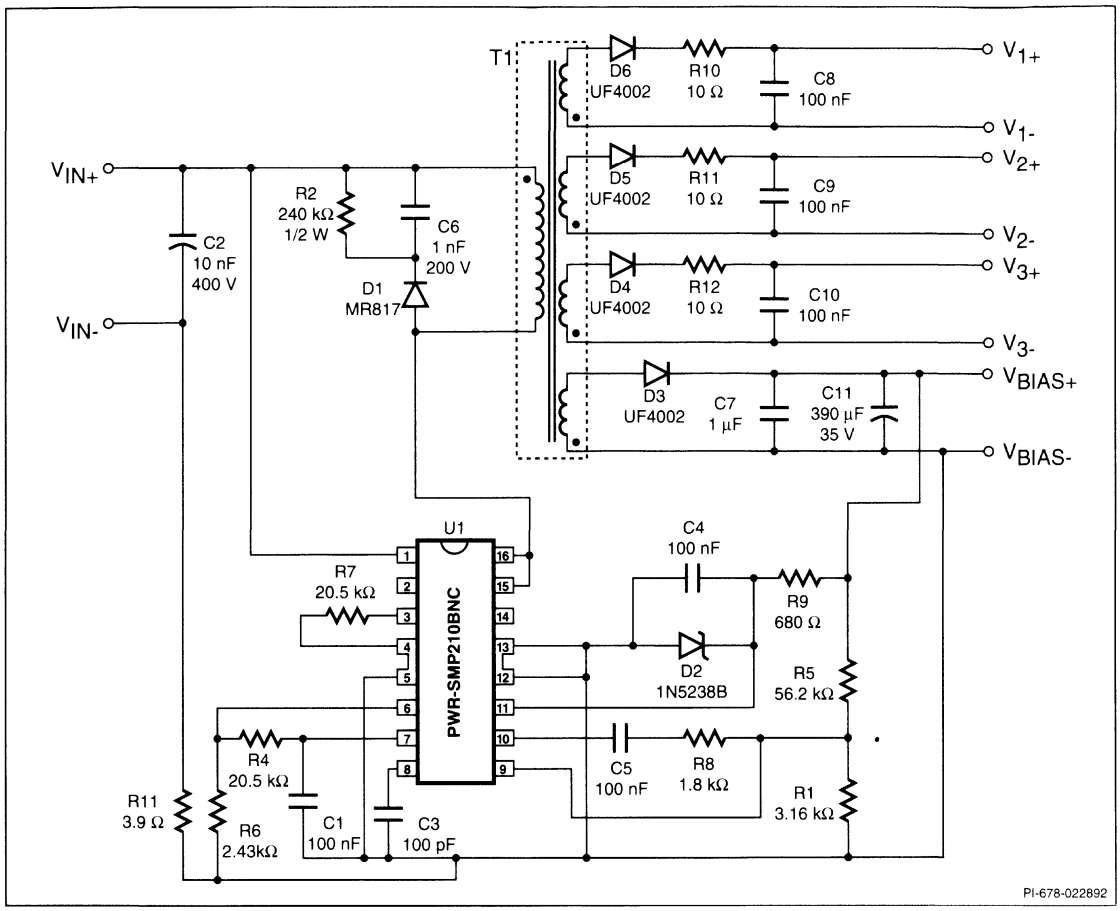

Figure 25. Using the PWR-SMP210 to Bias a 3-phase Drive Circuit.

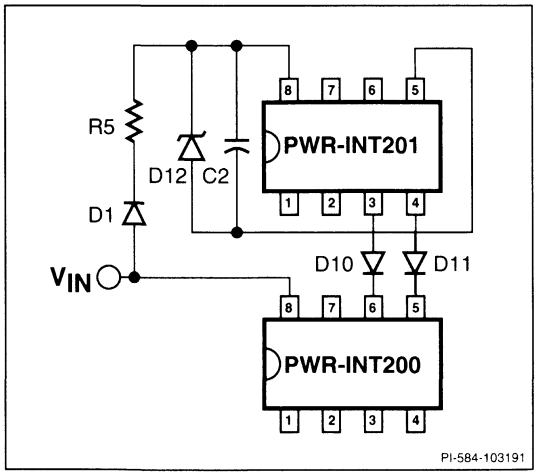

Figure 26. Protection of HSD1 and HSD 2 from Inductive Spikes.

Parasitic Series Inductance

In some applications parasitic inductance and fast changing currents will cause the source of the high-side MOSFET to dip significantly below ground for a short amount of time. If the magnitude of this voltage is greater than V_{DD}, the two high voltage channels HSD1 and HSD2 may be pulled below ground and V_{DDH} may charge up to a voltage greater than 16 V (both in excess of absolute maximum ratings). HSD1 and HSD2 can be protected by series diodes D10 and D11, as shown in Figure 26. Also shown are resistor R5 and Zener diode D12. Resistor R5 is selected to produce a time constant that is long when compared with the width of the negative going voltage spike, but short compared to t_{on} of the low-side MOSFET as shown in equation 21. For longer spike times or shorter MOSFET on times, zener diode D12 can be added across capacitor C2 to clip the spike.

$$t_{spike} \times 5 < R5 \times C2 < \frac{t_{on}}{5} \qquad (21)$$

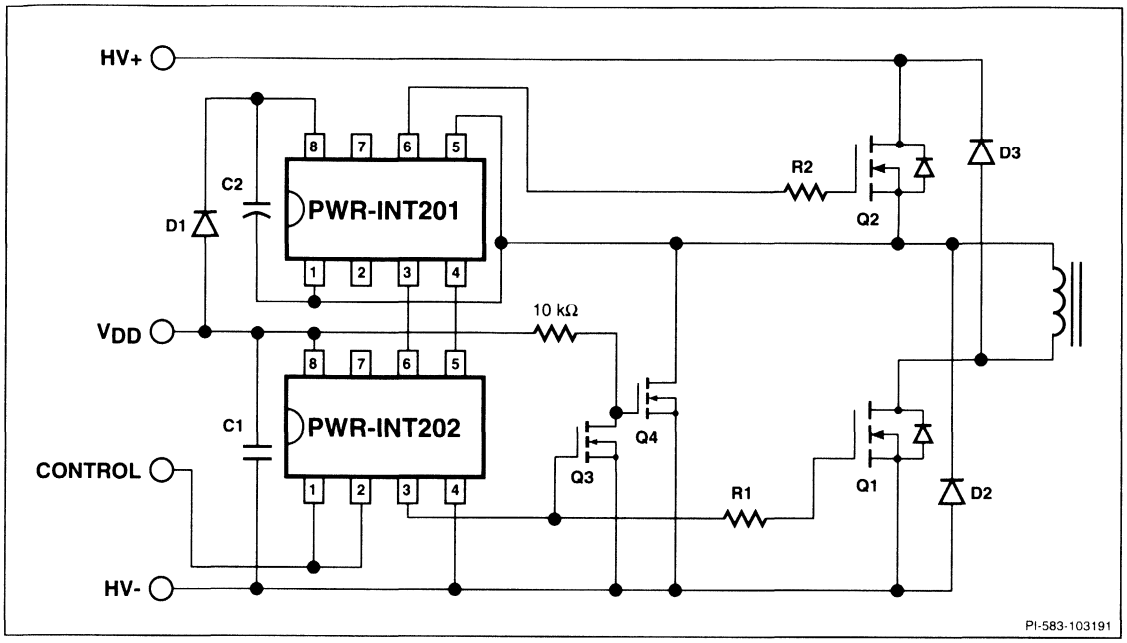

Figure 27. Bootstrap Charging Circuit.

Input Signal Conditioning

Two networks are shown in Figure 28 for conditioning the input signal. Both feature local shunt capacitors to counteract the effect of current flowing through the system ground impedance. The series resistor circuit can be used to filter logic inputs that actively drive the signal both high and low. The pullup resistor circuit is used with open drain or collector logic outputs, or when a signal must be terminated to reduce reflections and ringing.

Power Sequencing

It is important that the V_{DD} supply always exceeds the logic voltage on either LS IN or HS IN to eliminate the possibility of latch-up on power up. Ideally, the V_{DD} supply should be allowed to reach its full voltage before any logic signals are applied.

The diode pullup and blocking network shown in Figure 29 can be used to ensure proper operation if the recommended power sequencing is not possible. D13 and D14 ensure that the input voltage never exceeds V_{DD} by more than one diode drop, while D12 blocks current flow back to the V_{DD} supply.

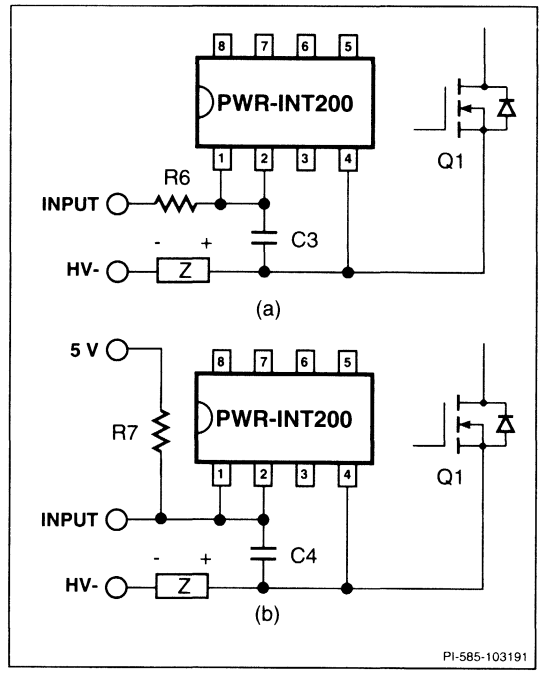

Figure 28. Input for (a) Active Drive, and (b) Open Collector Drive.

Layout

Creepage Distance Constraints

Creepage distance is the shortest path between two conductors measured along the surface of the PC board. Creepage distance must be maintained between all conductors carrying high voltage and those carrying low voltage. Typical creepage distances are 1.5 mm for 110 VAC, 2.5 mm for 250 VAC, and 3.2 mm for 277 VAC applications. Individual requirements vary with the application (i.e. business equipment, factory automation, etc.). Figure 30 shows the high voltage boundaries of a typical circuit with high voltage traces highlighted. The circuit group within the indicated boundary is not subject to creepage constraints since the relative voltage is low. However, creepage distance must be maintained between this circuit group and all other high- and low-voltage circuitry.

HSD1, HSD2 Circuit Routing

HSD1 and HSD2 are high voltage signals even though the relative voltage between the two level shifting channels is actually quite low (less than 5 V). The two channels should be connected using parallel "mirror image" PC traces with minimal spacing (10 to 20 mils) to increase common mode rejection and reduce the effects of switching noise. Proper creepage distances must be maintained between these traces and the rest of the circuitry.

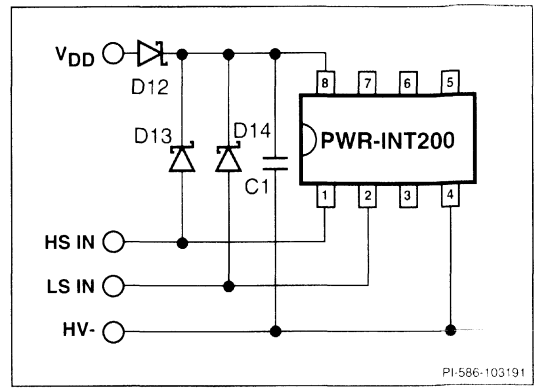

Figure 29. Logic Input Protection Components.

Gate Source Circuit Routing

The COM connection of the PWR-INT200/202 low-side drivers should be connected directly to the source of the low-side MOSFET switch, while the SOURCE connection of the PWR-INT201 high-side driver should be connected directly to the source of the high-side MOSFET switch, as shown in Figure 31. Gate trace runs should be kept as short as practical.

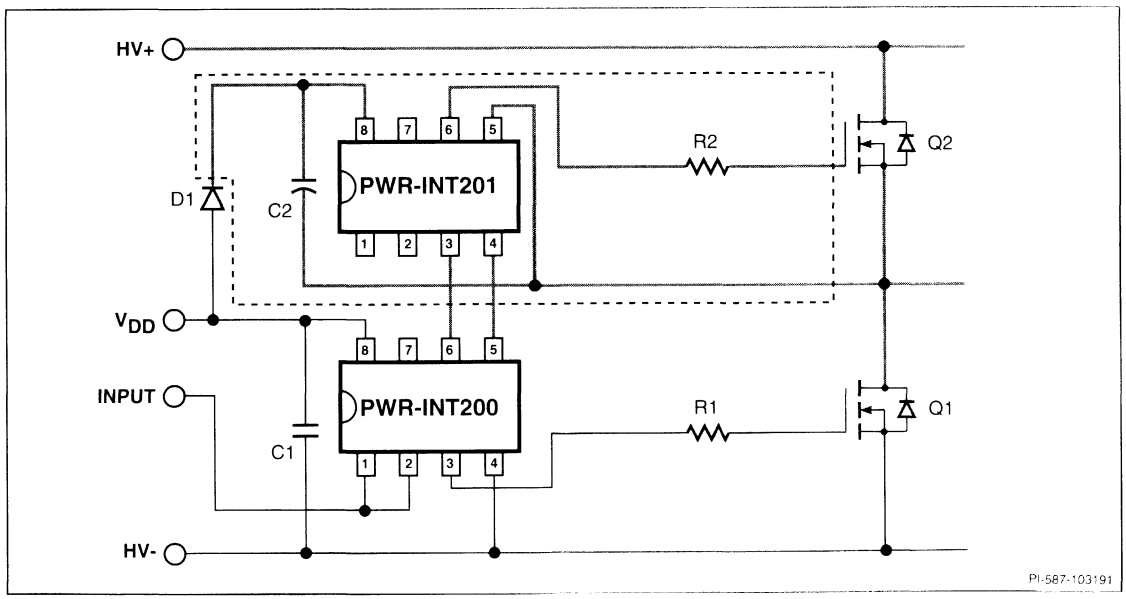

Figure 30. High-voltage Traces Requiring Creepage Separation from the Low-voltage Portions of the Circuit.

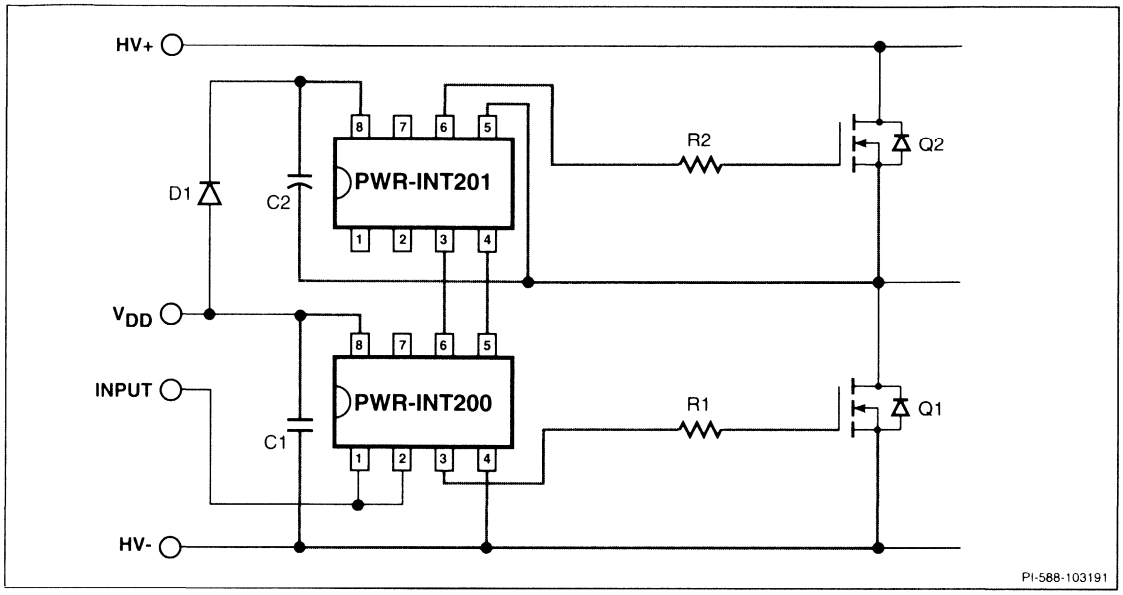

Figure 31. Traces Requiring Attention to Minimizing Loop Area and Trace Length.

Grounding

The sources of all low-side MOSFET switches should be tied together at a common node and a separate trace should run back to the return of the high voltage source as shown in Figure 32. The high voltage source should be bypassed locally with a capacitor to this common node. Logic return should be connected to the common node. This will keep logic currents away from MOSFET currents, which minimizes noise related problems. Ground planes are not necessary in all applications. If used, the ground plane should be shaped like an "hourglass" with a "noisy" half and a "quiet" half as shown.

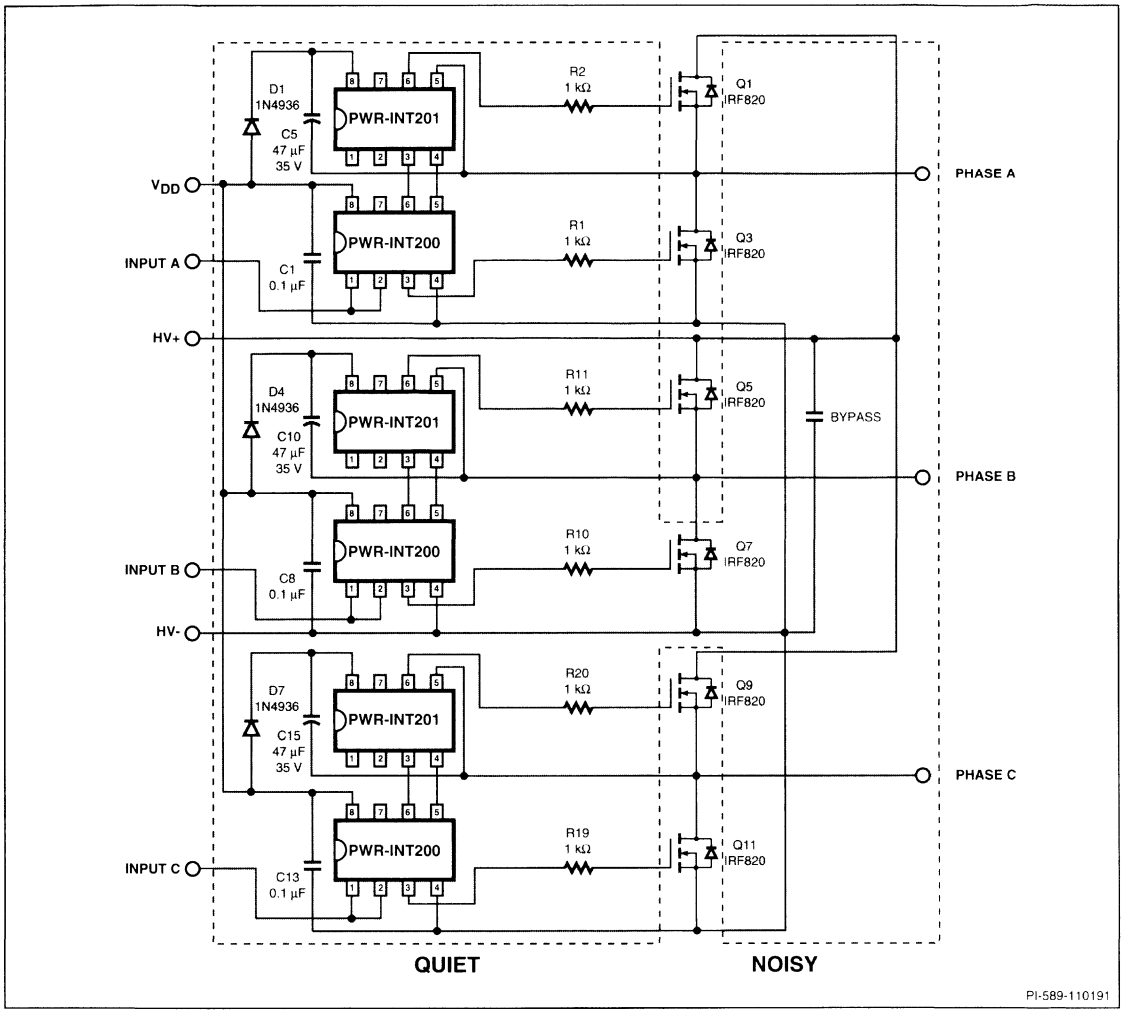

Figure 32. Grounding and Ground Plane Division.

Function and Application of the PWR-SMP240/260

APPLICATION NOTE AN-11

The power supply industry continues to push for higher power densities. As a result, the power components industry is responding in many ways. Passive components are adapting to the requirements of higher frequency and higher efficiency designs. Active component manufacturers are responding by producing parts with higher levels of integration to support these designs. A prime example of this is the PWR-SMP240 and PWR-SMP260, two off-line current-mode PWM regulators designed to deliver up to 60 W of power in a very small, efficient package.

The PWR-SMP260 combines a 700 V, 3 Ω MOSFET, a fully-featured fixed frequency current-mode controller, and an extended set of sophisticated power management circuitry to supervise the operation of the power supply. The PWR-SMP240 combines a 700 V, 5 Ω MOSFET with the same controller for lower power applications. All following references to the PWR-SMP260 will apply to the PWR-SMP240 unless specifically identified.

Digital synthesis is used in the protection features to eliminate many analog problems encountered in long time delays. This design has eliminated the need for large value, low leakage timing capacitors required for "latched" fault logic and "full cycle" soft start functions in other designs[1]. The integration of the logic-level MOSFET with the current-mode controller has allowed optimization of the gate drive design. It also allows the entire delay time from current-mode comparator to MOSFET output to be guaranteed without performance assumptions of an external gate driver.

Minimum external parts count is a goal for all high-density designs. The PWR-SMP260 control section requires seven external components, including the off-line and bootstrap bias supplies. The integrated circuit is designed to connect directly to a feedback optocoupler without any primary-side support circuitry.

Wide range bootstrap and off-line bias supplies make the integrated circuit ideal for universal input battery charging applications as well as power supply applications. The feature set required for battery charging applications contains all of the power supply requirements plus additional requirements. Battery chargers require a wide range output voltage, precise control of the output power, and a method of turning the charger on and off.

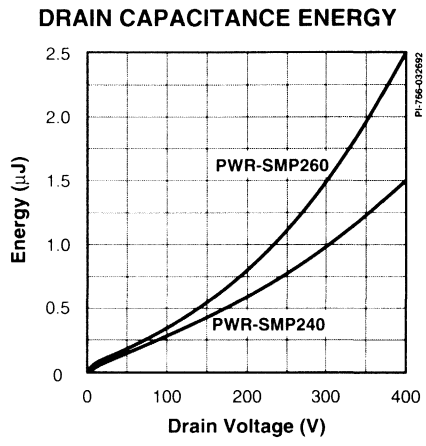

Figure 1.

The Power MOSFET

The gate drive requirements are significantly reduced because of the logic-level threshold voltage and very low Miller capacitance of the lateral geometry MOSFET. However, in an integrated solution the advantage of these characteristics is apparent to the user only as low bias supply current. The power supply designer need only be concerned with the output terminal characteristics of the MOSFET.

The conduction losses of the output MOSFET can be calculated from the on-state resistance ($R_{DS(ON)}$). The PWR-SMP260 $R_{DS(ON)}$ is 3 Ω for currents up to 1 A, and increases to 4 Ω at greater than 2 A. The PWR-SMP240 $R_{DS(ON)}$ is 5 Ω for currents up to 600 mA, and increases to 6.7 Ω at greater than 1.2 A. The practical limit for peak drain current of the PWR-SMP260 in continuous operation is greater than 2 A, and 1.8 A for the PWR-SMP240. Switching losses due to the stored charge on the drain can be calculated from the 2.5 µJ of stored energy at 400 V, (1.5 µJ for the PWR-SMP240). Figure 1 shows the relationship between drain voltage and stored energy in the nonlinear drain capacitance of the MOSFET. Application note AN-9 discusses how to use the drain capacitance stored energy for calculating power supply efficiency. The stored charge in the output rectifier and transformer capacitance reflected to the transformer input must be taken into account to get a good estimate of the total switching loss[2].

The Current Mode Controller

Many of the discrete components required in a current-mode controller design have been integrated in the summing junction function. The number of support components required for a production design has been reduced by at least a factor of two as compared to a "3842/3823 style" circuit.

Summing Junction

The output of the summing junction is a current source. The constant-current output of the sum junction flowing through R_C creates a fixed offset voltage. This voltage is equivalent to the 1 volt maximum comparator input signal on "3842/3823 style" circuits. The maximum comparator input signal is programmable with the value of the primary current sense resistor R_S. The current mode controller compares this offset voltage to the voltage across R_S. The full-scale summing junction output current (480 µA) times the ratio of the gain setting resistor R_C to the current sense resistor R_S will set the maximum current for the current-mode controller and output MOSFET. If the current sense resistor is 250 mΩ and the maximum desired switch current is 2 A, then the gain setting resistor R_C should be:

$$R_C = \frac{I_{pk}}{I_{LIMIT}} \times R_S = \frac{2A}{480mA} \times 250m\Omega = 1k\Omega$$

The output of the summing junction can be controlled by injecting a current into the FEEDFORWARD pin or the FEEDBACK pin. Current flowing into these pins will linearly decrease the current flowing from the summing junction output which controls the peak current in the output switch, as shown in Figure 2. FEEDBACK has an associated current source which insures that the optical coupler will be biased at 480 µA before the summing junction output current will be affected[1]. The voltages on these pins are 1.25 and 2 V respectively and have input impedances of less than 1 kΩ. The FEEDFORWARD and FFEDBACK currents have a gain of 2 within the summing junction.

The PWR-SMP260 is designed for a secondary-referenced error amplifier with optical feedback. However, primary-side regulation can be achieved by adding a primary-referenced error amplifier circuit. A simple error amplifier can be implemented by connecting a Zener diode between the bootstrap bias supply and the optical coupler pin. The current source on the pin will bias the Zener diode and the diode will control the bootstrap bias voltage that is proportional to the output voltage via the transformer turns ratio.

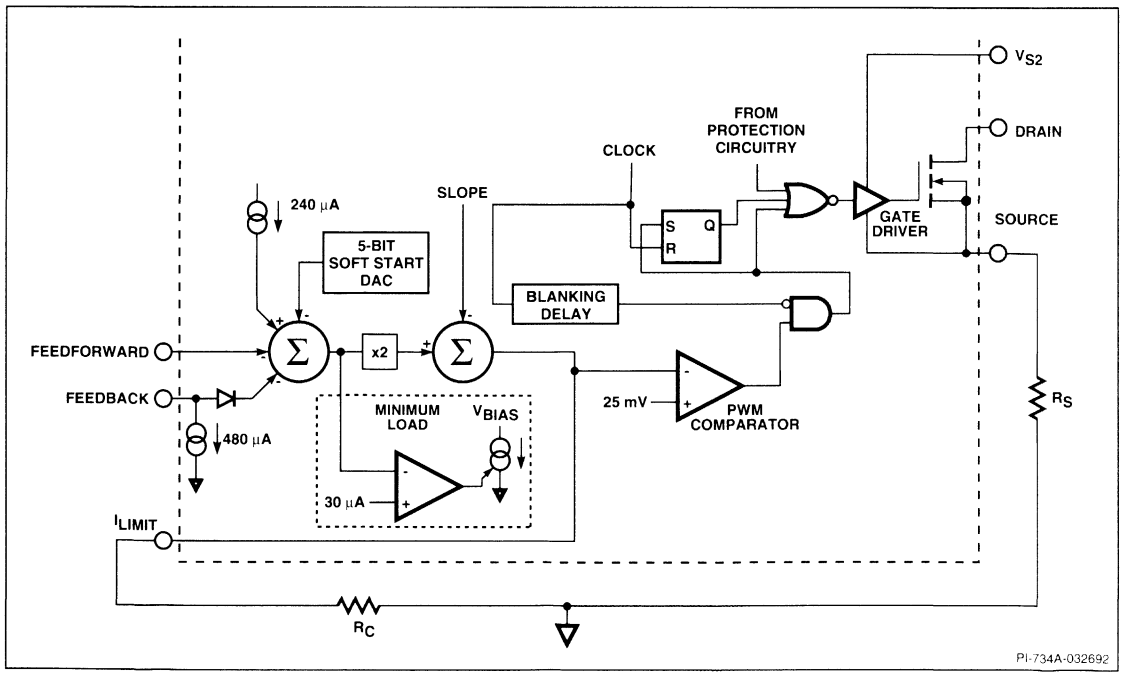

Figure 2. Functional Block Diagram of the Current-mode Controller Section of the PWR-SMP260.

FEEDFORWARD can also be used for control loop compensation for changes in input voltage. A separate pin is provided so that open loop compensation is available when the secondary regulator control loop is open. A constant input power regulator for wide ranges of input and output voltage can be constructed using this feature. This feature along with a wide bootstrap bias supply range is very useful in battery charging applications.

The summing junction also has internal control inputs from the soft-start digital to analog converter and the slope compensation circuit. The soft-start DAC will inject 100% of the reference current into the summing junction at the beginning of the soft start sequence and incrementally decrease the soft start injection to zero.

The slope compensation causes the summing junction output current to be linearly decreased over the programmed pulse width. The rate of decrease is programmable with an external slope compensation resistor. The shape of the compensation current is the same as the oscillator waveform. Slope compensation is inhibited and 50% maximum duty cycle is selected when the SLOPE COMP pin is connected to V_S.

Comparator and Blanking Time

The key elements of the current-mode control circuit are the comparator, R-S flip flop, gate driver, and output transistor. The two parameters of interest are the delay time from the comparator input to the MOSFET output and the leading edge blanking time[4]. The delay time of the current sense comparator, gate driver and output MOSFET are all specified together in an integrated controller. Figure 3 shows the effect of overdrive on comparator delay time. The comparator needs very little overdrive (20 mV) to achieve its 70 ns delay time. The delay time is important in determining the error between desired and actual peak current. The error for a drain current waveform with 542 mA/μs rate of rise (330 μH, 162 VDC input) will increase 38 mA in 70 ns. This translates to a 2.9% error at 1.3 A drain current. At twice the input voltage the error will double to 5.8%, causing an unexpected change in current limit due to the comparator delay time. A discrete design must consider the tolerance of each part, also the effect of the printed circuit board layout capacitance and inductance on circuit delay time. Another advantage of an integrated solution is the gate driver is optimized for the output transistor characteristics. An integrated design also removes the chance of noise injection in the critical gate drive portion of the printed circuit board layout.

Leading edge blanking allows the turn-on current transient to stabilize before the output of the current-mode comparator is connected to the R-S flip flop. The start of the blanking time is the turn-on point of the MOSFET. The blanking time is

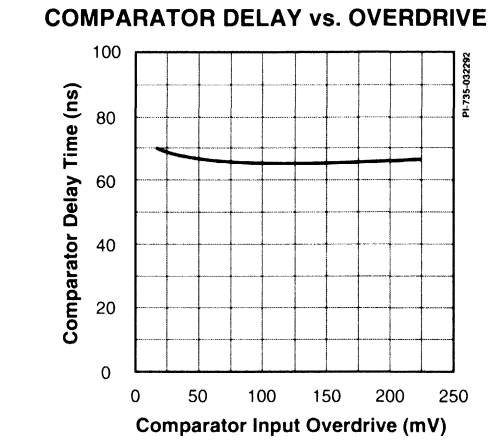

Figure 3.

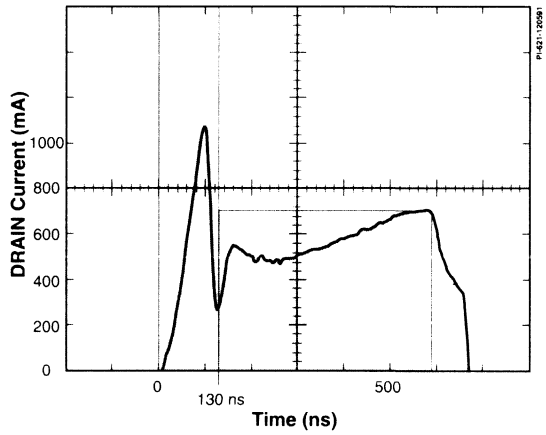

Figure 4. Leading Edge Blanking of a Current Spike.

specified as the maximum time the comparator input can exceed the comparator threshold and not have the output MOSFET switch off. The blanking time, typically 130 ns, is designed to allow the turn-on current spike to recover in a flyback power supply operating in continuous conduction mode with an "ultra fast" rectifier. A current spike waveform similar to Figure 4 will not cause a circuit malfunction.

Oscillator

The oscillator-switching regulator circuit is designed for optimum performance between 30 and 400 kHz. The oscillator waveform is a sawtooth with a slow rise from 50 mV to 1.75 V followed by a rapid discharge. The oscillator will operate at twice the power supply frequency when the 50% maximum duty cycle option is selected. The oscillator frequency is set with a timing capacitor connected to the C_{EXT} pin.

The oscillator charging current source supplies 240 µA and produces a linear slope. The discharge rate is controlled by the 5 Ω $R_{DS(ON)}$ of the discharge transistor. The equation for oscillator frequency is:

$$f = \frac{1}{\left((C_{EXT} + 20pF) \times 7.12 \times 10^{-9}\right) + 100ns} \approx \frac{127 \times 10^{-6}}{C_{EXT}}$$

The oscillator can be synchronized to a clock that is running at a higher frequency. A pulse width of 0.1 to 1 µs applied to the SYNC pin will terminate the clock cycle. The interface circuits for isolated synchronization and remote turn-off signals are shown in Figure 5. The SYNC pin has a CMOS logic level with no hysteresis and is negative-edge sensitive. SYNC has an internal 200 µA pull-up current source to V_{S1}. The 2N3904 has a storage time of approximately 500 ns, which means the maximum driving pulse width will be approximately 500 ns. However, if the signal is held low for longer than 5 to 10 µs, it will be interpreted as a turn-off signal sending the circuit into a power down state which continues for as long as the signal is low. The current consumption of the IC is reduced to 800 µA when the IC is commanded off. The SYNC internal current source is reduced to 20 µA during power down. During shutdown, the high-voltage bias supply will continue to power the circuit.

Maximum Duty Cycle

The maximum duty cycle is user programmable. If a 50% maximum duty cycle is desired, the SLOPE COMP pin is connected to the V_S internal bias supply voltage. A frequency divider flip-flop is inserted between the oscillator and the current-mode R-S flip-flop and the maximum duty cycle will be 50%. The oscillator timing capacitor will need adjustment so that the oscillator will run at twice the output frequency.

If a 90% maximum duty cycle is desired, a resistor is connected between SLOPE COMP and COM. The resistor determines the amount of slope compensation current flowing in the output of the summing junction. Slope compensation has the effect of reducing the current flowing from the summing junction linearly with time. The desired slope compensation resistor value is calculated with the following equation:

$$R_{SLOPE} = \frac{1.75V}{I_{SLOPE}}$$

A current-mode control loop operating in the continuous conduction mode with duty cycles over 50% requires slope compensation for stability[5]. The amount of slope compensation is a function of the slope of the magnetizing current flowing in the MOSFET. Circuits that have discontinuous conduction over the entire duty cycle range do not need slope compensation. However, in noisy environments, a small bypass capacitor is recommended.

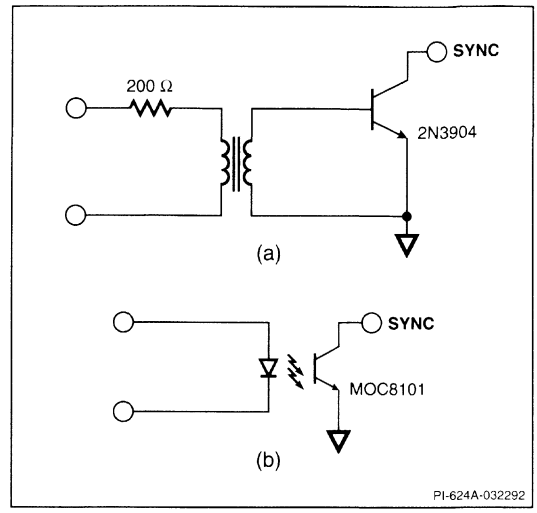

Figure 5. Circuits for (a) Synchronizing and (b) Remote Turn-off.

Minimum Load

The 130 ns leading edge blanking feature of the current-mode controller and the 70 ns comparator to output delay time gives the power supply an effective 200 ns minimum on time. The minimum on time ensures that a minimum amount of power is transferred to the output. This can be a problem for many applications that require no-load operation. The usual solution is to pre-load the output with fixed resistors that are equivalent to the minimum load required by the power supply or allowing the switching frequency to be reduced by initiating a subharmonic oscillation. The pre-load solution is unacceptable in thermally-limited high-efficiency designs. The subharmonic oscillation, often called "hiccup mode" is equally unacceptable because of possible audio noise emissions.

A characteristic of a current-mode controller is that the error amplifier output signal is proportional to the output current or power. The PWR- SMP260 has integrated a minimum load regulator that monitors the onset of the minimum pulse width condition[6]. The circuit monitors the summing junction current before slope compensation is added. A shunt regulator is activated when the summing junction current falls below 12% of full scale. The shunt regulator will increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale. Figure 6 shows the load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However, this occurs when the dissipation in the switching MOSFET is very low. The package has excess thermal capacity and can safely dissipate the power.

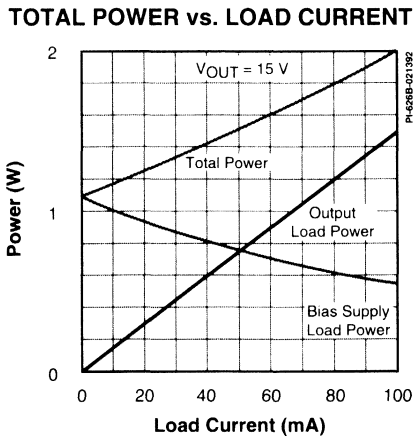

Figure 6. Minimum Load Transfer Effect.

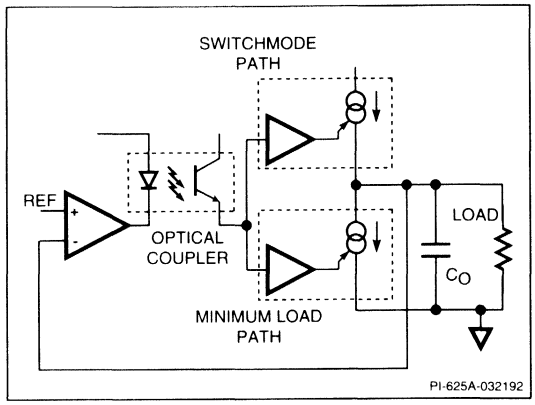

Figure 7. Current-mode and Minimum Load Control Loop.

The control loop gain path is shown in Figure 7. The gain of the minimum load regulator has been matched to the gain of the current mode switching regulator. This allows the control loop dynamics to remain the same whether the minimum load circuit is active or not active.

The output transient load response is shown in Figure 8. Note that at light load the gain of the switch mode path decreases but the gain of the minimum load path remains the same and the transient load response is not significantly degraded. An interesting side effect of the minimum load circuit is its effect on bias supply power during a transient, shown in Figure 9. The power consumed from the bias supply is greater than the average of the two states when the period of the transient is close to the control loop response time. The control loop overshoot, settling time and transient repetition rate affect this characteristic.

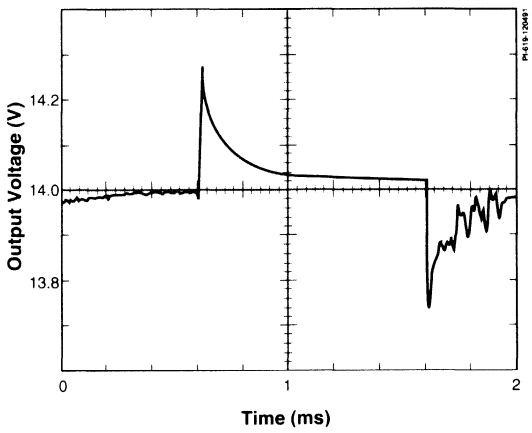

Figure 8.

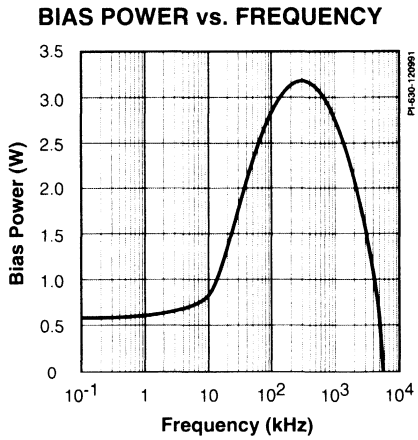

Figure 9. Effect of Load Transient Frequency on Bias Power.

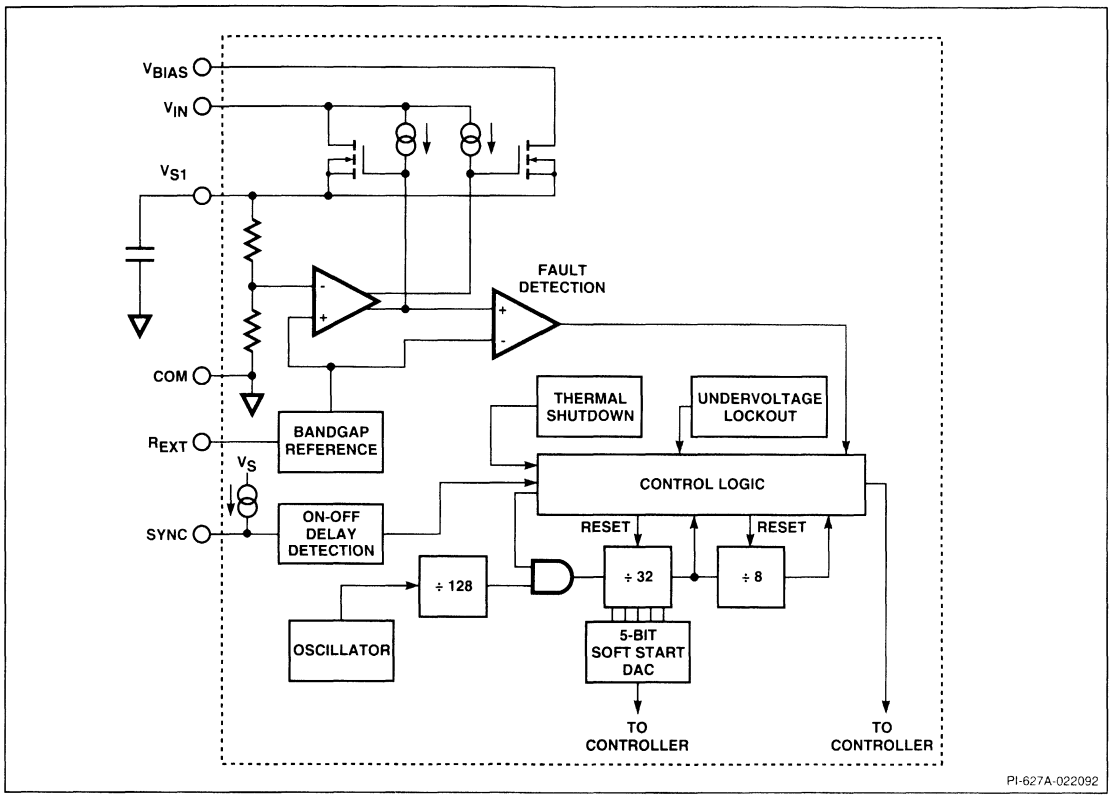

Figure 10. Functional Block Diagram of the Regulator and Protection Circuits of the PWR-SMP260.

Bias Regulators & Protection Circuits

The high-voltage linear regulators and power supply fault detection and recovery sequencing circuits are shown in the block diagram of Figure 10. The high-voltage linear regulator continuously powers the control circuit over a V_{IN} range of 20 to 400 VDC. The bootstrap bias supply, V_{BIAS}, turns off the high-voltage regulator when the V_{BIAS} voltage exceeds the fault detector threshold voltage of approximately 10 V. The integrated circuit cannot be turned on from the V_{BIAS} supply, as the gate pull up current source is connected to the V_{IN} pin.

Figure 11 shows the typical current requirements for the PWR-SMP260 and PWR-SMP240 as a function of frequency with the 90% maximum duty cycle option selected. The data was taken with 10 V on the V_{IN} and V_{BIAS} pins. The data is valid for the 50% mode if the output frequency is used. The slope of the curve is mainly due to the gate drive power which is a function of the output frequency (46 µW/kHz).

Bias Regulators

The linear regulator for the internal supply voltage V_S has two sources of power. They are the bootstrap bias supply and the off-line high-voltage supply. The regulator has a built-in preference for the bootstrap bias supply. Should the bias supply be incapable of supplying the total requirement, the remaining current will be sourced from the off-line supply. A 25 µA current source connected to the V_{IN} pin is the only current consumed from the off-line voltage when the off-line regulator is turned off.

The internal V_S supply voltage will be operational at a minimum V_{IN} voltage of 20 V. This is independent of the bootstrap bias supply voltage. The wide range of the bias voltage, 10 to 30 V, allows significant output voltage range which is useful in battery charging applications.

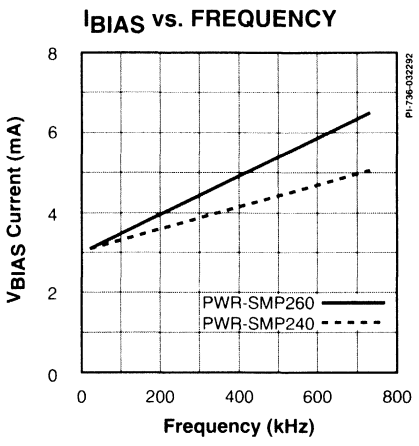

Figure 11.

Reverse current through the bootstrap bias regulator transistor has been eliminated. The V_S supply will not be loaded by circuitry powered from the bias supply at turn-on. Additional primary-referenced circuitry may be powered from the bootstrap bias supply without affecting the operation of the control circuit. The output impedance of the V_S supply is approximately 50 Ω and must be bypassed with 100 nF capacitor.

AC voltage on the V_{BIAS} supply can inject currents into the summing junction through the optical coupler and into the FEEDBACK pin. The optical coupler collector-base is capacitive at the power supply frequency. Thus the AC voltage on V_{BIAS} can be coupled directly to the feedback input of the summing junction. The input impedance of FEEDBACK is less than 1 kΩ. 100 mV of ripple on V_{BIAS} will inject at least 100 μA of AC current into FEEDBACK. The active dynamic range of the FEEDBACK input is 240 μA, thus 100 μA will cause the I_{LIMIT} to change 42%. This susceptibility to AC currents can be reduced to acceptable levels in at least 4 ways.

1. Place a resistor in series with the opto-coupler to increase the input resistance and decrease the AC current. 4.7 kΩ will provide sufficient voltage for the opto-coupler to operate. This is the preferred solution.

2. Filter V_{BIAS} to a low ripple value.

3. Filter just the optical feedback signal path with an RC filter.

4. Power the optical coupler from a small-signal FET source follower connected to V_S. A FET was chosen because special care was made in the design of the PWR-SMP260 to not allow any load on the V_{BIAS} supply affect the V_S voltage. If a bipolar emitter follower must be used, a 100 kΩ resistor in series with the base lead is recommended.

Protection Functions

Protection features include input undervoltage lockout, overtemperature fault, output undervoltage fault and output overcurrent protection consistent with cycle-by-cycle peak limiting of the switch current. The input undervoltage lockout holds the gate of the output MOSFET low and resets the soft-start counter chain until the V_S supply voltage is within its valid operating range. The fault conditions control the functioning of the "latched fault logic" and restart delay sequence.

The power consumption of the control circuit is reduced during a fault to limit self-heating of the off-line regulator.

The PWR-SMP260 monitors the temperature of the power transistor and controls the operation of the power supply so that the peak junction temperature of the switching transistor is held to a safe temperature during over-temperature conditions. When an over-temperature condition is sensed (approximately 140°C), the power supply output is turned off and the controller is put in a low-power mode until the transistor cools 45°C. The power consumption of the control circuit is reduced during a fault to limit self-heating of the off-line regulator. When the power supply turns on again it will begin a soft-start cycle.

A fault condition also will be declared when the bootstrap bias voltage drops low enough to draw current from the off-line regulator. This condition indicates that the output voltage is significantly out of regulation and an overload condition exists. The fault condition is not declared when the bootstrap bias voltage is low and the minimum load circuit is active. The bootstrap bias voltage can be momentarily be pulled low during a minimum load transient which would erroneously indicate a fault.

The "latched fault logic" turns off the output MOSFET, reduces the power consumption of the control circuit and starts the restart delay sequence. When the counter reaches 28,672 power supply equivalent cycles the soft start sequence starts.

The power up sequence is 4096 power supply cycles long. During this time the switching regulator circuits are enabled and the bootstrap bias supply should reach its valid operating range. The bootstrap bias voltage is monitored at the end of this period. If the voltage is below the regulation voltage, a fault is signaled and the cycle repeats. This characteristic produces a foldback current limit function as shown in Figure 12. This function is very effective for limiting the dissipation in overload and short circuit conditions. The undervoltage lockout resets the last 8 bits of the 15 bit counter. During the first soft-start sequence, the count for the zero current state will vary from 3969 and 4096 power supply equivalent cycles as the state of the first 7 bits are undetermined at the beginning of the count.

Soft-Start

The soft-start function slowly increases the I_{LIMIT} current available from the summing junction output. Slowly increasing I_{LIMIT} will slowly increase the output current and output voltage. This characteristic will significantly reduce the peak power stress on the output rectifier and improve the demonstrated reliability of the power supply. Flyback power supplies without soft-start will drive a large short circuit current into the output capacitor and rectifier causing a peak power stress many times higher than normal operating.

Soft-start is initiated when V_{SI} is in regulation. The soft-start time is controlled by the oscillator frequency. The first twelve bits of a fifteen bit counter set the soft-start time of 4,096 power supply equivalent cycles. I_{LIMIT} is controlled by a five-bit digital to analog converter decoding the eighth through the twelfth bit of the counter chain. I_{LIMIT} will increase from zero to full scale in 4096 cycles of the power supply. Note that the change in oscillator frequency for 50% duty cycle mode will not affect this timing. A digital implementation of soft-start was used because it used no external parts and provided a more reliable solution.

Upon completion of the soft-start time, the fault detection function is enabled. The fault detector monitors the V_{BIAS} supply, which is related to the output voltage of the power supply. If a fault is not detected at the end of soft-start, the counting action of the counter chain is inhibited and the count is held at that point awaiting a fault. If an output overload occurs, the current limit will cause the output voltage to decrease. If V_{BIAS} falls below the fault detector level, the power supply will be turned off, limiting the current delivered to the overload and the counter chain will be enabled. The power supply will continue to operate into the overload until the output/V_{BIAS} voltage decreases to the fault detector threshold. The transformer turns ratio between the output and V_{BIAS} sets the threshold for the output voltage.

The circuit will check to determine if the output overload has been removed after the automatic restart time. The last three bits of a fifteen bit counter set the automatic restart time of 28,672 power supply equivalent cycles.

One objective of the soft-start circuit is to limit the current delivered to the output capacitors. However the voltage on the capacitors must be increased to the V_{BIAS} fault threshold before the end of the soft-start time or a fault will be detected and the power supply will be turned off, discharging the output capacitors. The effect on the power supply design is that the amount of capacitive stored energy in the output filters must be limited. The amount of capacitive stored energy is a function of the power level of the power supply, the V_{BIAS}-to-output turns ratio, and the power supply frequency. The maximum capacitance of a 30 watt universal input power supply operating

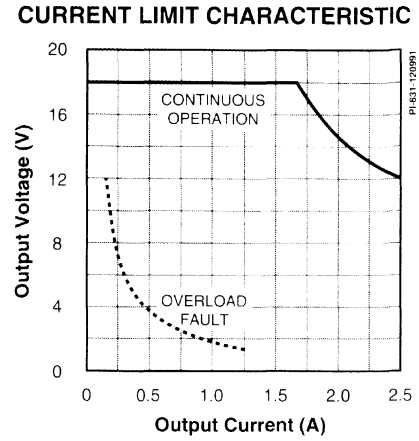

Figure 12. Foldback Current Limit.

at 120 kHz with a 15 V output and a 36:7:7 transformer is 2,000 µF. A power supply with an operating frequency of half of the example can have twice the output capacitance.

Power-up is when most power supplies fail. The soft-start function reduces all of the power supply component peak stresses during the power up sequence. This produces a power supply with superior demonstrated reliability. The auto-restart duty cycle of 1/8 reduces the power dissipation in the output rectifier and filter. The triangular ramp up of power during the soft-start time reduces the effective auto-restart duty cycle to 1/16.

The soft-start counter will be set to the beginning count if V_S goes undervoltage. When the overtemperature circuit is active, the auto-restart counter will continue to count. The counter will stop counting and hold at the beginning count of soft-start until the release of overtemperature signal. The effective overtemperature minimum off time is the auto-restart off time.

Turn On Sequence

The sequence of events when the power supply turns on, shown in Figure 13, is controlled by the biasing and power management functions of the IC. When AC voltage is first applied to the input terminals of the power supply, the voltage on the power line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{IN} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain will remain reset until V_{SI} is in regulation. The soft-start sequence begins when V_{SI} is in regulation. The peak switching current will increase as soft-start progresses. The soft-start time

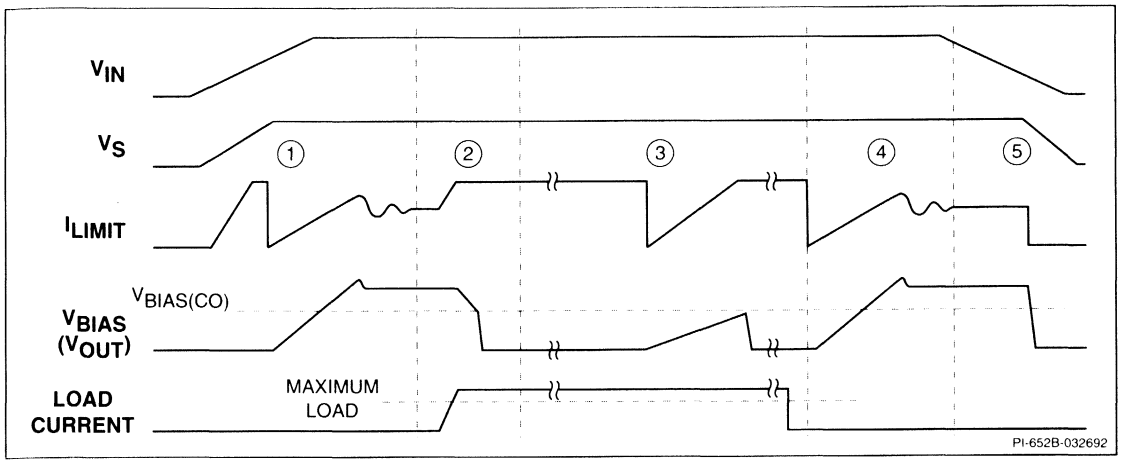

Figure 13. Start-up Waveforms (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

for a 120 kHz power supply is 34 ms, allowing the power line filter capacitor two powerline cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the power line filter capacitor. During the soft-start sequence the counter chain is counts and the five bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. The output and V_{BIAS} voltages will increase beyond the fault detection threshold. The output error amplifier will reduce the peak switch current when the desired output voltage is reached. The output voltage will overshoot slightly and return to the desired output voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

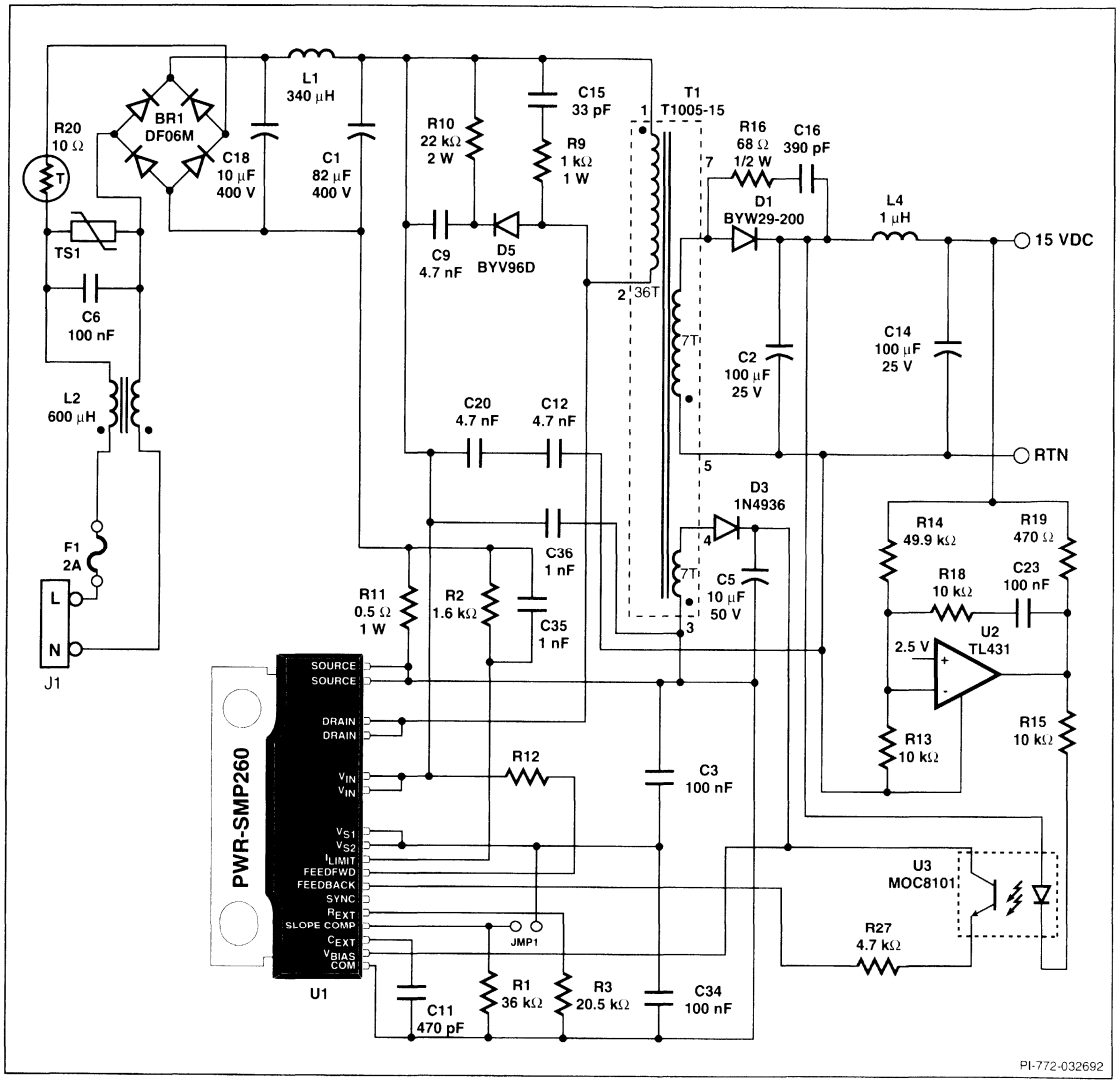

Figure 14. 30 W Universal Input Flyback Power Supply Circuit Utilizing the PWR-SMP260.

Typical Application

The schematic for a 30-watt flyback power supply is shown in Figure 14. The line and load regulation of this supply is <0.1%. The circuit can be designed to operate continuously over the universal input voltage range of 85 to 265 VAC_{RMS}. The 30 W circuit has been demonstrated within an enclosure with a volume of 11 cubic inches.

A forward converter can be constructed by replacing the secondary-side components of Figure 14 with those shown in Figure 15. The output inductor is common with the bias supply to insure minimum load operation.

Flyback Current Limit Independent of Input Voltage

A flyback power supply with a primary-side peak detecting current limit has an output current limit threshold that increases with increasing input voltage. Designs that use frequency modulation for regulation such as a blocking oscillators, exacerbate this characteristic. A fixed-frequency design can be optimized to have a relatively constant peak drain current as a function of input voltage for a particular output power. Using feedforward compensation, most designs can be corrected to a first order for a constant output current limit point with respect to input voltage. A characteristic of the current mode controller is that changes in input voltage will automatically be compensated for by the current mode controller trying to maintain the final switching current without any change in the error signal.

Figure 16 shows how the peak drain current for several transformer designs changes with input voltage for a constant output power of 30 watts. The transformer turns ratio is 36:7 and the primary inductance ranges from 300 to 1000 µH. The 300 µH design has the most constant relationship between peak drain current and input voltage. The higher inductance designs have a negative slope to this relationship and require some feedforward compensation to achieve a constant output current limit value. Figure 16 was generated from the efficiency versus input voltage data, and the results have been compensated for actual efficiency and its variations with input voltage. The peak drain current was calculated with a spreadsheet and the following equations. The voltage transfer function for a flyback supply is:

$$\frac{V_o}{V_{in}} = \left(\frac{N_S}{N_P}\right) \times \frac{D}{(1-D)}$$

solving for duty cycle:

$$D = \frac{1}{1 + \left(I_O \times \frac{N_S}{\eta \times I_{in} \times N_P}\right)}$$

$$I_{AC} = V_{DC} \times \frac{D}{L \times f}$$

$$I_{pk} = \frac{I_{in}}{D} + \frac{I_{AC}}{2}$$

A flyback power supply operating in the continuous current mode with 30 watts of output power has measurements of V_{in} = 168 V, Iin = 217 mA, V_O = 14.97 V, I_O = 2 A, N_S/N_P = 7/36, f = 120 kHz, and L_P = 330 µH, then:

$$D = \frac{1}{1 + \left(2A \times \frac{7}{0.81 \times 217mA \times 36}\right)} = 31.1\%$$

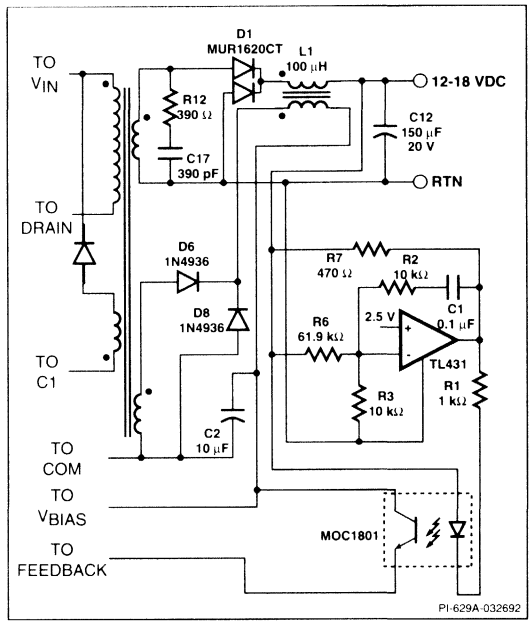

Figure 15. Secondary-side Changes to Form a Forward Converter.

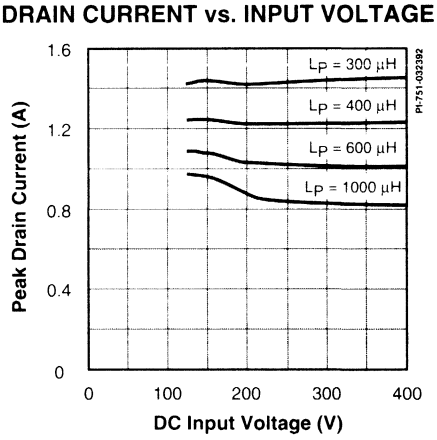

Figure 16.

$$I_{AC} = 168V \times \frac{31.1\%}{330\mu H \times 120kHz} = 1.32A$$

$$I_{pk} = \frac{217mA}{31.1\%} + \frac{1.32A}{2} = 1.358A$$

The peak drain current is 1.358 amperes.

The value of the feedforward compensation resistor can be calculated with the following procedure. Calculate or measure the peak drain current at nominal 110 and 240 VAC operating points. The 1000 µH design shown in Figure 16 has peak drain currents of 934 mA at 154 VDC and 840 mA at 336 VDC. These two points form a line that represents the amount of feedforward compensation required. The Y-intercept is then determined to be 1.014 A. The feedforward resistor value can be computed with the following equation once the Y-intercept (I_Y) and an operating point is known.

$$R = \frac{V_{DC}}{240\mu A \times \left(1 - \frac{I_{pk}}{I_Y}\right)}$$

If I_Y = 1.014 A, V_{DC} = 336 V, and I_{pk} = 840 mA, then:

$$R = \frac{336V}{240\mu A \times \left(1 - \frac{840mA}{1.014A}\right)} = 8.2M\Omega$$

The current limit resistor values can be calculated once the feedforward compensation has been calculated. The feedforward compensation for the 1000 µH transformer, 8.2 MΩ, will reduce the output current of the summing junction at current limit from 240 µA to:

$$240\mu A - \frac{336V}{8.2M\Omega} = 240\mu A - 41\mu A = 199\mu A$$

If the current sense resistor, R11 standard value of 500 mΩ is chosen, then the voltage across the current sense resistor with 840 mA flowing is 420 mV. R2 can be calculated from:

$$R2 = \frac{V_{CL}}{I_{CL}} = \frac{420mV}{199\mu A} = 2.11k\Omega$$

2.10 kΩ is a standard 1% value.

The example transformer with 300 µH primary inductance has no feedforward compensation and has a peak drain current of 1.436 A. If a 500mΩ resistor is used for R11, then R2 = 3 kΩ.

Resistors and Capacitors

The power dissipation in the current sense resistor can be calculated from the transformer primary RMS current:

$$I_{RMS} = \sqrt{\frac{D \times \left(i_a^2 + (i_a \times i_b) + i_b^2\right)}{3}}$$

where I_a is the initial current, I_b is the peak drain current, and D is the duty cycle. The calculation for the peak drain current has all the information to calculate the transformer primary RMS current:

$$I_a = \frac{217mA}{31.1\%} - \frac{1.32A}{2} = 38mA$$

$$I_{RMS} = \sqrt{\frac{31.1\% \times \left(38mA^2 + 51.6mA^2 + 1358mA^2\right)}{3}} = 443mA$$

The power in the 500 mΩ current sense resistor R11 is:

$$443\ mA^2 \times 0.5\ \Omega = 98\ mW$$

The RMS current in the input capacitor is equal to the transformer primary RMS current less the input current I_{in}:

$$I_{C(RMS)} = 443\ mA - 217\ mA = 216\ mA$$

The ripple current rating on a 68 to 100µF, 400V capacitor is between 0.3 and 0.4 A RMS at 105°C. The ripple current rating on capacitors changes with ambient temperture and frequency.

The RMS current in the output rectifier is described by the equation:

$$I_{RMS} = \sqrt{\frac{D \times \left(i_a^2 + (i_a \times i_b) + i_b^2\right)}{3}}$$

where D is the conduction duty cycle of the output rectifier, I_a is the initial current, and I_b is the final current flowing during the conduction time. The RMS current in the output capacitor is equal to the diode RMS current less the load current:

$$I_{RMS} = \sqrt{\frac{D \times \left(i_a^2 + (i_a \times i_b) + i_b^2\right)}{3}} - \frac{(I_a + I_b) \times D}{2}$$

For example, if the load current is 2 A, the output rectifier duty cycle is:

$$100\% - 31.1\% = 68.9\%$$

The initial diode current can be found by:

$$I_a = I_{pk} \times \frac{N_P}{N_S} \times \eta = 1.358A \times \frac{36}{7} \times 81\% = 5.657A$$

and the final diode current is:

$$I_b = I_m \times \frac{N_P}{N_S} \times \eta = 38mA \times \frac{36}{7} \times 81\% = 158mA$$

The average current during the conduction time is:

$$\frac{5.657A + 158mA}{2} = 2.907A$$

The output current is:

$$2.907\ A \times \text{diode duty cycle} = 2.907\ A \times 68.9\% = 2\ A$$

The diode RMS current is:

$$I_{RMS} = \sqrt{\frac{68.9\% \times \left(5657mA^2 + 894mA^2 + 158mA^2\right)}{3}} = 2.75A$$

The capacitor RMS current is:

$$I_{RMS} = 2.75\ A - 2\ A = 750\ mA$$

An Os-con 10x10 mm capacitor and a low ESR aluminum electrolytic 8x20 mm capacitor have ripple current ratings at 105°C of approximately 800 mA and are acceptable for this application.

The rectifier output capacitor should be chosen with care as its ripple current could be 4 times the output current. If the output voltage is low (for example, 7 V for a 6 V battery), then a forward converter might be the better choice of topology. The schematic for the forward converter is shown in Figure 15.

Transformer

Transformers of this power level can be wound using margin winding or insulated wire techniques as discussed in AN-7 and DA-3. The only special requirement that the PWR-SMP260 places on the transformer design is the requirement that the bias winding be capable of delivering 100 mA average load current when the minimum load circuit function is active. The capacitance between the bias winding and the primary should be minimized as this can inject noise currents into the PWR-SMP260 control circuit. The symptom of this noise is an apparent leading edge blanking problem. The winding of the primary should provide for the minimum interwinding capacitance and leakage inductance. If a split-primary type of construction will meet the cost requirements for the transformer, it should be strongly considered. However, if this not feasible, a multi-layer primary should be wound in one direction only to minimize interwinding capacitance. Interwinding capacitance will appear as unexplained heat in the power transistor.

A high-efficiency single output supply for a battery charging application may need to have the multi-filar wound secondary winding as the skin depth of the third harmonic of a 120 kHz power supply is equivalent to #31 AWG or 0.23 mm. Figure 17 shows the skin-depth frequency for common AWG values and their metric equivalents. Skin depth is the distance from the surface where the AC resistance of a conductor is twice the DC value and is considered the point of diminishing returns for a high frequency conductor.

This multi-filar winding technique can be used to force current sharing in multiple output rectifiers. Half the output winding is connected to one diode in the center tapped bridge rectifier and the second half of the output winding is connected to the second diode in the bridge rectifier. If a foil secondary winding structure is desired, as is the case with T1005, then the thickness of the foil should be limited to the diameter for the wire gage chosen above (#31 AWG diameter is 0.004 inches, thus maximum foil thickness should be 0.004 inches). The use of high-voltage Schottky diodes should be considered for medium and low output voltages as the reverse recovery times will greatly improve efficiency and generated noise in the continuous conduction mode.

A forward converter transformer and output inductor can be constructed on one magnetic structure which would minimize the negative material cost impact of changing from a flyback configuration to a forward configuration.

The difference between a 240 VAC and a universal transformer design is the number of turns on the primary winding and the air gap in the core. In general the 240 VAC design has twice the number of primary turns with wire half the area. The air gap in the core is increased so that the inductance with twice the turns is only two times the universal transformer value. The number of secondary and feedback turns remain the same. The primary current for a 240 VAC transformer is half that of a universal transformer.

The difference between a universal transformer and a 100 VAC transformer is the margin winding dimensions inside the bobbin. The margin winding dimensions are 2.5 mm for 100 VAC and 5 mm for universal voltage per IEC950 and UL1950. The number of turns will remain the same.

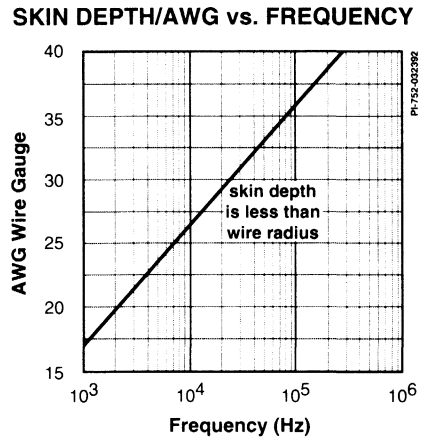

Figure 17. Skin Depth.

EMI Filter

The difference in EMI between an integrated circuit such as the PWR-SMP series and a discrete circuit is dependent on the circuit layout and the transformer design and construction. However, the integrated approach will be superior as all high-speed drive circuits are located on the IC and the heat sink for the IC is referenced to circuit common, not the drain. A typical TO-220 power tab package has 40 pF of stray capacitance from the drain to heat sink. This will produce a 180 mA, 100 ns pulse of current that can cause common-mode EMI problems.

The differential or normal-mode EMI filtering requirements for the 330 µH example power supply design can be estimated from the following calculations and references to Figure 16. The amplitude of the fundamental frequency component of the switching current is equal to:

$$I_1 = \frac{I_{pk}}{\pi D^2} \times \sqrt{\sin^2(\pi D) + \pi D \times (\pi D - \sin(2\pi D))} = 379\text{mA}$$

where D = 31.1% and I_{pk} = 1.358 A

379 mA times the input capacitor ESR of 300 mΩ will produce 114 mV_{RMS}. The "B" level at 150kHz is 54db-uv which is 0.5mv RMS. Thus the normal mode EMI filter must provide 47db of attenuation with a 50 ohm termination impedance. A single stage normal mode EMI filter, L1, C1, C___ is shown in figure 14 to provide the required attenuation.The input capacitor can be modeled as a series R-L circuitwhere R equals 300 mΩ and L equals 48 µH, which sets the R-L corner frequency of 1 MHz.

Package and Layout Considerations

The integrated circuit package is a single in-line power tab package 30 mm wide by 3.5 mm thick by 20.2 mm high. The high-voltage pins have a 3.1 mm gap between them for international safety spacing requirements. The pins are on 1.27 mm (0.05 inch) centers with a 2.54 mm (0.1 inch) stagger bend. This allows a printed circuit board to be designed with a high-voltage pad-to-pad spacing greater than the required 2.5 mm for IEC950. A pad diameter of 1.52 mm (.04") and a hole size of 1.02 mm (.026") can be used.

The power tab is electrically connected to the source of the output MOSFET. An insulator between the heat sink and the power tab is not required. Connecting the heat sink to the circuit common is also advantageous for EMI suppression. Circuit nodes that are sensitive to layout configuration and coupled noise include FEEDBACK and FEEDFORWARD. Any current spikes coupled into these nodes will be transferred to I_{LIMIT} and cause false triggering. V_{S1} and V_{S2} are also sensitive to circuit trace lengths. V_{S2} is the bypass capacitor for the switching transistor gate drive and should be returned to SOURCE. V_{S1} is the output of the high-voltage linear regulator and powers the analog circuits and should be returned to COM. SOURCE and COM are both connected to the substrate and the heat spreading tab. V_{S1} and V_{S2} must be connected together, either directly or through a 150 Ω resistor.

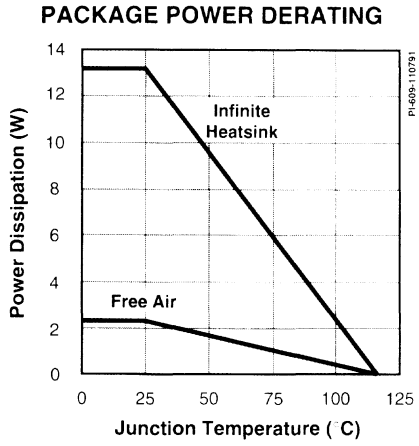

Figure 18. Power Dissipation Capability of the 23-Pin SIP.

Thermal Design

The PWR-SMP260 is packaged in a 23 pin power tab single inline (SIP) package with a junction to case thermal impedance of 7.2°C/W. Figure 18 gives the power dissipation of the package in free air and connected to an infinite heatsink.

The amount of power that can be delivered from an unvented plastic enclosure is limited by the power dissipation within the enclosure and the efficiency of the power supply. The majority of the heat within the enclosure is dissipated by the output rectifier and PWR-SMP260. The thermal model for the plastic enclosure assembly consists of two major thermal impedances. These impedances are from ambient air temperature to surface temperature of the plastic enclosure and from the enclosure to the dissipator heatsinks. The thermal impedance for the enclosure is inversely proportional to the exposed 5 sided surface area (147°C-in²/W). Plastic is a poor thermal conductor, however it is much better than air so place the heatsink within 0.1 inch of the inside surface of the enclosure. The heat does not spread well within the plastic enclosure. This effect was demonstrated by measuring the two thermal impedances of the plastic enclosure (32.5 mm x 60 mm x 95 mm) with two sizes of heatsinks. The heatsinks covered 50% and 100% of the enclosure inside surface. Doubling the heatsink area reduced the thermal impedance from the heatsink to the surface of the enclosure by a factor of two. The thermal impedance from the enclosure

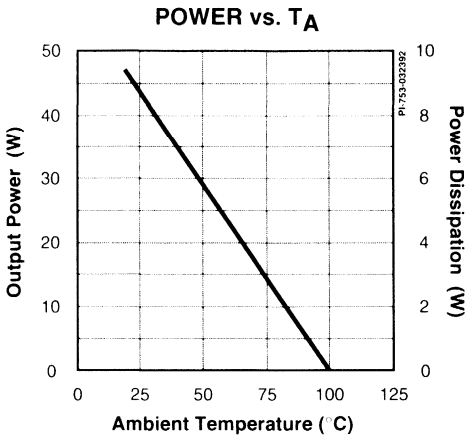

Figure 19. Output Power Capability Within an Enclosure.

surface to ambient should not change as the surface area of the enclosure did not change. However the thermal impedance of enclosure surface to ambient was reduced by 25% for the larger inside heatsink. Thus the heat was being distributed over a larger area of the enclosure and the effective size of the enclosure was increased 32% by distributing the heat to all of the enclosure.

The surface temperature of a plastic enclosure is limited to 70°C rise from nominal operating temperature by Underwriters Laboratories, UL1950. The heatsink temperature is limited to approximately 100°C as the ambient air around the capacitors must be less than 105°C. The capacitor temperature is the limiting factor for the heatsink temperature. The air within the enclosure is equal to or greater than the heatsink temperature.

Figure 19 shows the relationship between ambient air temperature, power dissipation within a plastic enclosure and 83% efficient output power. The surface temperature is limited to 95C and a heatsink temperatute to 100°C. If the ambient temperature is 50°C the maximum dissipation inside the box must be limited to 6 watts or the heatsink temperature will exceed 100°C. The enclosure surface temperature for this condition is 86°C.

Special Characteristics and Features

Error Amplifier

The gain of the optical coupler is equal to the current transfer ratio (CTR). The CTR for a MOC8101 optical coupler is typically 0.5 with a range of 0.3 to 1 when operating at output currents between 500 and 750 µA. The input impedance of the optical coupler port on the integrated circuit is kept low so that the pole formed by the optical coupler capacitance will be as high frequency as possible.

The following equation describes gain of the typical TL431 error amplifier circuit shown in Figure 14.

$$\frac{I_D \times R_O}{V_O} = 1 + \frac{\frac{1}{2\pi \times R14 \times C23} \times \left(1 + \frac{F}{\frac{1}{2\pi \times R_{18} \times C_{23}}}\right)}{F}$$

The error amplifier circuit has two forward gain paths. The first is through the amplifier section, which is dominant until the amplifier reaches unity gain. The second is directly from the output to the optical coupler. At frequencies greater than the unity gain frequency the signal path directly from the output to the optical coupler dominates. See application note AN-8 for a complete treatment of the response of this circuit.

Output Filter

Circuits that have an output pi-section filter should partition the error amplifier. The optical coupler should be connected to the input of the pi-section filter and the voltage sensing divider should be connected to the output of the pi-section filter. This insures that the two poles of the output pi-section filter will not be present in the high-frequency response of the error amplifier. The pi-section output filter will decrease output voltage ripple but will also increase the output impedance of the power supply. The rectifier side capacitor of the pi-section filter should be larger than the output capacitor to insure that the resonant frequency of the filter will not be to close to the gain cross over frequency of the control loop. The minimum value of the output capacitor is set by the maximum output impedance specification. See Application note AN-8 for more information regarding this technique.

Peak Drain Voltage

There are two typical circuits for limiting the leakage inductance flyback voltage spike across the switching transistor. The first uses an additional winding on the transformer to limit the voltage to twice the DC input voltage The second circuit, which has been used on the EVAL series power supplies, uses a dissipative clamping network. The network will clamp the drain voltage to 100 to 150 volts over the DC input voltage.

The 700 V rating of the PWR-SMP260 is sufficient for 250 VAC applications as the maximum rectified input voltage is 375 VDC. The peak transformer flyback voltage is 150 V, bringing the peak repetitive voltage to 525 V. Common design practice is to derate the repetitive working voltage to 80% of rated breakdown voltage, or 700 V × 0.8 = 560 VDC. This provides an actual derating ratio of 75% for additional margin. The margin for lightning strike surges and other non repetitive power line transients is 175 V (700 V - 525 V) after attenuation by the input filter. The value of R10 in the schematic diagram of Figure 14 is chosen to limit the voltage across C9 to 150 VDC.

Test Mode

The integrated circuit has a test mode that cannot be encountered during normal circuit operation. The test pin turns on the power transistor continuously for testing of $R_{DS(ON)}$. The test pin on the PWR-SMP260 is ILIMIT, and its activation voltage is within 1 volt of V_{SI}.

References

1 Andreycak, Bill and Wolford, Larry, "High frequency PWM controllers - a new enhanced generation," HFPC Proceedings, June 1991, pp. 94-107

2 Berdard Corp Booklett on stored charge(?)

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4 Andreycak, Bill, Wolford, Larry, "High frequency PWM controllers - a new enhanced generation," HFPC Proceedings, June 1991, pp. 94-107

5 Hsu, S.P., Brown, A., Rensink, L., and Middlebrook, R.D., "Modelling and analysis of switching DC-DC converters in constant-frequency current-programmed mode," Proceedings of the IEEE Power Electronics Specialists Conference, 1979, pp. 284-301

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Circuit Board Layout with the PWR-SMP Family

DESIGN AID DA-2

Printed circuit board design is an important factor in the performance of switching power supplies. Proper attention to the printed circuit layout will eliminate ground loops, reduce output noise levels, reduce conducted and radiated EMI, and meet the requirements for electrical isolation. These guidelines will help the designer avoid some common problems associated with switching power supply printed circuit layout.

The concepts presented here also apply to breadboards constructed for purposes of experimentation. Attention to the guidelines for current paths, ground loops, conductor length and loop area will minimize noise related problems when breadboarding.

The example given here is a single output 5 volt power supply designed for the PWR-SMP3 (PWR-EVAL1). This power supply has been recognized by Underwriter's Laboratories for "Business Machine Applications Including Data Processing Equipment" operating from 125 VAC input according to UL1950. The power supply has also been designed to meet FCC, part 15, subpart J, EMI conducted emissions (class A and B). A complete schematic diagram of the power supply is shown in Figure 6 while the PC design is shown Figure 12.

Basic Design Rules

Following these general layout practices will reduce the problems associated with high-frequency power supply layouts:

- Identify the Current Path for Each Circuit
- Eliminate Ground Loops
- Minimize Conductor Loop Area for Fast Changing Currents
- Minimize Conductor Length for Fast Changing Voltages
- Use double sided PC board construction with primary and secondary reference planes.
- Shape planes to contain loops with fast changing currents.
- Eliminate trace inductance when connecting to capacitors.
- Eliminate trace to trace capacitance when connecting to inductors.
- Maintain sufficient clearance/creepage distances. Special attention is required for:
  - Spacing between high voltage component pads and planes
  - Spacing between traces, pads, and transformer core

Determining Current Paths

Some components contain fast changing currents while others do not. The first step to a successful power supply layout is to identify and contain the fast changing currents. The key fast changing current waveforms are confined to the circuit of Figure 1 when the power switch is on and the circuit of Figure 2 when the power switch is off.

The shape of the ON-state current waveform is a composite of a trapezoidal primary current I_1 and a leading edge spike current I_2 caused by charging the RC network (C13 and R9). These currents flow in the indicated loop. The current flows out through COM pins 12 and 13, through resistor R19, input capacitor C1, C15, the series connection of transformer T1 primary, and back in to DRAIN pins 15 and 16. Trace length and loop area of this circuit must be minimized.

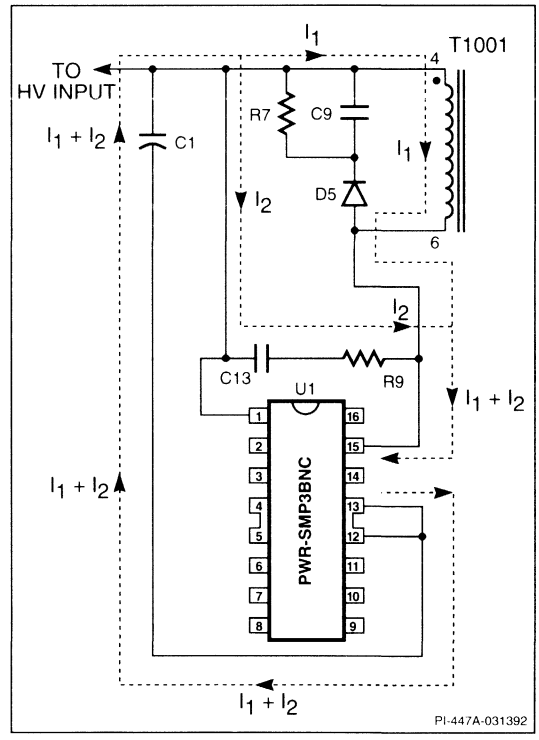


Figure 1. Current Paths when the MOSFET is ON.

Fast changing currents flow in three distinct and separate loops when the power MOSFET transistor turns off as shown in Figure 2. Current I_3 is a very narrow spike current caused by transformer leakage inductance. Trapezoidal current I_4 flows out the transformer power secondary through diode D2, capacitors C2 and C10, back to the transformer. Trace length is extremely critical since I_4 is the highest current. Current I_5 flowing through D3 and C5, although much lower than I_4, is still fast enough to cause problems if not properly treated. Trace length and loop area for these circuits must also be minimized.

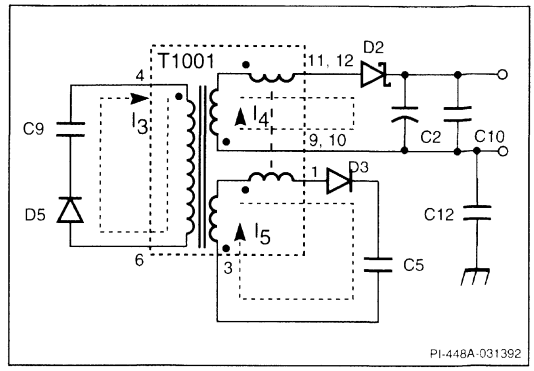


Figure 2. Current Paths when the MOSFET is OFF.

Eliminating Ground Loops

There would be no need to eliminate ground loops if "ground" was truly a zero potential reference point. Fast changing currents and finite trace inductance lead to noise voltages in conductors. The key to eliminating ground loops is to identify the reference (ground) traces containing fast changing currents and separating them from the remaining quiet reference traces. Three versions of the same subcircuit are shown in Figures 3, 4, and 5 to illustrate the elimination of noisy references.

In Figure 3, MOSFET current flowing out the COM pin will generate noise voltages in the reference conductor as shown influencing oscillator capacitor C11, bypass capacitors C3 and C5, and feedback network resistor R6. Switching frequency and output voltage variations are two symptoms that can be expected when MOSFET current flows in the reference conductor used by sensitive analog circuitry.

The circuit of Figure 4 indicates ties to a reference plane with "ground" symbols. The high frequency current path is impossible to determine as is the effect on the sensitive analog circuitry.

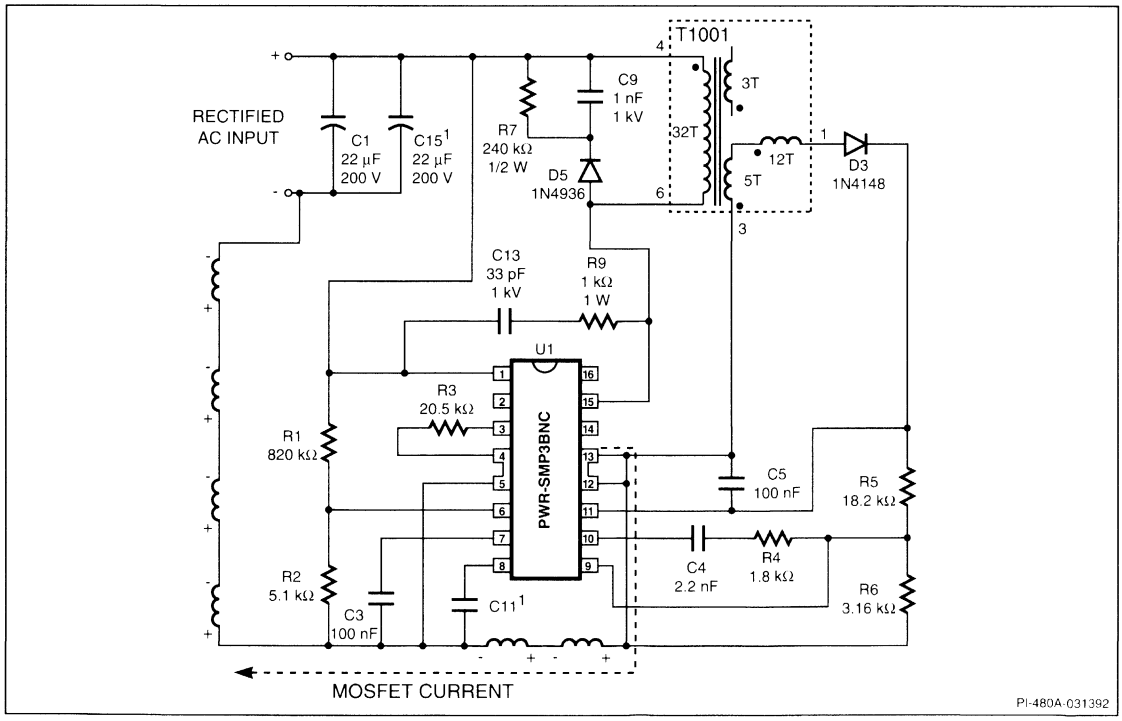


Figure 3. A Noisy Reference Connecting all "Grounds" to a Common Return Via a Long Path.

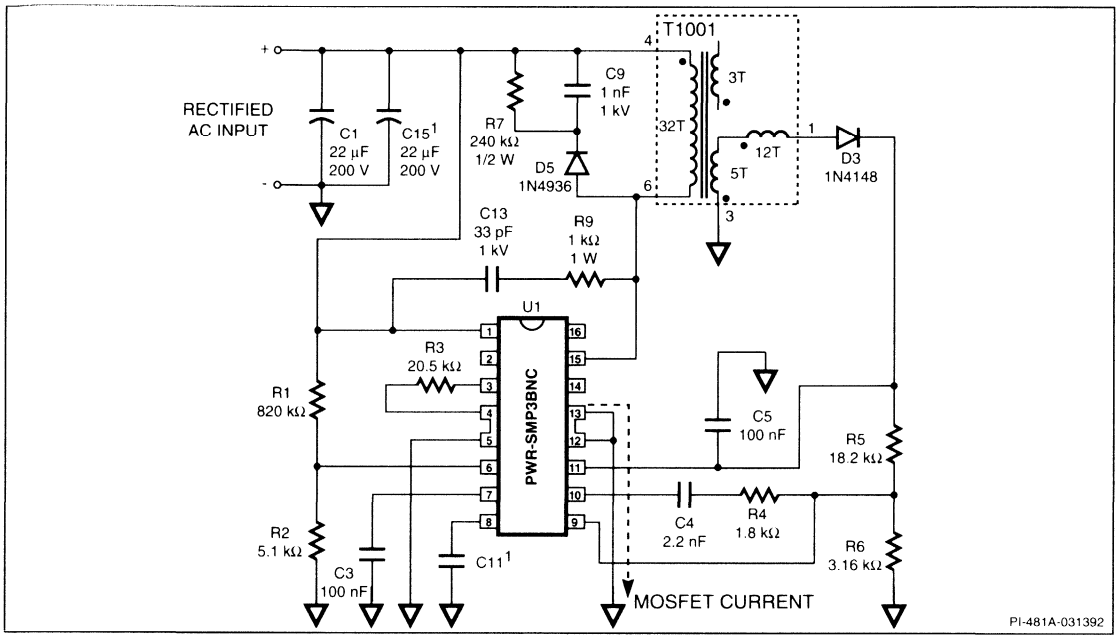


Figure 4. Indeterminate Reference With MOSFET Current Flowing Through Many Different Return Paths.

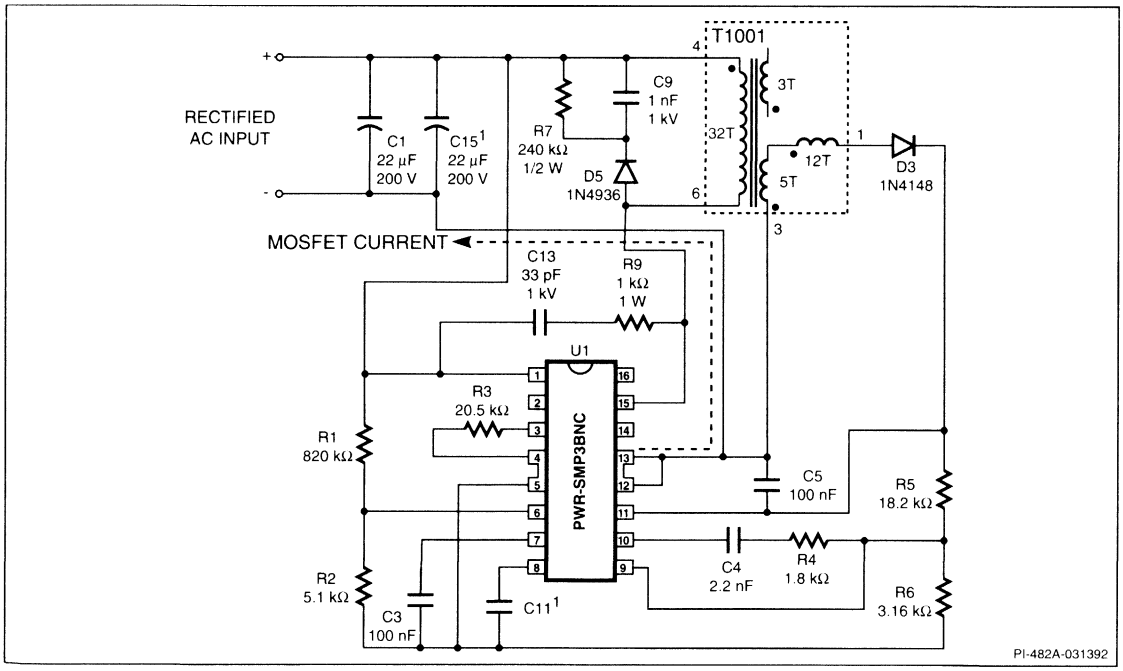


Figure 5. Minimum Noise is Coupled to the Analog Circuitry When a Separate Return is Supplied for the MOSFET Current.

Figure 5 shows that MOSFET current flows directly from COM pins 12 and 13 back to C1 (and C15) without flowing in the reference conductor for the sensitive analog circuitry. The sensitive circuitry has a quiet reference since the "ground loop" has been eliminated.

The COM pins (5, 12, and 13) on the IC are all tied together on the IC but should be carefully connected to properly route current flow. In the absence of a ground plane the return side of all low power analog components (C3, C11, R2, R6, R8) should be returned to pin 5, while the power processing components (C1, C15, D7, D8) should be returned to pins 12 and 13.

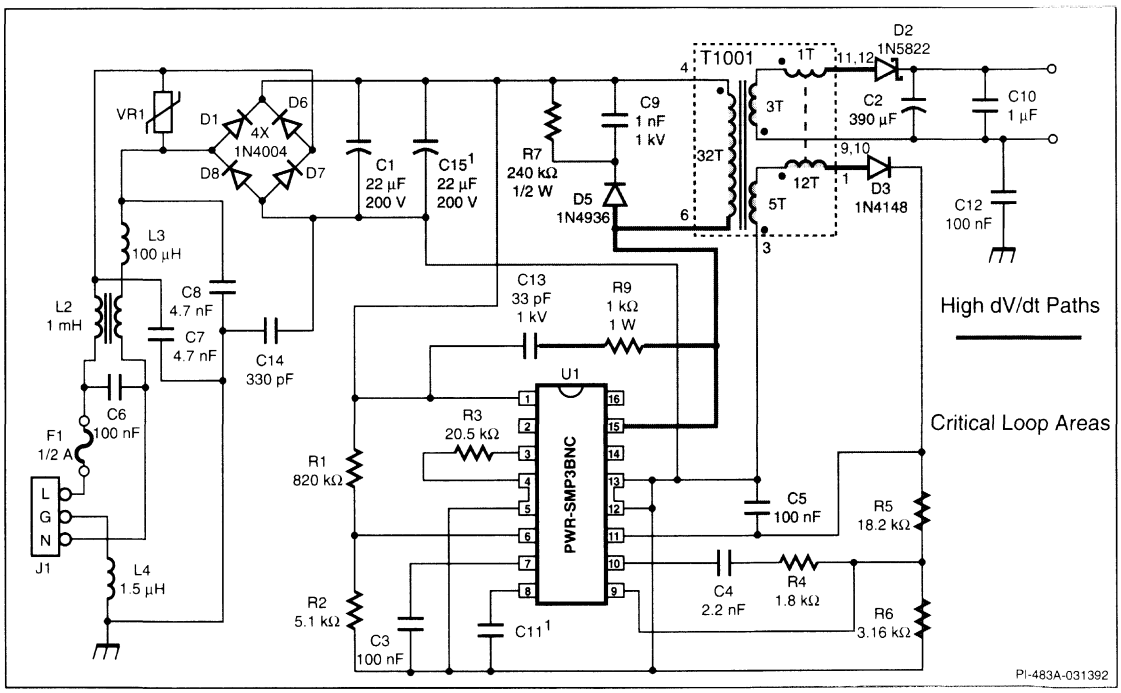


Figure 6. Critical Loops and High Slew Rate Paths.

Minimizing Radiated EMI

Electro-Magnetic Interference (EMI) is generated by any switching power supply. High frequency repetitive waveforms with fast rise and fall times create both conducted and radiated EMI. Conducted EMI is usually controlled with a filter placed between the power supply and the power line. Radiated EMI is heavily influenced by the printed circuit layout. The following guidelines will reduce switching power supply radiated emissions.

Minimizing Loop Area

The area bounded by conductor loops with fast changing currents should be minimized. These loops are shown in Figure 6:

C1+/C15+ → T1 Primary → DRAIN → COM → C1-/C15-
C1+/C15+ → C13→R9→ DRAIN→ COM→C1-/C15-
D5 Cathode → C9 → T1 Primary → D5 Anode
D2 Cathode→ C10→ T1 Secondary (pins 5&6)→ D2 Anode
D3 Cathode → C5 → T1 Feedback (pins 3&4) → D3 Anode

Minimizing Length of dV/dt Conductors

Any component with fast changing voltages can act as an antenna and produce radiated emissions. Minimizing the length of the traces connected to these components reduces these radiated emissions. Some components have a "noisy" side with fast changing voltages and a "quiet" side connected to a supply, reference, or common. Long traces in the "quiet" lead of the component generate less radiated emissions than long traces in the "noisy" lead. For reduced radiated emissions minimize trace length to the following components as shown in Figure 6:

- IC DRAIN (U1 pins 15 and 16)
- T1 primary (pin 6)
- Diode D2 anode
- Diode D3 anode
- Diode D5 anode
- R9
- C15

Reference Planes

Planes can be used to improve grounding, reduce circuit impedance, and provide shielding. Planes should be constructed to route fast moving currents away from sensitive circuitry. There are usually at least two reference planes in each power supply: a power line referenced primary plane and an output referenced secondary plane. The primary plane floats with the rectified AC power line. The secondary plane is isolated from the primary plane and connects to the load.

Typical primary planes are shown in Figure 7. The plane in Figure 7(a) has a "noisy" side and a "quiet" side. Note that the clearance areas around the pads for pins 1, 2, 14, 15, and 16 are much larger to meet creepage distance constraints. The plane in Figure 7(b) is carefully shaped into "noisy" and "quiet" sections with a bottleneck at COM pins 12 and 13 of the IC U1. This approach can be used when fast changing current paths are difficult to identify.

The noisy section of the primary plane should extend beneath C1, C15, C5, C9, C13, D3, D5, R7, R9, primary connected windings of T1 (pins 1, 2, 3 and 4). Feedback winding (T1 pin 3) and C5 tie directly to the "noisy" plane. C5 should be located as close as possible to pins 11 and 12 of IC U1.

The quiet section of the primary plane should extend beneath R1, R2, R3, R4, R5, R6, R8, C3, C4, C11, and IC U1. Pin 5 of U1 should tie directly to the "quiet" section of the primary plane. C3, C11, R2, R6, and R8 should also tie directly to the "quiet" section of the primary plane.

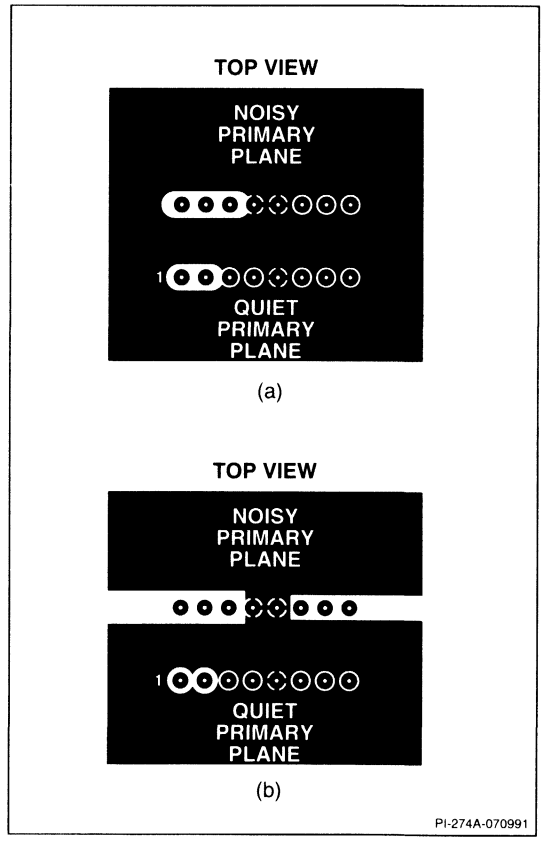


Figure 7. Using Reference Planes to Minimize EMI.

The primary plane should not extend beneath the EMI filter and safety components (F1, C6, C7, C8, C14, L2, L3, L4, VR1) or bridge rectifier diodes (D1, D6, D7, D8) due to creepage distance constraints.

The secondary plane should extend beneath the secondary side of transformer T1 (pins 5 and 6), D2, C2, C10 and C12.

Creepage distance constraints must always be maintained between the primary and secondary planes. Primary traces on one PC board layer should not extend over the secondary plane on the other layer. Secondary traces on one PC board layer should not extend over the primary plane on the other layer.

Shield Box

Suppressing radiated emissions to meet EMI requirements usually requires a "Faraday Cage" which surrounds the equipment in an enclosed conductive container and contains the displacement currents flowing in stray capacitance terms. Figure 8 shows displacement currents with and without a faraday cage. Without the cage the displacement current is free to flow just about anywhere (earth ground, back to the power mains, etc.). The Faraday divides the stray capacitance as shown. Current flow is diverted by the Faraday cage back to the source.

Typical methods include metal enclosures or plastic enclosures with conductive coatings on inside surfaces. Applications that do not have conductive enclosures may require a shield box mounted directly on the power supply over the circuitry generating the radiated emissions. The shield box should enclose C5, C9, C13, D2, D3, D5, R7, R9, T1, U1, and (optionally) C1 and C15. One method uses a drawn can that solders directly to the primary reference plane. The primary and secondary planes should be located on the non component side of the PC board to complete the "faraday cage".

Creepage and clearance distances (discussed later) must be maintained between the primary referenced shield box and both primary and secondary circuitry to meet safety requirements.

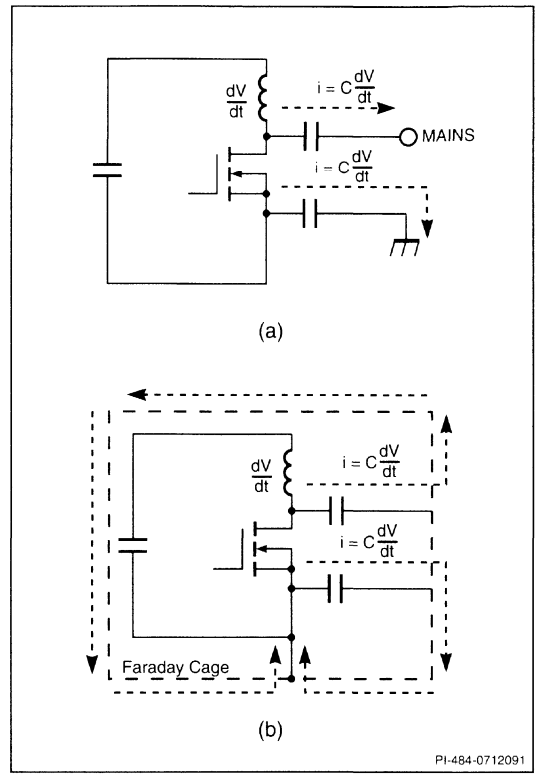


Figure 8. Collecting Displacement Currents with a Faraday Cage.

Minimizing Output Noise

Output noise levels can be minimized with the proper connection to the output filter capacitors. Reducing the effective series impedance of the capacitor is key to achieving the lowest level of output noise. Figure 9 shows two connection strategies for capacitors. The layout in 9(a) simply extends the leads of the capacitor with PC traces to the power bus which introduces additional impedance causing noise levels to increase. The better approach shown in 9(b) bends the power bus to pick up the capacitor connection with the shortest possible leads. This technique provides more of a "Kelvin Connection" to the low impedance filter capacitor.

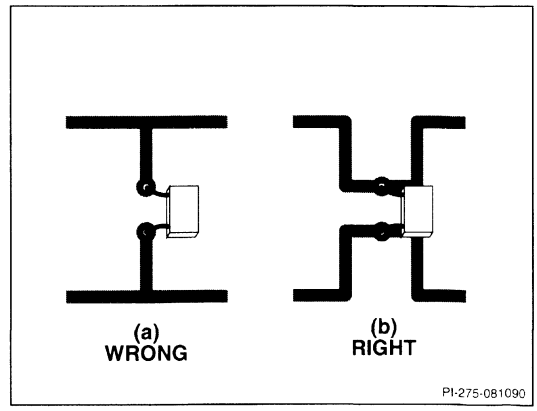


Figure 9. Bending the Bus to Minimize Resistive Effects.

Safety Agency Requirements

The safety agencies (such as Underwriters Laboratories) establish specifications and conduct investigations on materials, devices, products, equipment, constructions, methods and systems with respect to hazards affecting life and property. Printed circuit board conductor spacing is an important design constraint specified by these agencies. The two most important spacings are clearance and creepage distance.

Clearance is the shortest distance between two conductors measured through air. Creepage distance is the shortest path between two conductors measured along the surface of the PC board. Clearance and creepage distances are determined by regulatory agencies such as Underwriters Laboratories (UL) in the United States and the International Electrotechnical Commission in Europe (IEC). (UL requirements are usually quite similar to those of Canada and thus encompass the entire North American market.) Factors which include input voltage, type of equipment, use of equipment, environment, and printed circuit board quality determine the actual clearance and creepage distances required for each application.

The creepage distances shown in the table meet the requirements (Pollution Degree 2, material group IIIa and IIIb) of UL1950 (3-15-89), for North American markets and IEC950 (1989) for European markets for information technology equipment including electrical business equipment. Other specifications may require different limits.

Creepage Distance	U.S. 110-125 VAC	Europe 220-250 VAC
Primary to Primary	1.5 mm	2.5 mm
Primary to Secondary	3.0 mm	5.0 mm

Clearance slots can be used in applications where the desired creepage distance cannot be obtained. For example: primary to secondary creepage distance spacing between T1 pin 4 and T1 pin 5 was impossible to maintain. A slot was used with the appropriate clearance distance from the table shown below (refer to the layout in Figure 13).

The clearance distances shown in the table meet the requirements (Pollution Degree 2) of UL1950 (3-15-89), for North American markets and IEC950 (1989) for European markets for information technology equipment including electrical business equipment. Other specifications may require different limits.

Clearance Distance	U.S. 110-125 VAC	Europe 220-250 VAC
Primary to Primary	1.0(0.7) mm	2.0(1.7) mm
Primary to Secondary	2.0(1.4) mm	4.0(3.4) mm

(The values in parentheses can be used if manufacturing is subject to a formal quality control program. Primary to Secondary isolation must be subjected to 100% electric strength testing in accordance with UL1950 and IEC950).

Primary to primary spacing applies to circuitry on the primary side with voltage levels greater than 50 volts compared to low voltage circuitry on the primary side. The low voltage analog circuitry is considered to be at the same potential and is treated as a group. Figure 11 identifies primary circuitry with voltage levels greater than 50 volts. Primary to primary spacing must be maintained between all traces inside the shaded area as well as between shaded traces and unshaded (low voltage) primary circuitry. Primary to primary spacing must also be applied between all primary circuitry and GND (third wire earth ground).

Primary to secondary spacing applies between all primary and "safe" secondary circuitry. The lighter shading identifies secondary circuitry. Primary to Secondary spacing must be maintained between this circuitry and all primary circuitry.

Special Considerations - Special attention to the following areas will minimize creepage/clearance related problems:

- Examine T1 core creepage and clearance to secondary circuitry. The core is considered to be a conductor.
- Clearance annular ring between high voltage component pads and primary reference plane must meet primary to primary spacing requirements (see plane in Figure 7(a) for example).
- Unused IC pins: use non plated through holes to meet spacing requirements in 220 to 250 VAC applications.

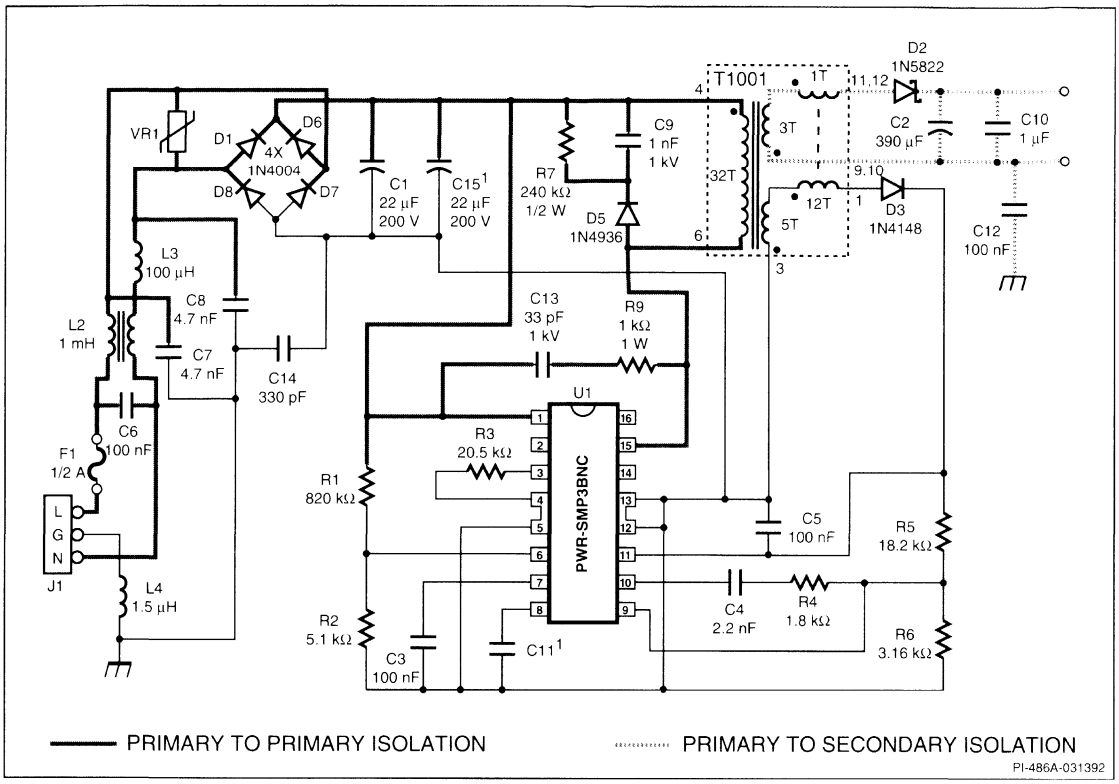


Figure 10. Circuit Paths Which Must be Measured for Primary to Primary and Primary to Secondary Isolation Requirements.

EMI FILTER LAYOUT ISSUES

Filter layout is extremely important to obtain the desired attenuation. Poor layout practice can cause conducted emissions to actually couple around the filter components directly into the AC mains conductors.

Capacitor lead length must be minimized as much as possible to reduce inductance. This includes the traces on the PC board leading up to the capacitor pads. Bend the power bus to pick up capacitor connections as described in Figure 9.

Inductors should be mounted to avoid introducing parallel capacitance. Figure 11 shows the right and wrong way to route PC traces to inductors. Keep the traces well separated to prevent coupling.

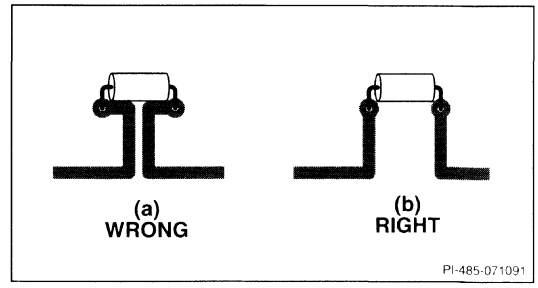


Figure 11. Minimizing Parallel Capacitance When Placing an Inductor on the Board.

Locate differential mode filter capacitor C6 across the AC input conductors as close as possible to the power entry point. Locate common mode filter capacitors C7, C8, and C14 as close to the bridge rectifier as possible.

Maintain appropriate primary to primary creepage and clearance spacing between Hot and Neutral traces of EMI filter.

BREADBOARDING GUIDELINES:

Use ground planes. Copper foil can be added to breadboards that do not have integral ground planes.

Shape and separate planes as required to route currents and maintain isolation.

Do not use solderless breadboards. The techniques discussed here are quite difficult to apply when solderless breadboards are used.

Keep wiring length to a minimum.

Use wire insulated with Teflon. Teflon will not melt when touched with a hot soldering iron. This prevents inadvertent short circuits as breadboarding progresses.

Attach test points for oscilloscope probe connections. This prevents accidental shorts and opens caused by probing the breadboard.

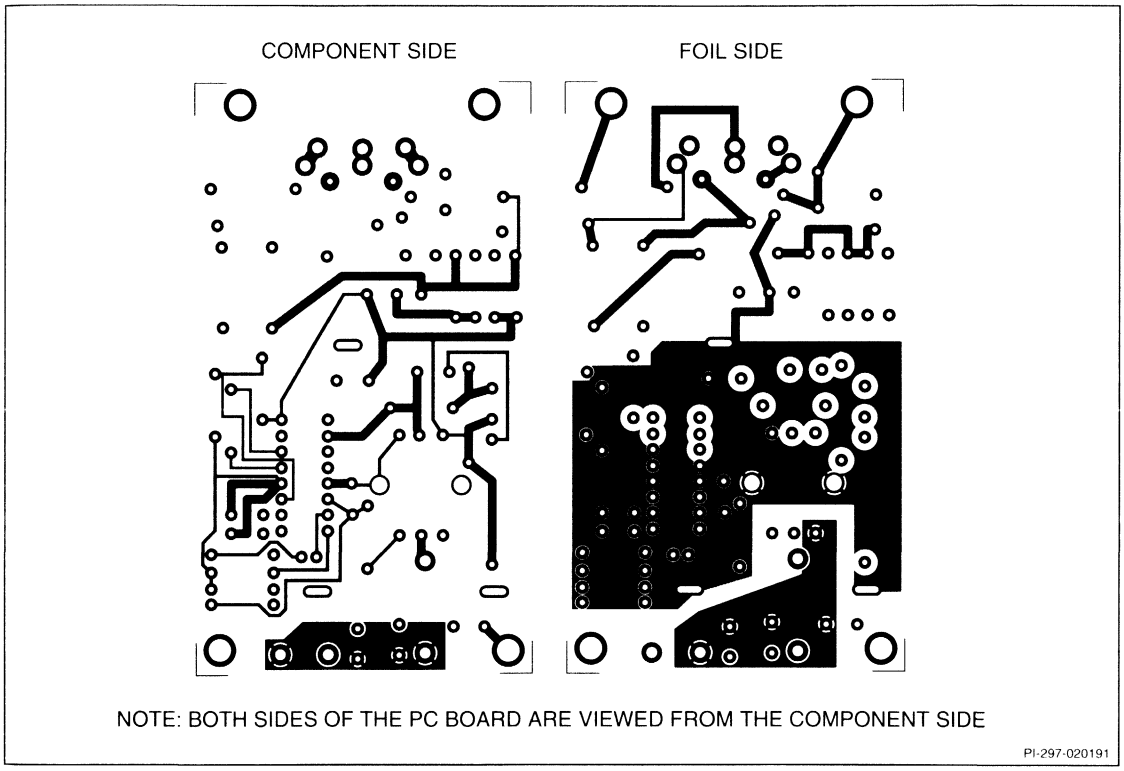


Figure 12. Layout of the PWR-EVAL1 Printed Circuit Board.

Standard Transformers for the PWR-SMP Family

DESIGN AID DA-3

The PWR-SMP family of high-voltage power supply circuits are designed to be used in a flyback configuration. The simplified schematic diagram in Figure 1 shows the key components. The most critical external component in the circuit is the high-frequency flyback transformer. To simplify evaluation and implementation of 5 V power supply designs, a single output standard transformer optimized for each member of the PWR-SMP family is provided here, as well as a list of transformer manufacturers who have worked with Power Integrations to provide these as standard, "off-the-shelf" items.

These standard transformers can also be used as the basis for other "custom" designs based on specific output voltage and current requirements. For more information on customizing transformers for the PWR-SMP family, see AN-7 and AN-9.

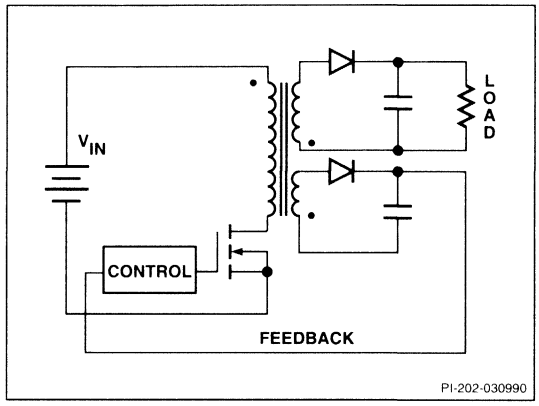


Figure 1. Basic Flyback Converter Circuit.

Basic Flyback Power Transformer

The basic flyback power transformer is shown in Figure 2. Three separate windings and a shield are wound on a common core. The primary winding stores energy in the transformer core. The power secondary winding transfers the energy from the core to the load. The feedback secondary winding provides bias power to the integrated circuit and may also be used for regulation. The shield reduces Electro-Magnetic Interference (EMI).

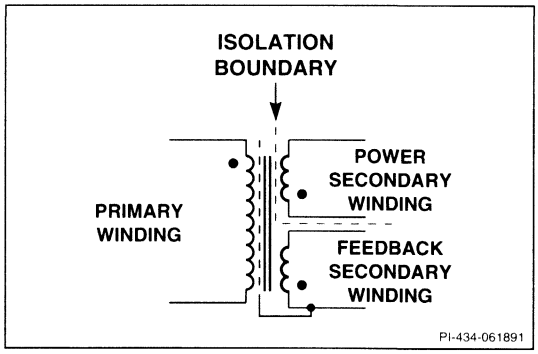


Figure 2. Schematic Diagram of the Three Transformer Windings.

Safety Considerations

Safety agencies such as UL, CSA, VDE, and TUV specify both the electric strength between primary and secondary windings and the minimum distances between primary and secondary windings. Creepage and clearance distance are described in DA-2. All of the standard transformers have been designed to meet the above specifications.

Two construction techniques that provide sufficient primary to secondary insulation for "SELV" (Secondary Extra Low Voltage) rated secondaries use rated insulated wire or margin winding. For single output designs, insulated wire transformers will yield the smallest overall size. No margins are required between the primary and secondary windings for creepage and clearance because the secondary is insulated with UL or VDE rated wire. All windings and the shield cover the bobbin from flange to flange. All four standard transformers are wound using rated insulated wire. (A list of agency-approved wire vendors can be found at the end of this document.)

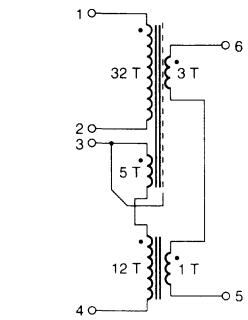
4

TRANSFORMER PART NUMBER	FOR USE WITH	INPUT VOLTAGE	OUTPUT VOLTAGE	ISOLATION VOLTAGE	REGULATION TYPE
T1001	PWR-SMP3BNC PWR-SMP110BNC	85-130 VAC	5 V	2000 V	Feedback Winding
T1002	PWR-SMP120BNC PWR-SMP210BNC PWR-SMP210BNI PWR-SMP210SRI PWR-SMP520BNC	85-265 VAC	5 V	3000 V	Feedback Winding
T1003	PWR-SMP400BNC	36-72 VDC	5 V	2000 V	Feedback Winding
T1004	PWR-SMP120BNC PWR-SMP210BNC PWR-SMP210BNI PWR-SMP210SRI PWR-SMP520BNC	85-265 VAC	5 V	3000 V	Optical Feedback
T1005	PWR-SMP240WTC PWR-SMP260WTC	85-265 VAC	5 V, ±12 V	3000 V	Optical Feedback

Table 1. Standard Transformer General Specifications.

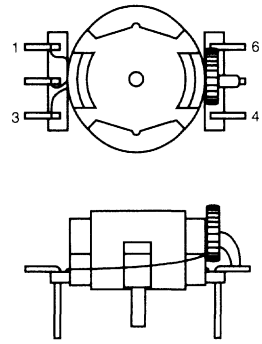
Margin winding is commonly used in transformer construction for switching power supplies operating at frequencies up to 100 kHz and greater than 25 watts. Margin winding requires a barrier of insulation of greater than one half the creepage distance between the end of the magnet wire winding and the edge of the bobbin for successive windings to create a SELV insulation.

Margin winding is the preferred approach for transformers with more than two output voltages of significant power capability. Higher voltage outputs (above 15 volts) are also best served by margin wound transformers.



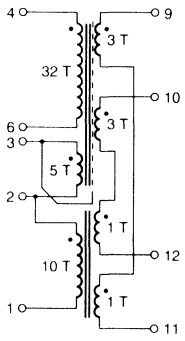
CORE # - B65541-D0100-A033
B65541-D0000-R033

PIN	FUNCTION
1	HIGH-VOLTAGE DC BUS
2	PWR-SMP DRAIN
3	PRIMARY-SIDE COMMON
4	8.5 V FEEDBACK
5	+5 V OUTPUT
6	+5 V RETURN



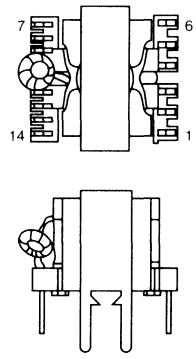
PI-439-062491

Figure 3. T1001 Transformer Pinout and Physical Dimensions[1].



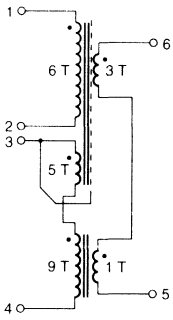
CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
2	N/C
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	PWR-SMP DRAIN
9/10	+5 V RETURN
11/12	+5 V OUTPUT



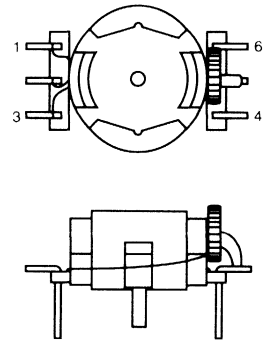
PI-435-061991

Figure 4. T1002 Transformer Pinout and Physical Dimensions[1].



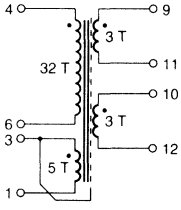
CORE # - P-41408-40

PIN	FUNCTION
1	HIGH-VOLTAGE DC BUS
2	PWR-SMP DRAIN
3	PRIMARY-SIDE COMMON
4	8.5 V FEEDBACK
5	+5 V OUTPUT
6	+5 V RETURN



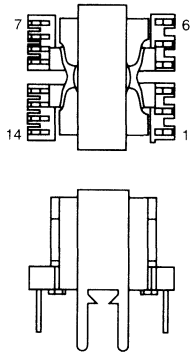
PI-440-062491

Figure 5. T1003 Transformer Pinout and Physical Dimensions[1].



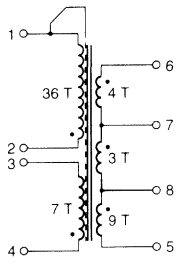
CORE/BOBBIN # - PQ2016

PIN	FUNCTION
1	8.5 V FEEDBACK
3	PRIMARY-SIDE COMMON
4	HIGH-VOLTAGE DC BUS
6	PWR-SMP DRAIN
9/10	+5 V RETURN
11/12	+5 V OUTPUT



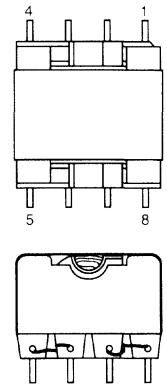
PI-438-062091

Figure 6. T1004 Transformer Pinout and Physical Dimensions[1].



CORE/BOBBIN #
FQK2522-T11-255-2500B2

PIN	FUNCTION
1	HIGH-VOLTAGE DC BUS
2	PWR-SMP DRAIN
3	PRIMARY-SIDE COMMON
4	V_{BIAS}
5	-12 V OUTPUT
6	+12 V OUTPUT
7	+5 V OUTPUT
8	RETURN



PI-694-031692

Figure 7. T1005 Transformer Pinout and Physical Dimensions[1].

Pulse Transformer Considerations

Three of the four standard transformers include a coupled inductor or pulse transformer. The pulse transformer improves the load regulation for the feedback winding approach (discussed in AN-8). The pulse transformer is combined with the power transformer in a single unit. Overall cost is less and the electric strength requirement can be verified with a single test by the transformer vendor.

Standard Transformer Vendors

The following vendors have submitted samples which have been tested and characterized specifically for use with the PWR-SMP Family of products. Standard transformers developed to date are given in Table 1.

The T1001, T1002, and T1003 are designed to use the feedback winding regulation technique, and include the integrated coupled inductor. The T1004 and T1005 have been designed for use with optically-isolated feedback, which does not require a pulse transformer.

- AT&T Microelectronics
  Transformer and Inductor Group
  3000 Skyline Drive
  Mesquite, TX 75149
  (800) 372-2447

- Datatronics
  28151 Highway 74, Box 1579
  Romoland, CA 92380
  (714) 928-7700

- Delta Electronics, Inc.
  9th Floor, Asia Enterprise Center
  144, Section 3
  Min Chuan E. Road
  Taipei 104
  Taiwan, R.O.C.
  (02) 7164822

- Inductor Supply
  1849 West Sequoia Avenue
  Orange, CA 92668
  (800) 472-8421 (800) 854-1881 (in CA)

- Renco Electronics, Inc.
  60 Jeffryn Boulevard, East
  Deer Park, NY 11729
  (800) 645-5828

- Tokin Magnetics, Inc.
  1100 Fulton Place
  Fremont, CA 94539
  (415) 490-7500

- Tokin
  Tohoku Metal Industries, Ltd.
  Haxama Building, 5-8
  2-chome, Kita-aoyama
  Minato-ku, Tokyo 107
  Japan
  (03) 402-6166

Agency-Approved Wire Vendors

For 120 VAC Applications (UL1430 Wire)

- Weico Wire & Cable
  161 Rodeo Drive
  Edgewood, NY 11717
  (516) 254-2970

For 240 VAC Applications (Triple Insulated Wire)

- Rubudue Wire Company, Inc.
  11080 Rose Avenue
  Fontana, CA 92335
  (714) 357-0151

References

1 Transformer physical outline drawings courtesy AT&T Microelectronics, Transformer and Inductor Group

EMI Filter Design for the PWR-SMP Family

DESIGN AID DA-4

Switching power systems have many advantages over traditional linear approaches including smaller size, lower weight, and improved efficiency. However, successful implementation of a switching power system requires careful attention to the area of Electromagnetic Interference (EMI). EMI refers to the radio frequency energy, either conducted or radiated, emitted from electronic equipment. EMI filter design is an important part of switching power system development, as proper design of the EMI filter allows both conducted and radiated emissions to be reduced to acceptable levels.

This application note will be directed at power systems operating directly from 120 or 240 volt AC mains, but is also relevant for DC input applications such as telecommunications systems. Example specifications and basic conducted emissions testing are briefly discussed. Ideal and non-ideal filter component characteristics are explored. Critical circuit waveforms in flyback power supplies which lead to normal-mode and common mode conducted emissions are identified. Normal-mode and common-mode LC section filters are analyzed. Typical examples of different EMI filters for flyback power supplies are given, along with examples of practical layout and test procedures.

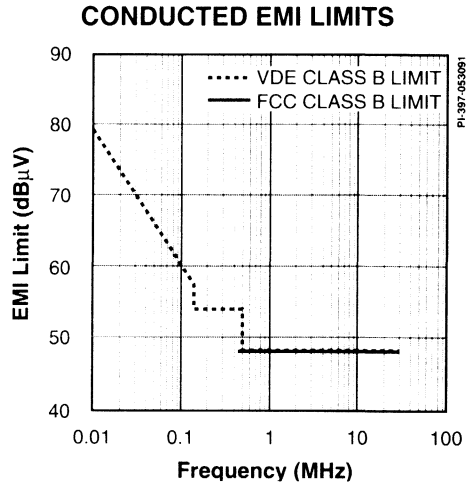


Figure 1. Current VDE and FCC Maximum Limits for Conducted EMI.

Testing

Specifications

EMI specifications vary from country to country, product to product, and also change over time. The applicable EMI specification must be identified for the intended product family and target market. The Federal Communications Commission (FCC) regulates EMI specifications for the American market, and Canadian specifications are similar to FCC specifications. However, it is important to note that the situation is very different in Europe.

Each European country currently has its own set of EMI regulations. Presently, the International Special Committee on Radio Interference (CISPR) and International Electrotechnical Commission (IEC) develop and recommend specifications which may, or may not, be adopted by each country[1]. The twelve- member European Community is proceeding toward a unified EMI specification. However, until a unified specification is in place, the conservative approach is to design for the most stringent requirements, which is the VDE specification in Germany. Figure 1 compares the conducted emissions limits governed by FCC rules, Part 15, subpart J with the limits specified by VDE for electronic data processing equipment [2].

Safety specifications must also be considered in the EMI filter design, since the filter is applied directly across the AC power mains. Two key safety specifications are IEC950 and UL1950 for business and data processing equipment. IEC950 is the "harmonized" safety specification for the twelve member countries of the European Community. UL1950 is a relatively new safety specification from Underwriters Laboratories that harmonizes the European community requirements with those of the American market.

Measuring Conducted Emissions

Details of testing apparatus and methodology are governed by the various EMI specifications, but share the same general concept. Conducted emissions measurements are made with a Line Impedance Stabilization Network (LISN). Figure 2 shows that inside the LISN is a filter represented by L_F and C_F. This filter forces emission currents to flow through coupling capacitor C_C and sense resistor R_S. Instrumentation reads the emissions level as a voltage across R_S.

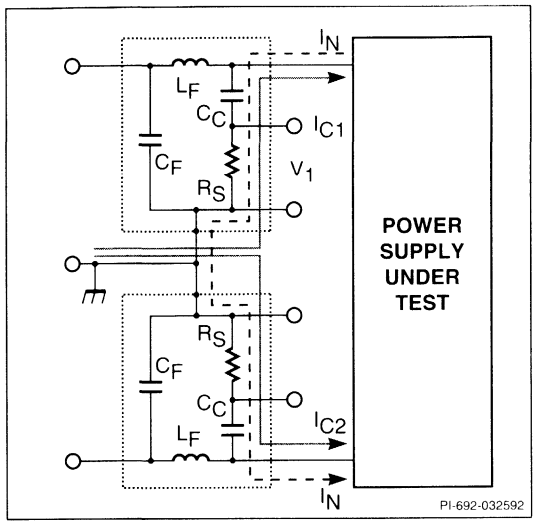


Figure 2. LISN Test Configuration.

Normal-mode conducted emissions are caused by currents circulating from one AC lead through the power supply to the other AC lead (such as I_N). During testing, normal-mode current I_N flows through both LISNs and back to the power supply. Normal-mode emissions will generate test voltages equal in magnitude and opposite in phase across each of the LISN sense resistors.

Common-mode conducted emissions are caused by currents which do not circulate between the AC leads and may or may not be related (such as I_{C1} and I_{C2}). Common-mode current I_C flows between the power supply and earth ground. Common-mode emissions will generate voltages with different magnitudes and phase relationships across each of the LISN sense resistors.

Filter Components

EMI filters are actually simple combinations of inductors and capacitors. Series resistors, which lead to undesirable power dissipation, are not normally used.

Single-section EMI filters (one common-mode, one normal-mode section) take the least space and have the lowest cost but require careful attention to details such as circuit parasitics, component parasitics, and layout. Multiple-section filters are widely used because one stage can be designed to overcome the deficiencies of the other. The resulting design may meet the specification but may not address size or cost goals of the end product. Understanding the basics of EMI filter design and application allows the designer to implement small, low cost, single section EMI filters.

Capacitors

Proper capacitor selection for EMI filters requires attention to three key parameters: impedance characteristics, voltage ratings, and safety specifications.

Figure 3 shows the impedance characteristic for both ideal and non-ideal capacitors. An ideal capacitor has an impedance characteristic that decreases linearly with frequency. A real capacitor has parasitic inductance and resistance elements which cause the impedance to behave quite differently from an ideal capacitor.

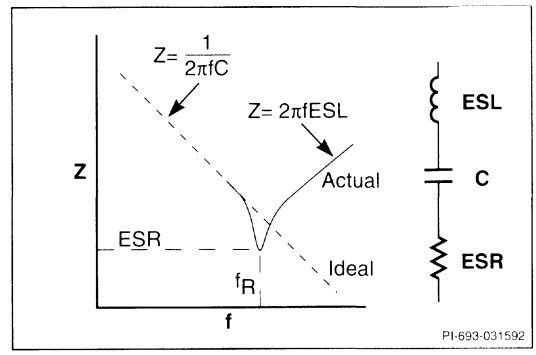


Figure 3. Comparison of Ideal and Real Capacitor Impedance.

Equivalent series inductance (ESL) creates a capacitor self resonant frequency f_R as shown on the plot. The impedance of the capacitor at this self-resonant frequency is determined by equivalent series resistance (ESR). Beyond the self-resonant frequency (f_R), the capacitor actually acts like an inductor. Capacitors with plastic film, combination plastic film/paper, or ceramic dielectrics usually have the highest self-resonant frequencies and are commonly used in EMI filters. Aluminum electrolytic capacitors impedance is also important in the development of EMI filters.

Typical impedance characteristics for three different AC rated capacitors are shown in Figure 4. Two X-type capacitors from different manufacturers are compared. Note that the 1 µF capacitor has lower impedance at low frequency but resonates at approximately 2.5 MHz. The 0.1 µF capacitor has higher impedance at low frequency but maintains lower impedance than the larger part above 6 MHz. Installing the larger component to improve low frequency attenuation may actually cause higher frequency components to pass through and exceed the specification at a different frequency. The impedance for a 4700 pF Y-type capacitor is also shown. Note that the Y capacitor impedance characteristic is almost ideal with no resonance behavior below 40 MHz.

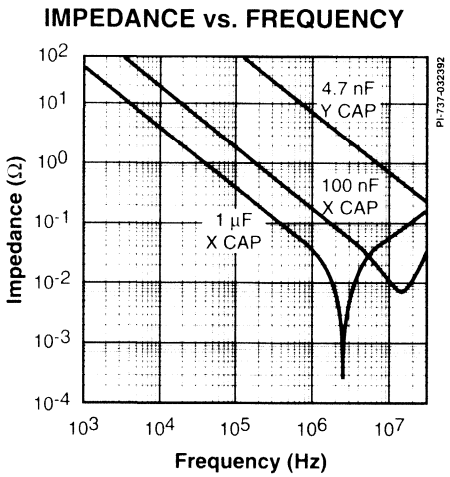


Figure 4. Impedance Plots of Various AC Capacitor Types.

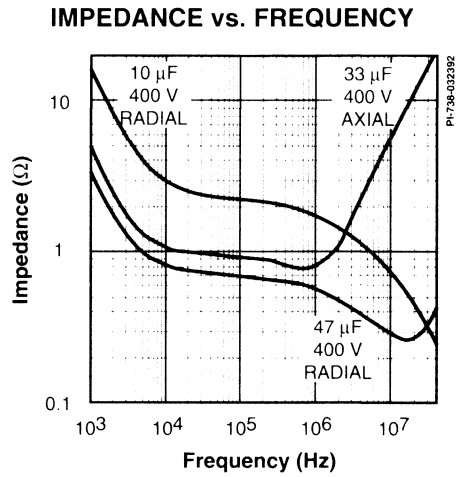


Figure 5. Impedance Plots of Aluminum Electrolytic Capacitors.

Typical impedance characteristics for three different aluminum electrolytic capacitors are shown in Figure 5. Two capacitors employ radial terminations with both leads coming out the same side of the can. Installing radial capacitors on end shortens the lead length and inductance which improves the frequency response. The axial capacitor always has a total lead length of at least one can diameter, leading to longer effective leads and higher equivalent series inductance (ESL). The two radial capacitors have an impedance characteristic that stays low out to almost 40 MHz, while the axial capacitor becomes inductive at 1 MHz. Note that above 3 MHz, the smaller radial capacitor actually has lower impedance than the larger axial capacitor. The impedance of the input aluminum electrolytic capacitor provides the first level of normal-mode filtering (which will be discussed later), and must be minimized.

Reliable operation requires selection of capacitors with proper voltage ratings. For operation directly across the AC mains capacitors with AC ratings should be chosen. Steady state and transient voltage limits should be taken into account. Capacitors with plastic film, combination plastic film/paper, or ceramic dielectrics are available with sufficient voltage ratings for AC operation.

Safety requirements vary from country to country but the basic concepts are the same. Capacitors that are applied directly across the AC mains must withstand specified levels of transient overvoltage surge conditions without creating a safety hazard (fire or electrical). These capacitors are usually denoted as X-type (and can be broken down even further to X1 and X2 depending on surge voltage rating).

Capacitors applied between either of the AC mains conductors (Line or Neutral) and the protective earth ground must survive a higher transient over voltage surge condition. These capacitors (usually denoted as Y-type) have an additional constraint on the maximum value of capacitance to limit the amount of current that could flow in the event of a broken earth ground connection.

Inductors

Proper inductor selection for EMI filters requires attention to three key parameters: the impedance characteristic, current rating, and surge current capability.

Figure 6 shows the small-signal impedance characteristic for both ideal and non-ideal inductors. Ideal inductors have an impedance characteristic that increases linearly with frequency. Real inductance have parasitic resistance R and interwinding capacitance (C_W). C_W creates a resonant frequency as shown on the plot. The impedance reaches a peak value equal to the winding resistance R. Beyond the resonant frequency (f_R), the inductor actually behaves like a capacitor.

Peak voltage rectification circuits draw a large pulse of current at each peak of the AC mains voltage. The inductor usually has a minimal effect on the peak value of the surge current, but must survive it. Note that the peak mains current will increase with the size of the energy storage capacitor and is highest when the AC mains voltage is first applied, as shown in Figure 7. The fusing current of the inductor is tested when the mains are turned on and surge limiting devices are disabled and must be greater than the rating of the safety fuse. Another alternative is to specifically design the inductor to function as a fuse at the appropriate current level.

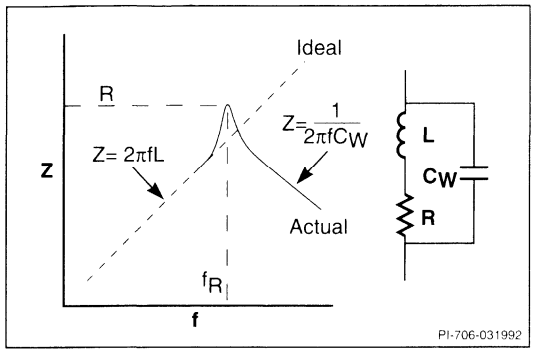


Figure 6. Comparison of Ideal and Real Inductor Impedance.

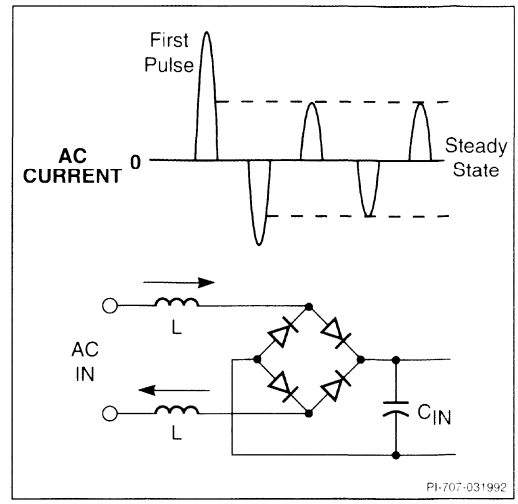


Figure 7. Input Current Waveform.

Normal-mode Inductors

Normal-mode inductors are usually wound on toroidal or solenoidal cores of either iron powder or ferrite material with single layer windings, as shown in Figure 8. These types have the lowest capacitance and highest resonant frequency.

The effective inductance varies with the current flowing through the inductor. Figure 7 shows a simple example with a rectifier and filter creating a high voltage DC bus from the AC line. Current flow is blocked by the bridge rectifier when the instantaneous AC input voltage is not near the peak. Input current flows only during a small portion of the input voltage waveform. The average value of the input current must be high enough to deliver sufficient power for the load and power system losses. Consequently, the peak current during normal operation is quite high as discussed previously. Inductors must be designed or selected with this peak current in mind. Figure 9 shows how inductance for a powdered iron toroidal core varies with number of turns and bias current. To achieve the desired inductance under high current bias, higher numbers of turns and/or larger inductor cores are normally required.

Typical impedance characteristics for two different inductors are shown in Figure 10. Note that the larger inductor resonates at a lower frequency and becomes capacitive. The smaller inductor actually has a higher impedance above 3 MHz due to the higher self-resonant frequency. Installing the larger inductor to attenuate the fundamental may have the effect of letting through current components above 3 MHz.

Balun Inductors

Balun inductors consist of two identical windings wound such that the magnetic fields caused by normal-mode currents cancel. Figure 11 shows one physical implementation and the schematic symbol for a balun inductor. Three currents, I_1, I_2, and I_3 are also indicated. I_1 is a "normal-mode" current which circulates

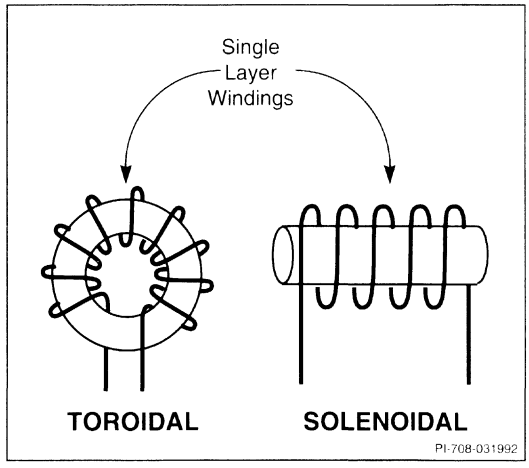


Figure 8. Typical Normal-mode Inductor Shapes.

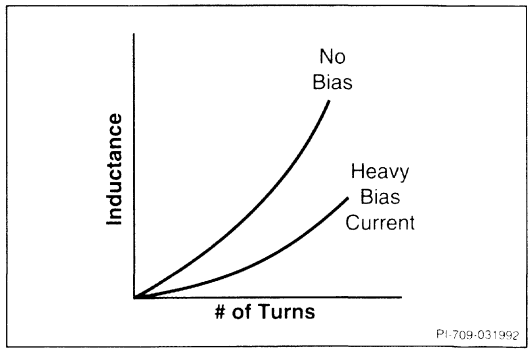


Figure 9. Variation of Inductance with Inductor Current.

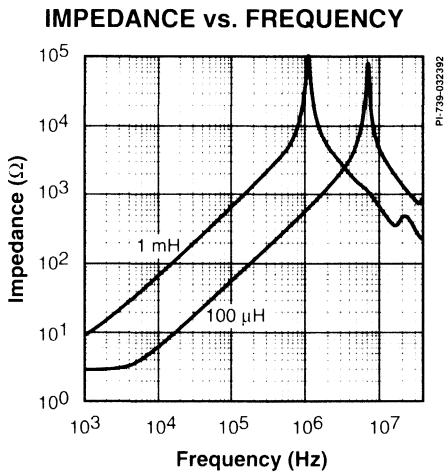


Figure 10. Impedance Plots of Various Inductor Types.

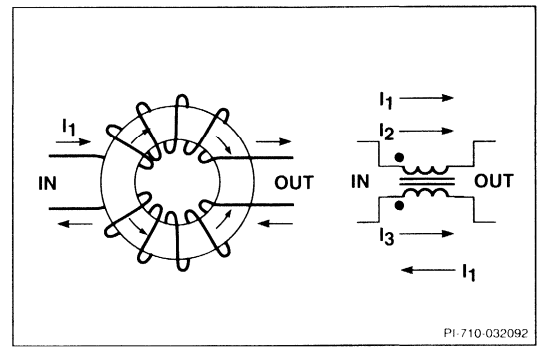


Figure 11. Balun Inductor Construction and Schematic Symbol.

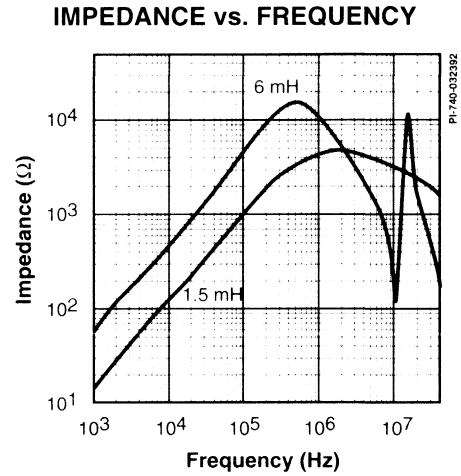


Figure 12. Impedance Plots of Various Baluns.

through one winding in one direction and through the other winding in the opposite direction. The magnetic fields within the core due to current I_1 cancel perfectly because of dot polarity and the equal number of windings. Note that the "start" of both windings enters the core on the same side and the "finish" of both windings leaves the core on the other side. Toroids, U cores, and E cores are the most commonly used shapes. Single layer windings on high permeability magnetic materials such as ferrite work best. Multiple sections or stages are used when a single layer winding cannot deliver enough inductance. Balun inductors behave like short circuits for normal-mode currents such as I_1 which flow out one winding and come back through the other. I_2 and I_3 are "common-mode" currents which may or may not be related in magnitude and phase. The balun behaves like an inductor to common-mode currents.

The balun must survive the surge current occurring when voltage is first applied to the power supply as described earlier, as well as operate at the steady-state RMS input current.

Typical impedance characteristics for two different balun inductors are shown in Figure 12. The smaller balun was wound with a single layer winding while the larger balun was wound with two layers. Note that the impedance of the larger balun peaks at 600 kHz and becomes capacitive. The smaller balun actually has higher impedance above 3 MHz and will attenuate common-mode noise better. Note also the multiple resonant terms at 10 MHz caused by multiple windings. Installing the larger balun to improve low frequency common-mode attenuation may actually cause higher frequency components to couple through and exceed the specification, especially in the 10 MHz range.

Flyback Power Supply EMI Signature

4

Flyback power supplies have a distinctive EMI signature that can be attributed to the superposition of several waveforms shown in Figure 13. The drain current, drain to source voltage, diode voltage, and diode current waveforms can each generate emissions which may exceed the desired EMI specifications if care is not taken.

Switch Drain Current

Drain current begins to flow when the MOSFET switch is turned on. The current ramps to a peak value determined by input voltage, primary inductance, switching frequency, and duty cycle. This trapezoidal waveform is characterized in the frequency domain by a spectrum with a fundamental at the switching frequency and harmonics determined by the relative

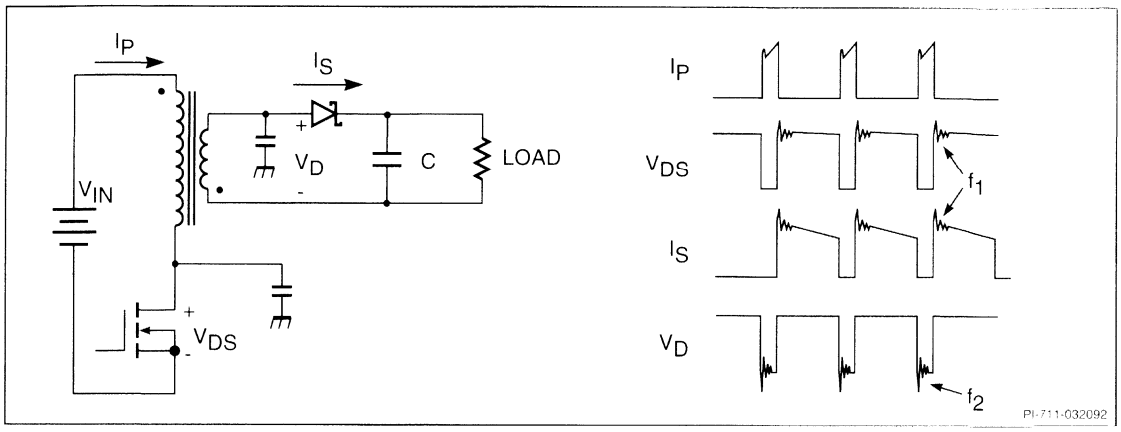


Figure 13. Examples of Noise-inducing Waveforms in a Typical Flyback Power Supply.

squareness of the waveform. This normal-mode current will circulate between the mains and the power supply if not properly filtered.

The drain current waveform causes spectral energy in the form of normal-mode emission currents to be concentrated at the switching frequency and related harmonics. This current waveform can also create radiated magnetic fields if the current path defined by the PC board layout encircles a large physical area.

Switch Drain-Source Voltage Waveform

The drain-source voltage waveform is characterized by high dV/dt transitions containing significant energy. Parasitic circuit elements (leakage inductance, MOSFET output capacitance, and transformer capacitance) cause additional voltage peaking and ringing at frequencies typically between 3 and 8 MHz. The drain of the power switch, transformer primary, and any other components connected to this node will radiate electric fields (similar to a transmitter driving an antenna), creating capacitive displacement currents flowing through ever present stray capacitance. This displacement current couples into whatever path is necessary (including either the mains line, neutral, or ground) to return to the driving node. The displacement currents generated by the drain voltage waveform cause spectral energy in the form of a common-mode conducted emission to be concentrated at the switching frequency and resonant frequency of the indicated ringing voltage waveform.

Diode Voltage Waveform

The diode voltage waveform is also characterized by large voltage changes and fast rise and fall times. Parasitic circuit elements (transformer leakage inductance and diode capacitance) cause additional voltage peaking and ringing at frequencies typically between 20 and 30 MHz. The diode voltage waveform will radiate electric fields (just like the MOSFET drain-source voltage) creating displacement currents seeking a return path. The displacement currents generated by the diode voltage waveform cause spectral energy in the form of a common-mode emission current to be concentrated at the switching frequency and resonant frequency of the indicated ringing voltage waveform.

Diode Current Waveform

Diode current begins to flow as soon as the MOSFET switch is turned off. The current starts at a peak value and decreases linearly at a rate determined by secondary inductance and output voltage. This trapezoidal waveform is characterized in the frequency domain by a spectrum with a fundamental at the switching frequency and harmonics determined by the relative squareness of the waveform. Additional ringing superimposed on the waveform is related to the drain source voltage waveform previously discussed. This composite current waveform can cause significant magnetic fields to radiate if the current path defined by the PC board layout encircles a large physical area. Spectral energy in the form of a common-mode emission current would be concentrated at the switching frequency and resonant frequency of the indicated ringing current waveform.

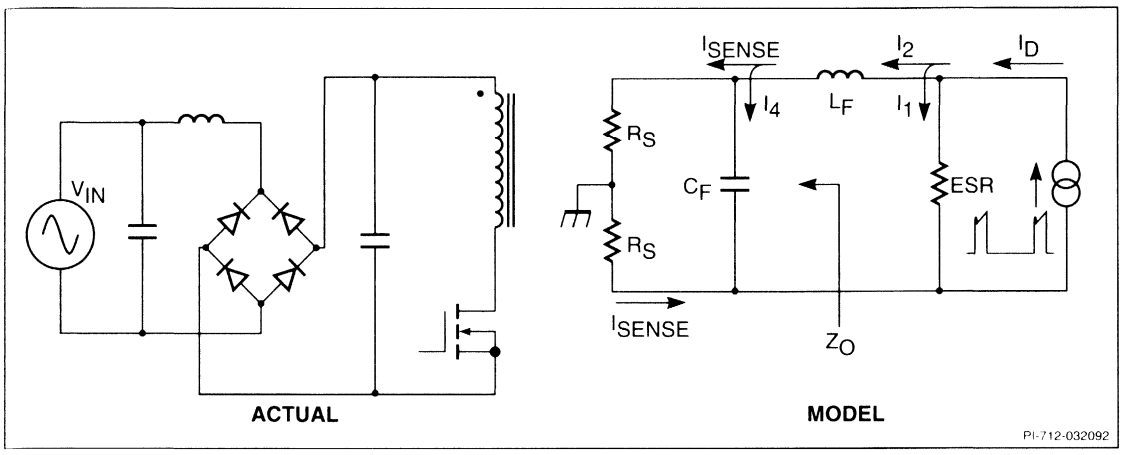


Figure 14. Power Supply Input Section with a Normal-mode Filter and Its Impedance Model.

Suppression Techniques

Controlling EMI requires attention to the following areas. Each will be discussed in detail:

- Normal-mode filtering
- Common-mode filtering
- High frequency return path to primary circuitry
- Power transformer shielding, gapping, and core connection
- Power cord damping

Normal-mode Filter Analysis

Normal-mode analysis starts by replacing the actual circuitry with an equivalent model, as shown in Figure 14. The trapezoidal drain current is modeled by current source I_D. The effective impedance of energy storage capacitor C1 is represented by ESR. The bridge rectifier is assumed to be conducting current and is replaced with a short circuit. The AC source impedance is modeled by the effective series combination of the 50 Ω LISN sense resistors. Normal-mode filtering is performed by the LC filter. This model is valid up to roughly 1 MHz.

The first analysis step is to estimate the magnitude of the current at the fundamental of the switching frequency. The fundamental can be found from the following equation where I_{PK} is the peak current, n is the harmonic (n = 1 for fundamental), D is the duty cycle, t_R is the rise time, and T is the period. The envelope of the harmonics as a function of frequency is shown in Figure 15.

$$I_D = 2I_{PK} \times D \times \frac{\sin(\pi n \times D)}{\pi n \times D} \times \frac{\sin\left(\pi n \times \frac{t_R}{T}\right)}{\pi n \times \frac{t_R}{T}}$$

At the switching frequency f_S, I_D flows through ESR, since the output impedance of the normal-mode filter (L_1, C_1) must be much higher than ESR's impedance. An effective voltage source is created across ESR by I_D flowing through the ESR impedance as shown in Figure 16. The difference between the magnitude of this voltage in microvolts and the desired conducted emissions specification determines the attenuation required of the normal-mode filter. The voltage transfer function H(s) is given in terms of L_1, C_1, and R_S. The denominator of H(s) is

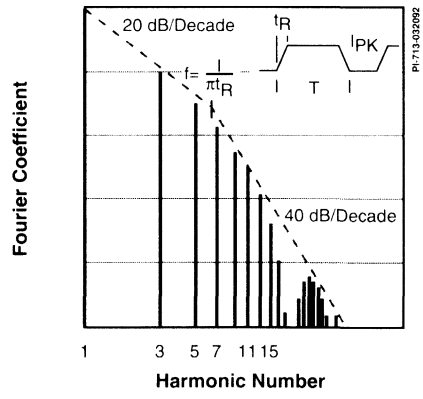


Figure 15. Envelope of Fourier Spectrum.

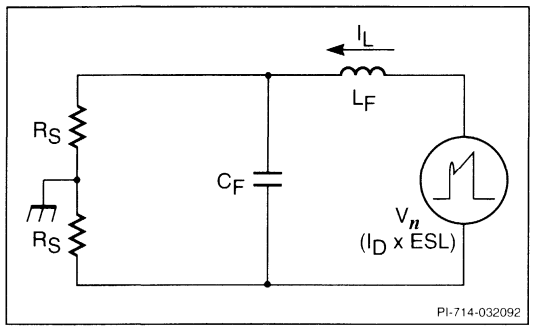


Figure 16.

dominated by the frequency dependent terms at the switching frequency and can be simplified as shown below. Rearranging this equation leads to an easily interpreted form. The effective input voltage V_D is converted to a current by inductor, split by the impedance divider R_S and C_F, and then converted back into the measured sense voltage by R_S.

$$H(s) = \frac{V_O}{V_D} = \frac{1}{\left(L_F C_F s^2 + \frac{L_F s}{2R_S} + 1\right)}$$

$$H'(s) = \frac{V_O}{V_D} = \frac{1}{\left(L_F C_F s^2 + \frac{L_F s}{2R_S}\right)}$$

$$V_O = V_D \times \frac{1}{L_F s} \times \frac{1}{\left(2R_S + \frac{1}{C_F s}\right)} \times R_S$$

Component selection starts by identifying a target sense voltage V_{SENSE} below the specification limit at the fundamental frequency. This voltage is converted into a total RMS current I_1. Il is then used to calculate the value of the inductor.

$$I_1 = V_{SENSE} \times \sqrt{\left(\frac{1}{2 \times R_S}\right)^2 + 2\pi f s C_F^2}$$

$$L_F = \frac{V_D}{2\pi f s \times I_1}$$

Note that different combinations of L and C are possible and that the LC product tends to remain the same. The inductor and capacitor can be selected to optimize the filter for either cost or size.

Peak load current normally limits the size of the inductor to between 100 µH and 1 mH (especially in mains applications with peak-charging capacitive input filters). Typical normal-mode filters have relatively large values of across-the-line capacitance (47 to 470 nF). Refer to the appendix for an example normal-mode filter calculation.

For balanced impedance, the single inductor should be replaced by two inductors of half the value installed in series with each mains line as shown in Figure 17.

Filter effectiveness decreases as parasitic elements of the filter components themselves become significant. The effective circuit model above 1 MHz is shown in Figure 18. Note the additional ESL terms in both the energy storage capacitor and the filter capacitor. Note also the shunt winding capacitance C_W across the filter inductor. As the frequency increases, the parasitic components begin to dominate, reducing filter effectiveness. Fortunately, the harmonics of the trapezoidal current source waveform are also decreasing above 1 MHz, which tends to offset the degradation in filter performance. Excursions above the required conducted emissions limit in this frequency range are usually due to the ringing waveforms identified earlier and resonances caused by parasitic components themselves.

Physical component layout becomes increasingly critical above 1 MHz. Improper layout can lead to increased capacitor ESL. It is also possible for noise voltages to couple around the EMI filter directly into the mains.

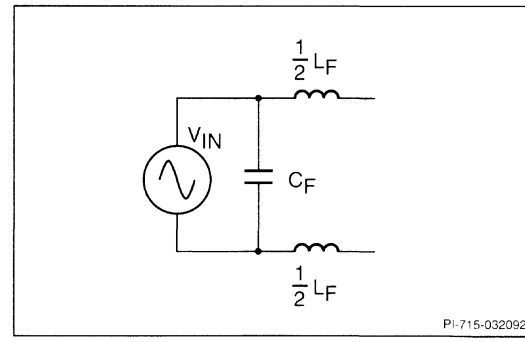


Figure 17.

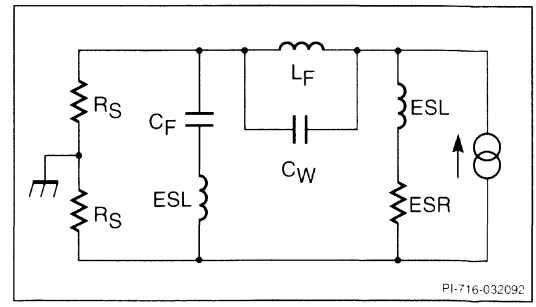


Figure 18. High-frequency Model of the Normal-mode Filter.

Common-mode Filtering

Common-mode filters require relatively high values of inductance since safety specifications limit the size of the common-mode capacitors to typically less than 10 nF. Safety specifications such as UL1950, UL544, and IEC950 limit the amount of fault current that can flow when a safety ground connection has been opened. A typical measurement example showing the placement of the safety capacitors is shown in Figure 19.

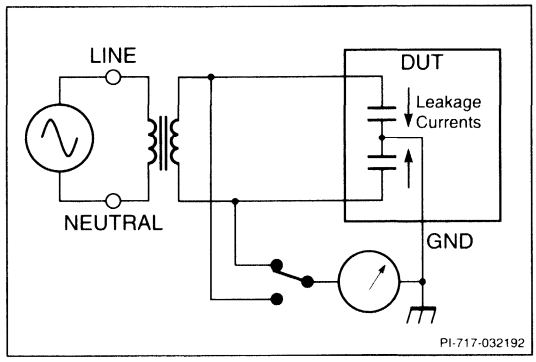


Figure 19. Typical Safety Measurement Setup.

The maximum safety capacitor size is a function of leakage current I_{LKE}, mains voltage V_{RMS}, and line frequency f_{LINE}. For 500 µA leakage current at 250 VAC and 60 Hz, C is limited to a maximum value of 5.3 nF. For a 3.5 mA leakage current at the same input conditions, the maximum C is 37 nF. Lower values must then be selected because of capacitor tolerance.

$$C = \frac{I_{LKE}}{2\pi \times f_{LINE} \times V_{RMS}}$$

Balun inductors are commonly used since the high inductance normally required (500 µH to 5 mH or higher) is unaffected by the circulating normal current. Inductors can also be used in some lower power applications if the peak current is taken into account.

Common-mode analysis starts by replacing the actual circuitry with an equivalent model as shown in Figure 20. Displacement currents through stray and interwinding capacitance are replaced by current source I_C referenced to ground. Energy storage C1 has no effect on common-mode emissions and is replaced by a short circuit. The bridge rectifier is treated as a short circuit to conducted emissions and is also removed. The AC source impedance is modeled by the effective series combination of LISN sense resistors with the common point connected to ground. This model is valid up to roughly 1 MHz. The effects of circuit and component parasitics dominate filter behavior above 1 MHz.

Common-mode emissions are difficult to model accurately if the stray capacitance is not known. This stray capacitance is heavily dependent on the circuit layout and transformer construction. An empirical approach is normally used requiring a working power supply breadboard with a normal-mode filter. Refer to the appendix for a sample common-mode filter calculation.

Filter effectiveness decreases as parasitic elements of the filter components themselves become significant. The effective circuit model above 1 MHz is shown in Figure 21. Note the additional ESL term in both the filter capacitors and shunt winding capacitance C_W across the balun inductor. With increasing frequency the parasitic components begin to dominate, reducing filter effectiveness.

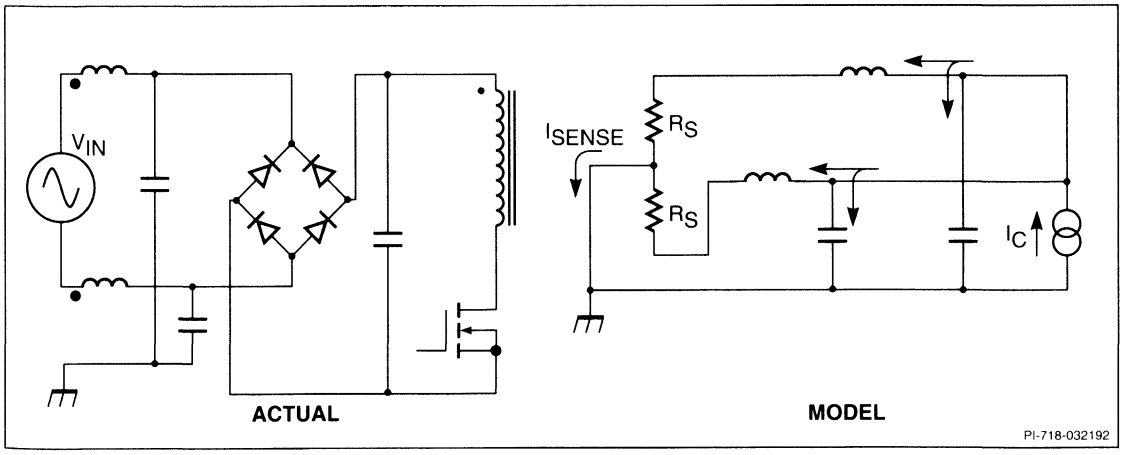


Figure 20. Power Supply Input Section with a Common-mode Filter and Its Impedance Model.

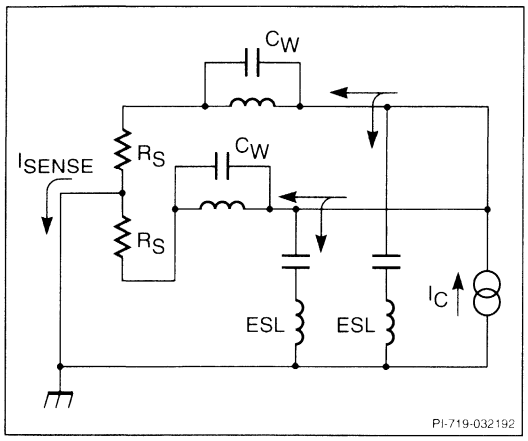


Figure 21. High-frequency Model of the Common-mode Filter.

Physical component layout becomes increasingly critical above 1 MHz. Improper layout can lead to increased capacitor ESL. It is also possible for noise voltages in close proximity to the EMI filter to couple around the filter directly into the mains.

High Frequency Return Path

High-voltage switching waveforms with fast edges and ringing on each transition drive displacement currents through stray capacitance. These displacement currents are free to flow in the mains if alternate shunt paths are not provided. The power transformer primary to secondary capacitance is one of the important parasitic capacitances. Figure 22 shows a noise current path from the MOSFET drain, through transformer capacitance C_X to the secondary return, out the enclosure on output power cables, into the mains ground conductor through additional stray capacitance, back through the EMI filter, and finally back to the MOSFET drain.

Best EMI performance is obtained in applications which have a conductive enclosure connected to the third wire earth ground of the mains. The enclosure forms a conductive shell which intercepts and returns displacement currents back to the primary circuitry. Practical implementations include metal enclosures or plastic enclosures with a conductive coatings on the internal surfaces. The enclosure is AC coupled with capacitors to the primary by the EMI filter and to the secondary by capacitor C12 as shown in Figure 23. Further partitioning between the EMI filter and the power control circuitry can further limit noise current paths, and will be discussed later. C12 can be a standard low voltage ceramic capacitor because the enclosure is grounded and the power transformer provides safety isolation. Low impedance connections to the enclosure are important. The use of long wires should be avoided.

Many applications connect only to the line and neutral and do not connect to protective earth ground. The AC path between primary and secondary is usually implemented with a series connection of two Y style safety capacitors rated for the required AC input voltage as shown in Figure 24. These capacitors will directly couple the AC input voltage to the load but will also limit current flow to safe levels when properly selected. The capacitors are selected to limit current flow between the AC mains and earth ground through a specified impedance (typically between 0 and 2 kΩ) to a safe value (typically 500 μA or less) at rated AC input voltage even if one of the capacitors fails as a short circuit.

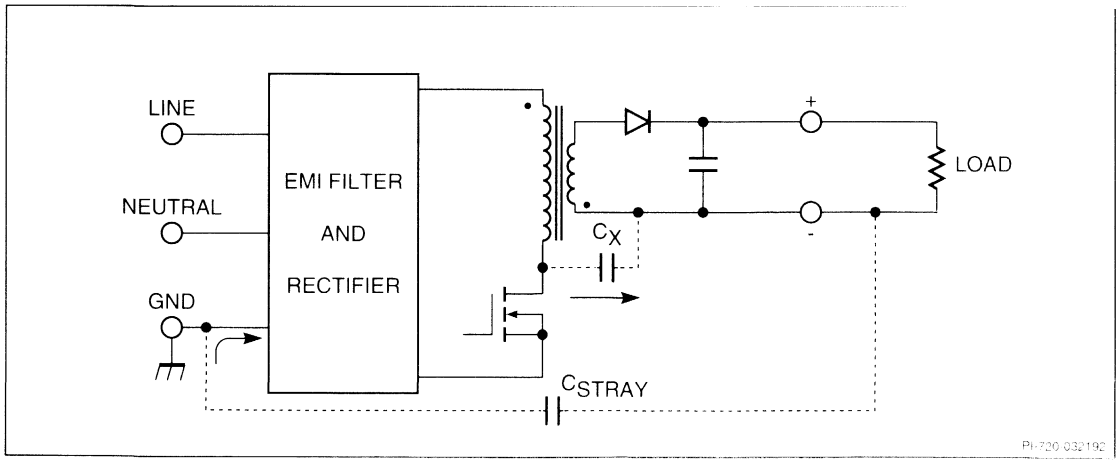


Figure 22. High Frequency Return Path.

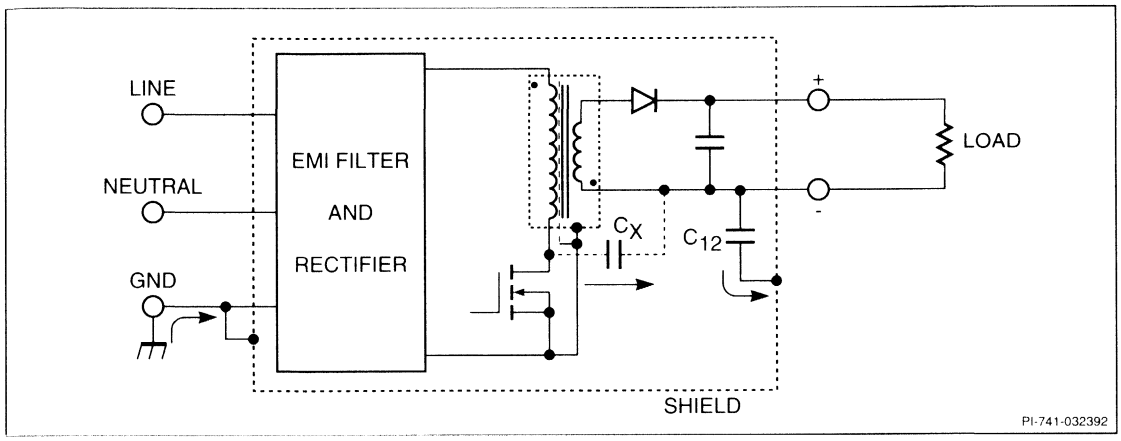


Figure 23. Using a Shield to Direct Noise Currents to Ground in a 3-wire System.

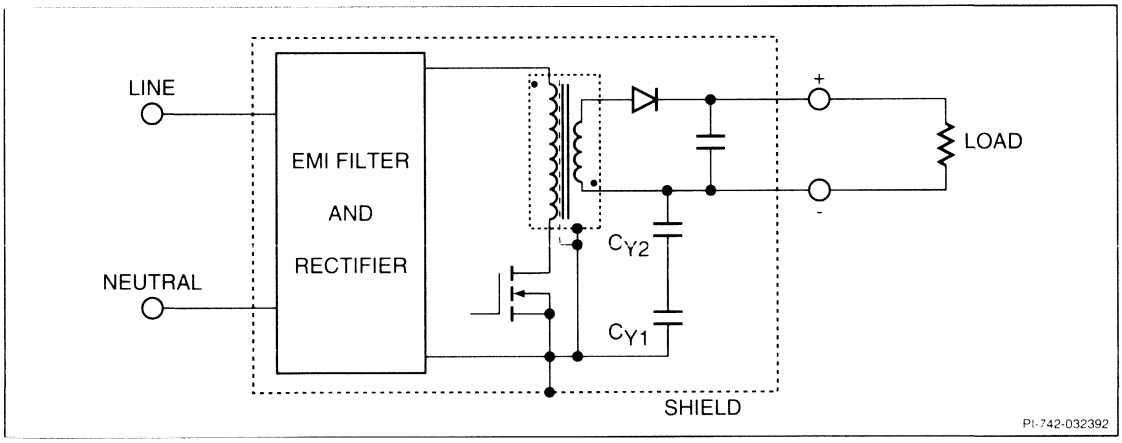


Figure 24. Using a Shield to Direct Noise Currents to the Internal Reference in a 2-wire System.

Shields can be used in applications without an enclosure in both grounded and ungrounded applications. The shield can cover just the high-frequency circuits on the power supply or cover the entire power supply. Practical implementations include stamped and formed metal shapes, deep drawn cans, and metal foil. Low-impedance connections to the shield are important. The use of long wires will degrade performance and should be avoided. In grounded applications, the shield can be treated as an enclosure and connected as shown in Figure 23.

In ungrounded applications the shield should be connected to either V+ or V- side of the primary referenced high voltage DC bus as shown in Figure 24. Note that in ungrounded applications the shield is essentially at primary potential and must be safely insulated from the secondary voltage. Avoid the use of long wires when connecting to the shield.

Transformer Shielding, Gapping, and Core Connection

Proper transformer construction techniques are necessary for reducing common-mode emissions. The transformer should have a primary-connected shield between the primary and secondary to return displacement currents. This shield intercepts interwinding capacitive displacement currents and returns them to the primary circuitry. The shield is shown connected to V- in Figures 23 and 24. The shield can also be connected to V+ if more convenient for construction or layout reasons. Note that safety insulation or creepage distance is required between the shield and secondary because the shield is at primary potential.

Flyback power supplies typically require the use of gapped ferrites as the transformer material of choice. The method used to gap the core can influence common-mode emissions heavily. Gaps always have fringing fields as shown in Figure 25. The gap should be confined to the center leg of either one or both cores so that the fringing field can be contained by the windings. End gaps will "leak" magnetic flux due to the fringing field which can produce common-mode emissions.

The core should also be connected back to the primary as shown in Figures 23 and 24. Transformer core clamps that solder directly into the PC board are available for most core shapes. Another common technique covers the outside of the core, exposed winding, and end gaps with a copper foil shield which is then connected by a wire to a bobbin pin. An insulated external shield could also be used if the core cannot be directly connected for safety reasons.

Refer to DA-3 and AN-7 for more information on transformer construction.

Power Cord Resonance

Applications with 3-wire power cords require special attention. A six foot power cord can be modeled as a transmission line with distributed inductance and capacitance, characteristic impedance of approximately 100 Ω, and little damping which leads to a sharp, well defined resonance, typically between 15 and 25 MHz. This resonance can amplify existing common-mode emission currents to levels in excess of the desired limit. A small, lossy ferrite bead or toroid placed over the ground wire reduces the resonant peak by adding series damping. The ferrite bead or toroid should have an effective impedance of 100 Ω in the 15 to 25 MHz range. The bead is placed over the safety ground wire between the enclosure power entry connector and the internal safety ground attachment point of the enclosure. The toroid is installed in similar fashion but can accommodate up to 5 or 6 turns of the insulated safety ground wire.

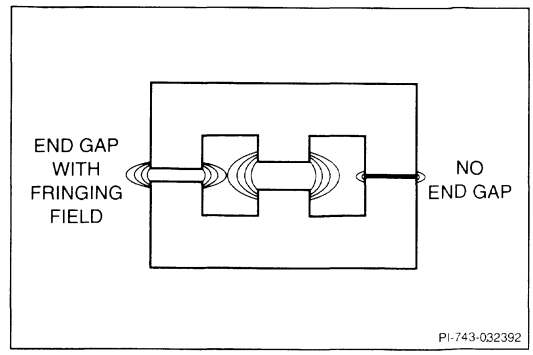


Figure 25. End Gap Magnetic Flux "Leakage".

General Purpose EMI Filters

3-Wire AC Input

A typical EMI filter for 3-wire AC input applications (Line, Neutral, and Earth Ground) is shown in Figure 26. Normal-mode attenuation is provided by C1, C6, and L3 while common-mode attenuation relies on L2, C7, and C8. Capacitor C17 provides AC coupling between the primary circuitry and chassis ground when no current is flowing through bridge rectifier BR1 to minimize common-mode emissions. Ferrite bead L4 slips over the ground conductor for power cord damping and further attenuation of common-mode signals. Capacitor C12 provides AC coupling between the secondary and primary.

2-Wire AC Input

A typical EMI filter for 2 wire AC input applications (Hot and Neutral with no Earth Ground) is shown in Figure 27. Normal-mode attenuation is provided by C1, C6, and L3 while common-mode attenuation relies on L2, C5, C6 and C7. Without a shield radiating fields couple common-mode displacement currents directly into the AC mains. Shielding contains the fields and returns displacement current within the physical boundaries of the power supply. Shielding can be implemented many ways which include metal enclosures, plastic enclosures with metalized coatings on inside surfaces, and metal foils which wrap around the power supply. Low impedance connections to the shield are important. Note that safety insulation or spacings will be required with this shield because there is no connection to earth ground by the third wire of the AC mains. The shield should be considered as electrically connected to the primary circuitry which contain hazardous voltage levels.

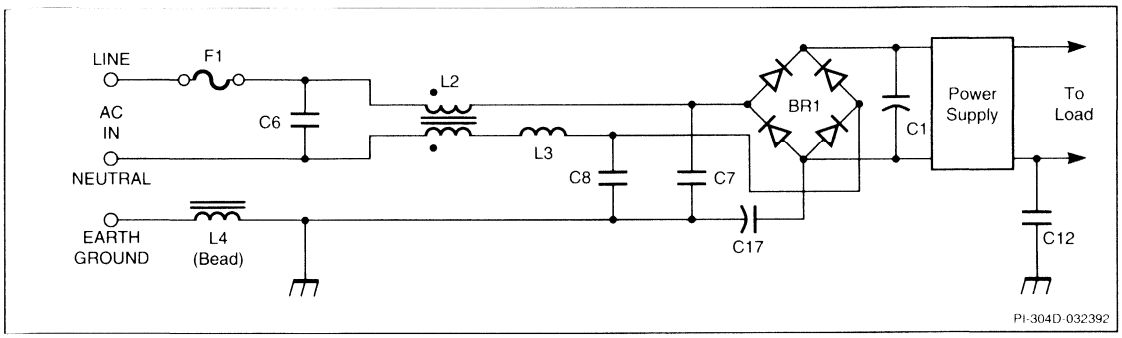


Figure 26. 3-wire Input EMI Filter Example.

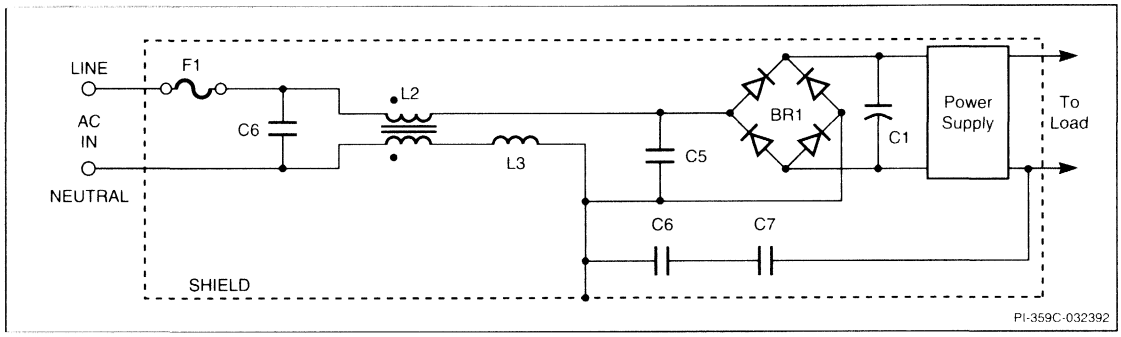


Figure 27. 2-wire Input EMI Filter Example.

Alternative Filter Approach Without Balun Inductor

An alternative filter for lower power applications is shown in Figure 28. This filter splits the required energy storage capacitor to create a pi type filter. Peak current in L1 and L2 is approximately half the peak current in bridge rectifier BR1 due to capacitor C1. Normal-mode attenuation is provided by C1, C2, L1, and L2. R1 and R2 damp the parasitic resonances of L1 and L2, respectively. Common-mode emissions are returned to primary by the shield shown connected to the primary voltage return. This shield is at primary potential and requires safety insulation or clearances. The secondary is AC coupled back to the primary by two series safety rated Y capacitors (C3 and C4) to further reduce common-mode emissions. C3 and C4 are chosen such that the leakage current between AC mains and secondary is below the maximum value specified by the required safety regulations even if one of the capacitors is a short circuit.

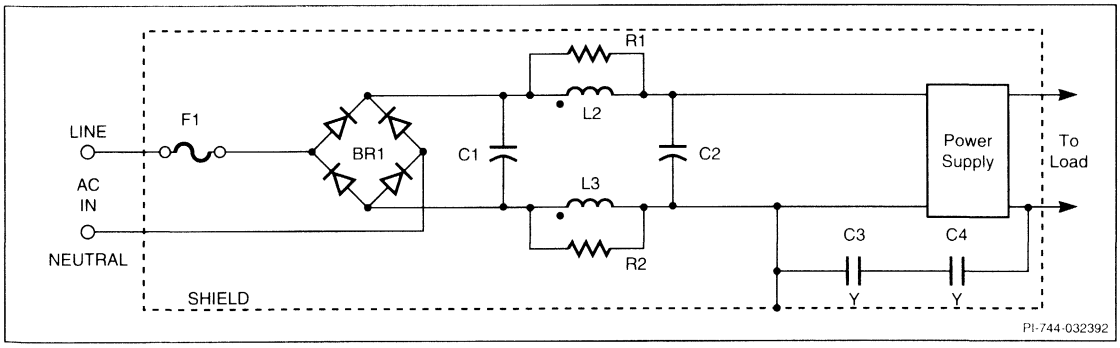


Figure 28. Alternative pi Filter EMI Approach.

EMI Filter Layout Issues

Filter layout is extremely important to obtain the desired attenuation. Poor layout practice can cause conducted emissions to actually couple around the filter components directly into the AC mains conductors.

Capacitor lead length must be minimized as much as possible to reduce ESL. This includes the traces on the PC board leading up to the capacitor pads. Figure 29 shows the right and wrong way to route PC traces to capacitors.

Inductors should be mounted to avoid introducing parallel capacitance. Figure 30 shows the right and wrong way to route PC traces to inductors. Keep the traces well separated to prevent coupling.

Locate the normal-mode filter capacitor across the AC input conductors as close as possible to the power entry point.

Keep power stage and output components away from the EMI filter to prevent coupling around the filter. The best approach is to place the EMI filter at one end of a rectangular power supply shape and place the output at the other end as shown in Figure 31. Square power supply shapes should be avoided if possible since the power stage and the output components will be in close proximity to the EMI filter, allowing noise to couple directly into the mains.

Practical Considerations

Successful EMI filter design begins with knowledge of the nature of the emissions. Switching power supply noise sources generating normal-mode and common-mode conducted emissions have been described in detail. At this point a working power supply is assumed to be available. Design, layout, and packaging have most likely followed some (if not all) of the recommended techniques to minimize EMI. The EMI filter must attenuate the remaining emissions below the specification limit. Implementing a successful EMI filter is an iterative process. The basic steps include:

- Identify and attenuate the normal-mode fundamental
- Identify and attenuate the common-mode fundamental
- Identify other emissions over the spec limit. Determine whether each emission is normal-mode or common-mode. Determine whether each emission is coupling around or passing through the EMI filter. Change the filter design, add a shield, or control the circuit source to attenuate each emission below the specification limit.
- Go back and check the earlier emission levels to make sure a change did not cause a different problem to occur.

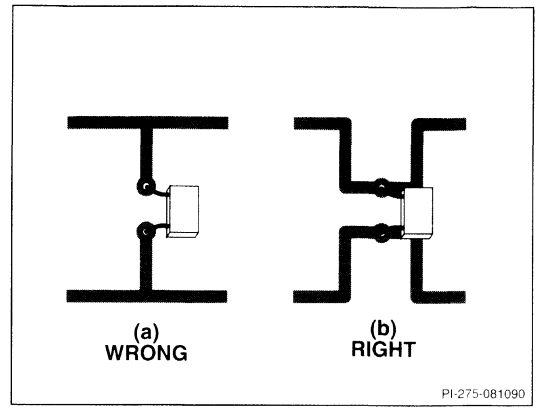


Figure 29. Bending the Bus to Minimize Resistive Effects.

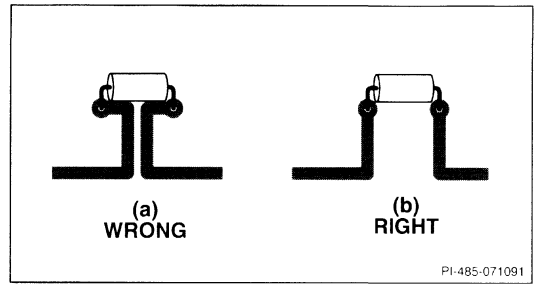


Figure 30. Minimizing Parallel Capacitance of Inductors.

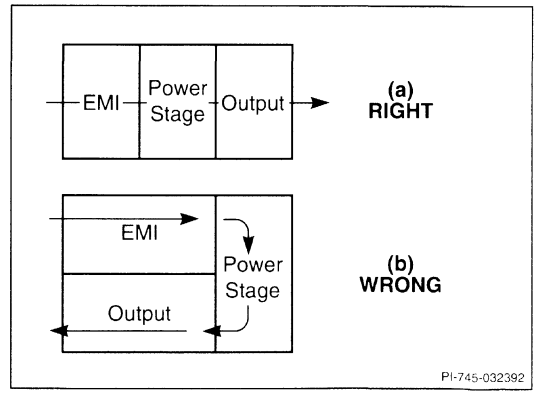


Figure 31. Power Supply Layout to Minimize Noise Coupling.

Normal-mode Versus Common-mode

The first frequency sweep for EMI conducted emissions will usually produce a spectrum as shown in Figure 32. The fundamental is outside the specification limit as well as some of the harmonics. Each harmonic is composed of both normal-mode and common-mode emissions. In Figure 33, a normal-mode component with magnitude 70 dB(μV) is shown relative to a common-mode component with magnitude 50 dB(μV). 20 dB difference between the two components is actually an order of magnitude between the absolute values of the two components. The signals will add and superimpose if the phasing is correct but the overall effect on the measured signal level is slight (10% increase, or less than 1 dB).

A normal-mode filter with 30 dB attenuation at the harmonic frequency of interest will not attenuate the measured peak by 30 dB (a). The normal-mode component will be attenuated from 70 dB to 40 dB, but the 50 dB common-mode peak will now dominate the measurement (b). Further normal-mode attenuation will have no effect on the measured harmonic because the signal is common-mode. Common-mode filtering will have to be employed to reduce this harmonic any further.

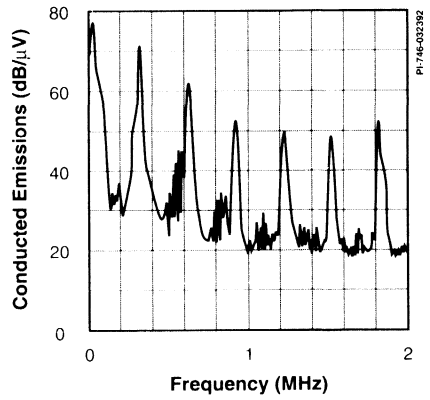


Figure 32.

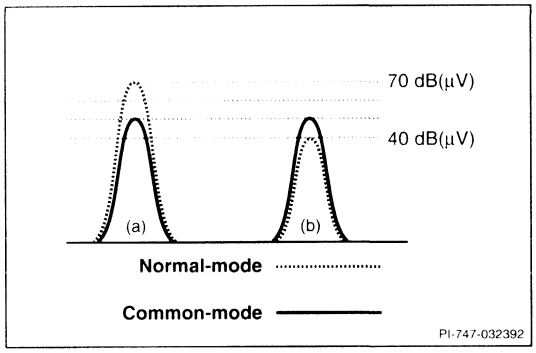


Figure 33.

Using Splitters

Splitters combine the outputs of the two LISNs to determine if a specific emission is common-mode or normal-mode. Two splitters are required: an in-phase splitter (Mini Circuits Lab[3] ZSC-2-2) where V_{OUT} is the sum of the two LISN signals and a 180 degree out-of-phase splitter (ZSCJ-2-2) where V_{OUT} is the difference between the two LISN signals. The splitter setup is shown in Figure 34.

Normal-mode

Normal-mode emission current (I_n) circulates from the power supply through the first LISN sense resistor (producing an in phase sense voltage), through the second LISN sense resistor (producing an out of phase sense voltage), and back to the power supply. The output voltage of the in-phase splitter will have no normal-mode component because the opposite phased sense voltages effectively cancel. The output voltage of the 180 degree out-of-phase splitter will have normal-mode components 6 dB higher than those measured directly at the LISN as the sense voltages are now effectively in phase and add.

Balanced Common-mode

Balanced common-mode currents (I_{cb}) are defined as those with similar gain and phase that flow from ground through each LISN sense resistor (producing sense voltages with the same phase) and through the AC input to the power supply. The output voltage of the in-phase splitter will have balanced common-mode components 6 dB higher than those measured

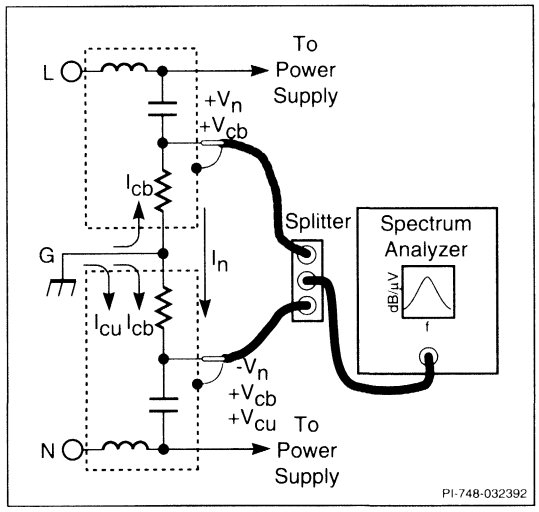


Figure 34.

directly at the LISN because the in phase sense voltages effectively add. The output voltage of the 180 degree out-of-phase splitter will have no balanced common-mode components as the sense voltages are now effectively out of phase and cancel.

Unbalanced Common-mode

Unbalanced common-mode currents (I_{cu}) flow from ground through either LISN sense resistor without a current with matching magnitude and phase flowing through the other LISN sense resistor. Unbalanced common-mode currents are found when the EMI filter does not have balanced impedance in each leg or when noise from the power path returns from the AC mains asymmetrically through one side of the EMI filter (typical for spatial coupling between power path circuitry and one side on and EMI filter). The output voltage of the in-phase splitter will have unbalanced common-mode components equal to those measured directly at the LISN because there is no cancellation. The output voltage of the 180 degree out-of-phase splitter will also have unbalanced common-mode components equal to those measured directly at the LISN for the same reason.

The results of using the two splitters on each of the three types of emissions is shown in Table 1.

LISN OUTPUT	IN PHASE	180° OUT OF PHASE
Normal (V_n)	0	V_n + 6 dB
Balanced Common-mode (V_{cb})	V_{cb} + 6 dB	0
Unbalanced Common-mode (V_{cu})	V_{cu}	V_{cu}

Table 1.

EMI Filter Components

No EMI filter component is perfect. At some frequency all components "give up" their basic characteristic to the effects of parasitics.

Measure all capacitors. Identify specifically the self-resonant frequency (above which the capacitor looks like an inductor) and effective Q. Examine for non-linear behavior such as capacitance which varies with frequency.

Measure all inductors. Look specifically for the self resonant frequency (above which the inductor behaves like a capacitor) and effective Q. Identify multi-resonant behavior due to multiple layer winding. Measure with DC current bias if possible to determine the true inductance at the peak of the input current waveform.

Spatial Coupling

As power supplies get smaller the EMI filter gets closer to circuitry acting as noise generators. High dv/dt voltage waveforms and high di/dt current loops generate fields which may spatially couple around the EMI filter and induce emission currents directly in the mains. Noise currents which couple around the filter must be distinguished from the noise currents which are passing through the filter.

One way to separate conducted emission currents is to place the power supply power circuitry and load within a grounded box as shown in Figure 35. The EMI filter is connected between the enclosed power supply and AC mains. The box will contain the fields, allowing conducted emission currents to be directly measured. This is especially effective when analyzing the fundamental.

The spatial coupling emissions can be reduced by containing the fields at their sources with local shields. Local shields over primary power circuitry such as the flyback transformer, primary damper, clamp diode, and power supply IC can be used to contain fields. Local shields can also be used over secondary circuitry such as output rectifiers. Shields can also be applied around the EMI filter although the preferred approach is to contain the field at the source. Heat sinks can be used as shields and grounded by using an insulator for isolation from the component.

Another type of shield is a conductive plate approximately the same size as the printed circuit board. This plate can be connected to earth ground, primary reference, or secondary reference (depending on the safety insulation system chosen). This is attractive for applications connecting to the third wire ground but without a conductive enclosure.

Lossy Beads

Small beads can be used in circuit leads to damp or eliminate high frequency ringing. Ferrite beads from Fair-Rite(4) and amorphous metal beads from Toshiba[5] (Spike Killer™ and Amobead ™) are available in a variety of shapes. These beads feature low impedance at low frequency for minimal effect on the current waveform but have high impedance at high frequency with significant parallel resistance to damp and reduce ringing voltage waveforms.

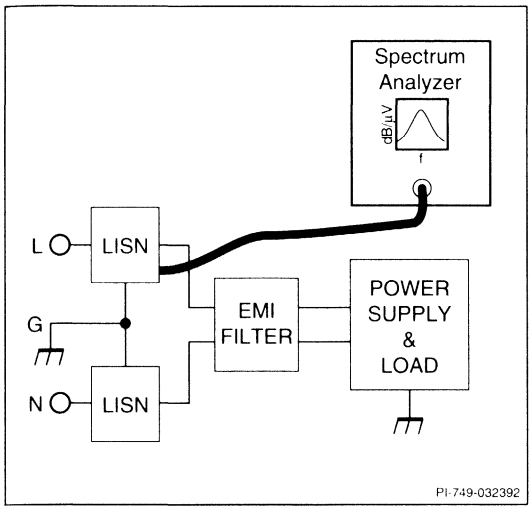


Figure 35. Isolating Conducted Emissions.

Grounding

Some applications connect the output voltage to earth ground. Others have no connection at all to earth ground. It is important to identify the earth ground connection expected for each application and to test in that configuration. EMI testing should be performed in both grounded and ungrounded configurations if, for example, the output is designed to be either grounded or ungrounded.

Power Cord

The power cord resonance previously described can interfere with conducted emissions testing. Switch between two power cords of different lengths to separate power cord resonances from other conducted emissions.

Miscellaneous Test Tricks

Terminate opposite LISN with 50 ohm terminator. The LISN sense impedance is actually determined by the termination and will change if not properly terminated.

Warm up equipment including Device Under Test (DUT) for at least 1 hour before testing so results will be repeatable.

Connect the load close to the power supply output. Long wires between the load and the power supply can radiate noise to the input wires and should not be used unless present in the actual application.

Compare EMI test results with both AC and high voltage DC input. Differences could be caused by inductors saturating on the peak of the AC current waveform because the effective peak current is much lower with DC input.

Make sure analyzer sweep speed is low enough to capture the peaks of each harmonic. The bridge rectifier conducts current (both power and emission currents) for a short time compared with the full line cycle which effectively "samples" the emission currents. Slower sweep speeds will collect enough data to accurately measure each emission. Increase sweep speed temporarily until "holes" in the data spectrum begin to appear as a quick check.

Step-by-Step Procedure

1) Calculate normal-mode fundamental and select filter components as shown in appendix. Measure impedance versus frequency for each component. Select components with resonant frequencies that do not coincide with waveform ringing frequencies in the power supply. Install normal-mode EMI filter outside the mechanical package or envelope of the power supply to reduce spatial coupling effects.

2) Use high voltage DC source through LISNs to provide power to the power supply. Use the 180 degree splitter to extract the normal-mode fundamental current component. Compare the measured normal-mode fundamental with the calculated value. Modify the normal-mode filter design if necessary to meet the specification limit with the desired margin.

3) Examine entire frequency range for normal-mode components close to or in excess of the specification limit. Pay special attention to frequency ranges around measured component resonances and identified circuit ringing frequencies. Modify normal-mode filter design if necessary.

4) Use in-phase splitter to extract the balanced common-mode fundamental current component. Place the largest value safety capacitor subject to leakage current limitations from the power supply high voltage return (negative side of the bridge rectifier) to safety ground and from safety ground to output return. If no safety ground is available use two safety capacitors in series between secondary return and the high voltage DC or high voltage return of the bridge rectifier. Select the smallest, widest bandwidth balun that attenuates the balanced common-mode fundamental to the desired level. Measure impedance versus frequency for each component used to ensure that it is appropriate for the application. Select components with resonant frequencies that do not coincide with waveform ringing frequencies in the power supply. Install common-mode EMI filter outside the mechanical package or envelope of the power supply to reduce spatial coupling effects.

5) Examine entire frequency range for common-mode components close to or in excess of the specification limit. Pay special attention to frequency ranges around measured component resonances and identified circuit ringing frequencies. Modify common-mode filter design if necessary.

6) Measure the unit with AC input voltage. Compare (using both splitters) the normal-mode and balanced common-mode emissions with the DC input results. Choose normal-mode inductors with higher saturation current ratings if the emissions are higher with AC input and repeat steps 1-6.

7) Combine filter with power supply in final packaged configuration and solve spatial coupling effects using grounding, shielding, or capacitive coupling techniques.

8) Perform final test with secondary attached to ground and also isolated from LISN ground.

References

1 Glenn Dash, "The ABCs of Regualtions and Standards," Compliance Engineering 1991 Reference Guide: Compliance Engineering Magazine, January 1991

2 Glenn Dash and Isidor Straus, "German Regulation of Electronic Equipment Emissions", Compliance Engineering 1991 Reference Guide: Compliance Engineering Magazine, January 1991

3 Mini-Circuits Lab, 2625 East 14th Street, P.O. Box 350166, Brooklyn, NY 11235, 718-934-4500

4 Fair-Rite Products Corporation, PO Box J, 1 Commercial Row, Wallkill, NY 12589, 914-895-2055

5 Toshiba Corporation, Material and Components Group, 1-1, Shibaura 1-Chome, Minatoku, Tokyo 105 Japan, (03)457-4961

APPENDICES

APPENDIX A:
Normal-mode Filter Example Calculation

For a typical 5 watt application with switching frequency f_S of 800 kHz, peak drain I_D current of 300 mA, 100 mΩ ESR of energy storage capacitor, rise time of 25 ns, duty cycle D of 0.5, and conducted emissions limits in accordance with FCC part 15, subpart J:

1) Establish noise voltage V_n:

$$I_D = 2I_{pk} \times D \times \frac{\sin(n\pi D)}{n\pi D} \times \frac{\sin\left(n\pi \frac{t_R}{T}\right)}{n\pi \frac{t_R}{T}}$$

$$= 2 \times 0.3\text{mA} \times 0.5 \times \frac{\sin(\pi \times 0.5)}{\pi \times 0.5} \times \frac{\sin\left(\frac{\pi \times 25\text{ns}}{1.25\mu\text{s}}\right)}{\frac{\pi \times 25\text{ns}}{1.25\mu\text{s}}} = 200\text{mA}$$

$$V_n = I_D \times \text{ESR} = 200\text{mA} \times 100\text{m}\Omega = 20\text{mV}$$

2) Select target noise voltage and convert from dB(μV) to absolute value:

$$V_{sense} = 1 \times 10^{-6} \times 10^{\frac{40\text{dB}(\mu\text{V})}{20}} = 100\mu\text{V}$$

3) Calculate RMS current I_1:

$$I_1 = V_{SENSE} \times \sqrt{\left(\frac{1}{2 \times R_S}\right)^2 + (2\pi \times f_S \times C_F)^2}$$

$$= 100\mu\text{V} \times \sqrt{\left(\frac{1}{2 \times 50\Omega}\right)^2 + (2\pi \times 800\text{kHz} \times 100\text{nF})^2} = 50.3\mu\text{A}$$

4) Calculate inductor L

$$L = \frac{V_n}{2\pi \times f_S \times I_1} = \frac{20\text{mV}}{2\pi \times 800\text{kHz} \times 50.3\mu\text{A}} = 79\mu\text{H}$$

Pick an inductor with at least this minimum inductance under the peak bias current expected in the application.

APPENDIX B:
Common-mode Filter Example Calculation

For a typical 5 watt input voltage application with a switching frequency (f_S) of 800 kHz, peak drain current of 300 mA, 140 VAC maximum input voltage, 50 Hz input frequency, safety leakage current limit of 500 μA, and conducted emissions limits in accordance with CISPR, Publication 22:

1) Measure conducted emission at f_S: 83 dB(μV)

2) Extract conducted emissions limit from specification: limit is 48 dB(μV) at f_S

3) Determine the necessary attenuation:

$$A(\text{dB}) = V(\text{dB}) - \text{SpecLimit} - \text{Margin}$$

$$= 83\text{dB}(\mu\text{V}) - 48\text{dB}(\mu\text{V}) + 6\text{dB}(\mu\text{V}) = 41\text{dB}$$

4) Convert attenuation from A(dB) to simple ratio A:

$$A = 10^{\frac{-A(\text{dB})}{20}} = 10^{\frac{-41\text{dB}}{20}} = 8.91 \times 10^{-3}$$

6) Calculate the LC product from f_S and A:

$$LC = \frac{1}{A \times (2\pi f_S)^2} = \frac{1}{8.91 \times 10^{-3} \times (2\pi 800\text{kHz})^2} = 75.5\text{kHz}$$

7) Calculate the filter corner frequency from LC product:

$$f_C = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi \times \sqrt{4.44 \times 10^{-12}}} = 75.5\text{kHz}$$

8) Select the maximum value for capacitors from leakage current I_L, maximum input voltage V_{IN}, and input frequency f_{IN}:

$$C_{MAX} = \frac{I_L}{V_{IN} \times 2\pi f_{IN}} = \frac{500\text{mA}}{140\text{V} \times 2\pi 50\text{Hz}} = 11\text{nF}$$

Select the next lower standard value based on component size, voltage rating, and availability: 10 nF.

9) Calculate the minimum required inductance L from the capacitor value and corner frequency f_C:

$$L = \frac{1}{C \times (2\pi f_C)^2} = \frac{1}{10\text{nF} \times (2\pi \times 75.5\text{kHz})^2} = 442\mu\text{H}$$

Charging Batteries with the PWR-SMP260

DESIGN AID DA-5

Portable products require the fast and safe recharging of the batteries used to power them. Examples of this class of equipment are laptop and notebook computers and portable instruments. There are two main elements to these systems; the power management circuit and the recharging circuit. The division of these functions varies from design to design, but generally, the battery voltage, temperature and charge time relationships are controlled by the secondary-side power management function. This in turn controls the primary-side recharging circuit. The algorithms for control are dependent on the battery being used and the power system configuration. This design aid addresses the interface between the power management function and charging function, and is divided into two sections that correspond to methods of control; digital interface and linear interface.

Digital Interface

The evolution of the digital power management function in microcontroller systems involves the management of battery recharging as well as minimizing the discharge rate during operation of the equipment. Microcontroller management of the recharging process will allow safe high-rate charging of the battery to minimize recharge time and maximize battery lifetime. The most common interface to the digital power management function is a digital one as well.

The most rudimentary digital interface for battery charging control uses the SYNC pin of the PWR-SMP260 as an ON/OFF control, as shown in Figure 1. The ON/OFF or two-state control depends on the constant-power characteristic of the flyback power supply. The feedforward function described in AN-11 can be used to make the current limit and constant power characteristics of flyback power supplies independent of input voltage.

Research on high-rate charging of NiCd batteries has indicated that pulse charging of the battery will enhance the recharge efficiency and reduce the heat build up effect commonly observed in continuous-current chargers. The two states of the charger do not need to be full and zero power. They could be full and some fraction of full power. The fractional power level can be accomplished by injecting a constant current into the FEEDFORWARD pin as shown in Figure 2, reducing the current limit of the power supply .

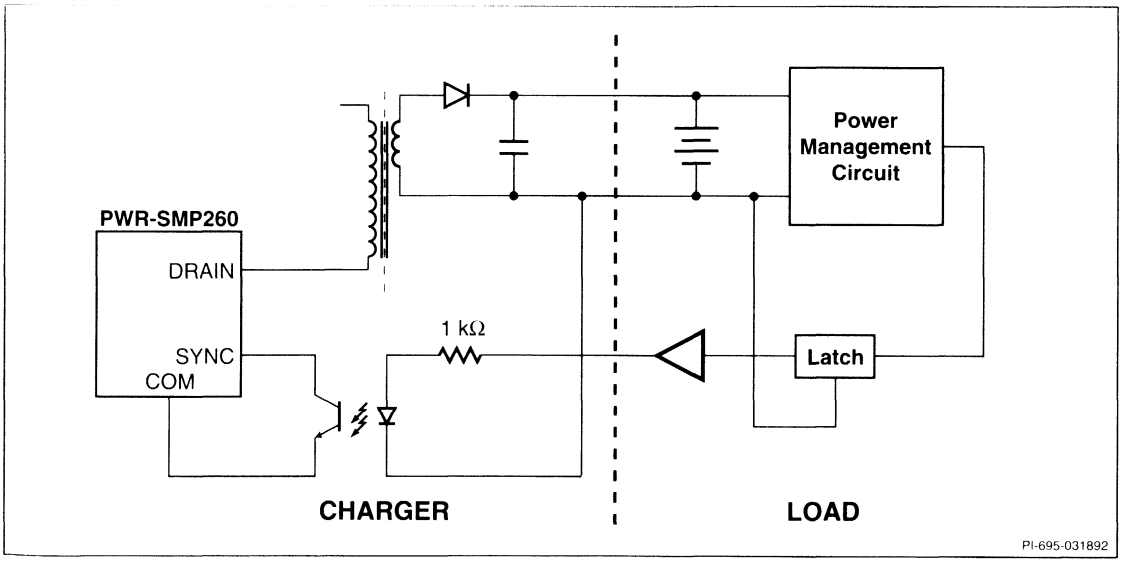


Figure 1. Two-state (ON/OFF) Pulse Power Charging Circuit.

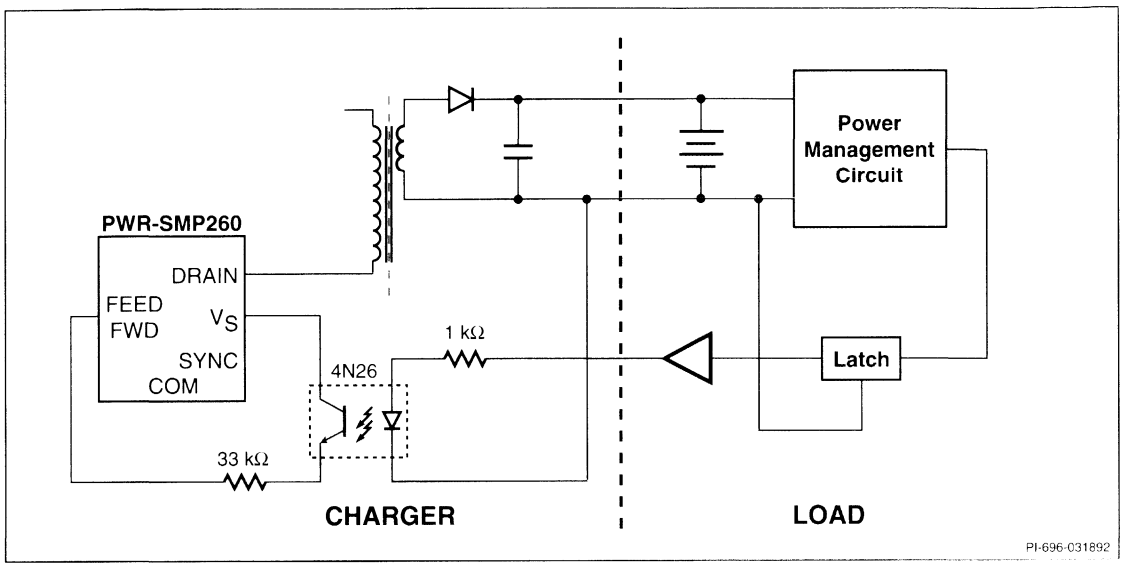


Figure 2. Two-state Factional Power Charging Circuit.

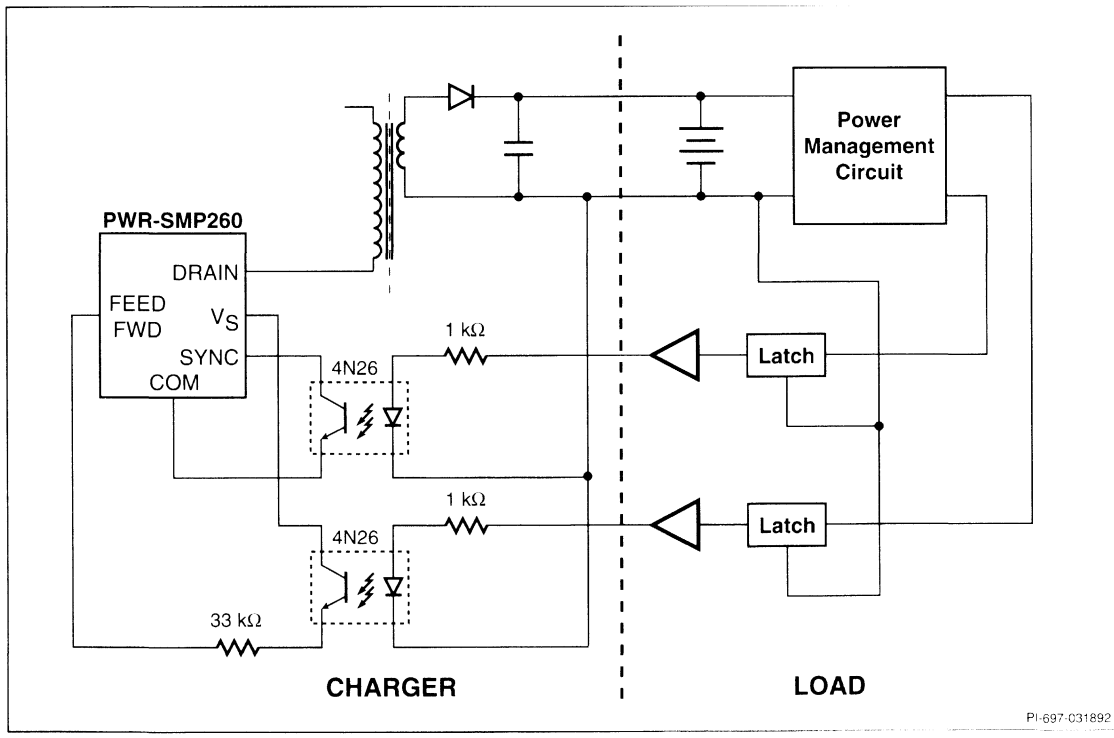


Figure 3. Three-state (Full, Fractional, Zero) Power Charging Circuit.

A three-state control function is shown in Figure 3. The three states are full, fractional, and zero power. The zero power state is controlled by the optical coupler, controlling the SYNC pin of the PWR-SMP260. The fractional power optical coupler injects a constant current into the FEEDFORWARD pin. Multiple fractional power levels can be controlled digitally with a weighted resistor ladder driving current from a reference voltage such as V_S, and controlled by optical couplers.

A two-state output voltage circuit is shown in Figure 4. The two-state voltage requirement is common for lead-acid battery applications. The circuit operates by changing the voltage divider ratio on the output error amplifier to adjust the float voltage. Low impedance battery technology such as NiCd, Nickel Metal Hydride, Lithium Manganese dioxide and Lithium Ion do not need to have the terminal voltage elevated to get the battery to accept charge.

Nickel Metal Hydride and Lithium battery chargers usually have a maximum length of charge time associated with them. This timing function can be implemented in the power management function or within the charger circuitry, depending on the requirements of the battery maintenance system design.

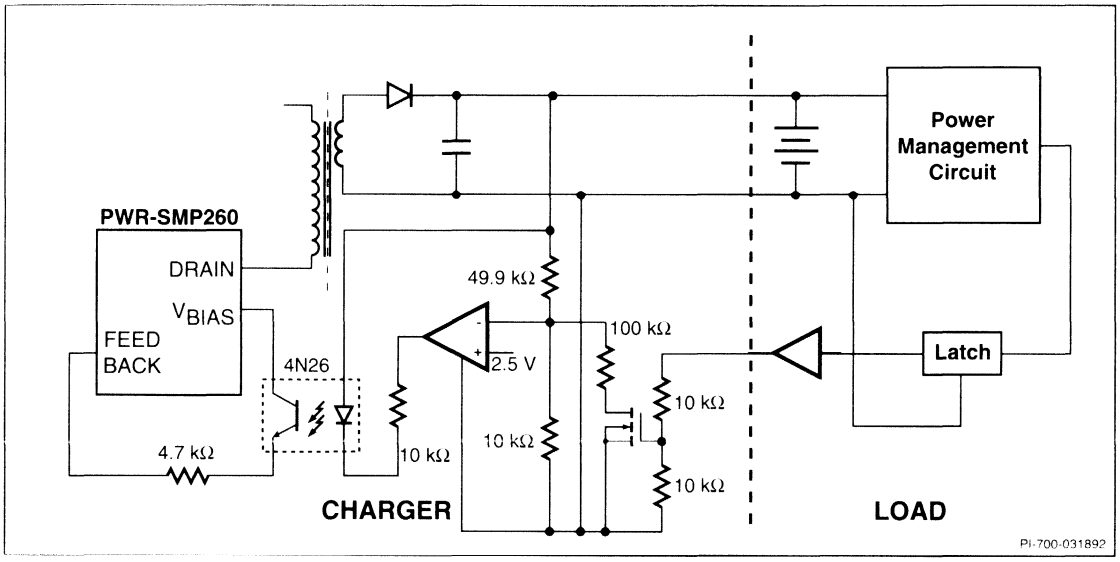


Figure 4. Two-state Output Voltage Adjust.

Linear Interface

The linear interface will proportionally control the output voltage over a specified range by controlling current offsets fed into the output voltage divider as shown in Figure 5. The digital to analog converter (DAC) in the power management function will output a 0 - 5 V signal to adjust the output voltage. The error amplifier will keep the middle of the voltage divider at 2.5 V. The value of the resistor in series with the control wire sets the maximum adjustment voltage. The voltage adjust range is symmetric around the 2.5 V level so that if a +/- 5% adjustment is required, then the series resistor value will be set to provide 95% of nominal voltage when the DAC output is 5 V. The output voltage will be 105% when the DAC output is 0 V. The voltage drop in the output power distribution cable will affect the exact offset voltage unless the output voltage is remotely sensed at the end of the cable. This will not be a problem if the precise offset is only desired at light load when the voltage drop in the distribution cable is low.

Feedback Signals

A digital feedback signal from the voltage error amplifier can be generated to indicate when the charger voltage has reached the float voltage level. This circuit, shown in Figure 6 monitors whether the output voltage error amplifier is operating in its linear region. If the error amplifier is driving the optical coupler then the logic signal will be high. This signal will change states on the constant voltage part of the charger V-I curve shown in figure 7(a). A different type of signal can be generated using the circuit shown in Figure 8. This circuit uses the minimum load characteristic of the PWR-SMP260 to indicate when the output power of the charger has decreased to less than 12% of full power. This signal will change states on the constant voltage part of the charger V-I curve shown in figure 7(b).

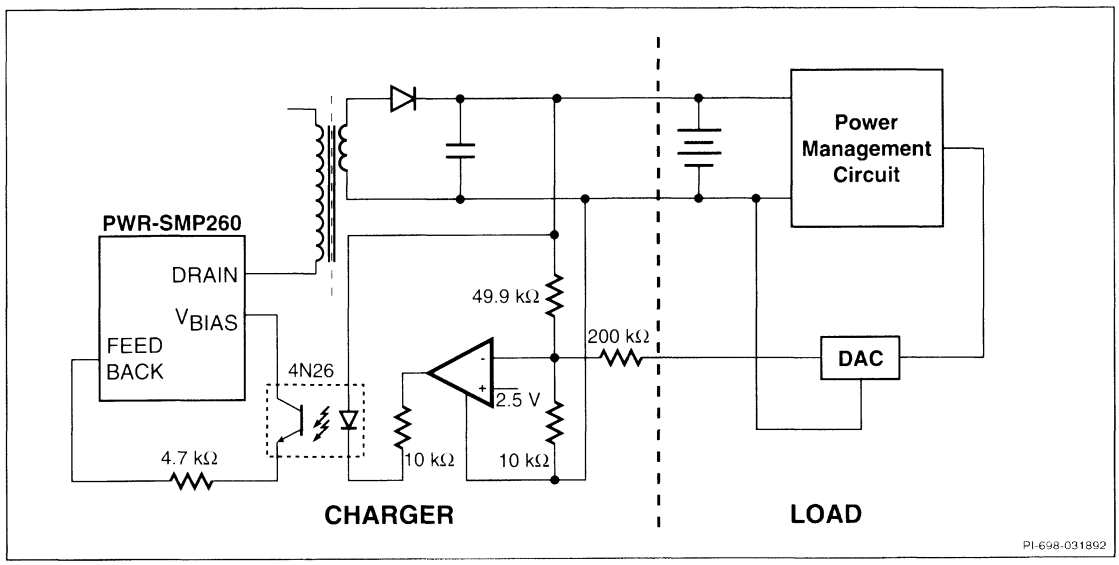


Figure 5. Limited Range Linear Interface Circuit.

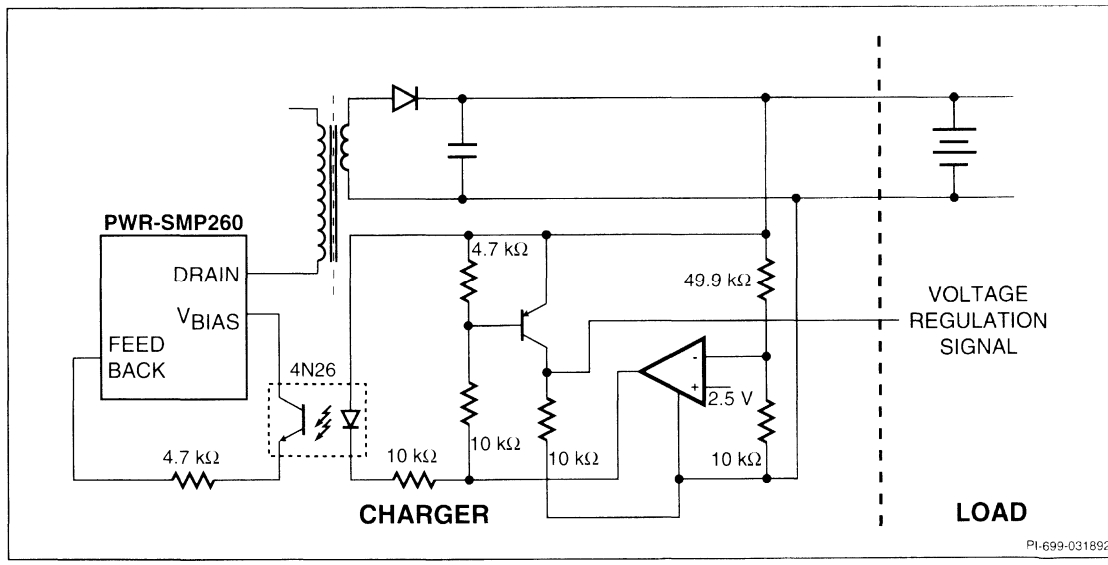


Figure 6. Voltage Regulation Monitor Circuit.

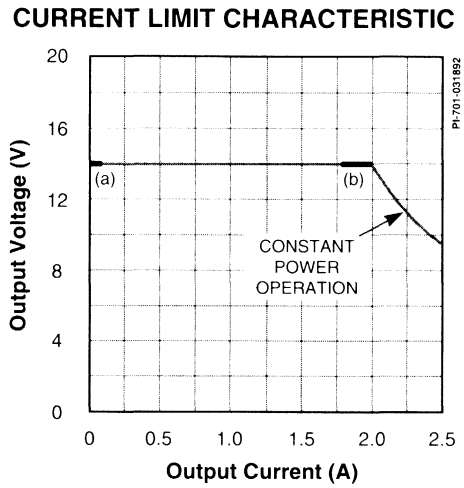


Figure 7. (a) Voltage Regulation Monitor, and (b) Low Output Power Monitor.

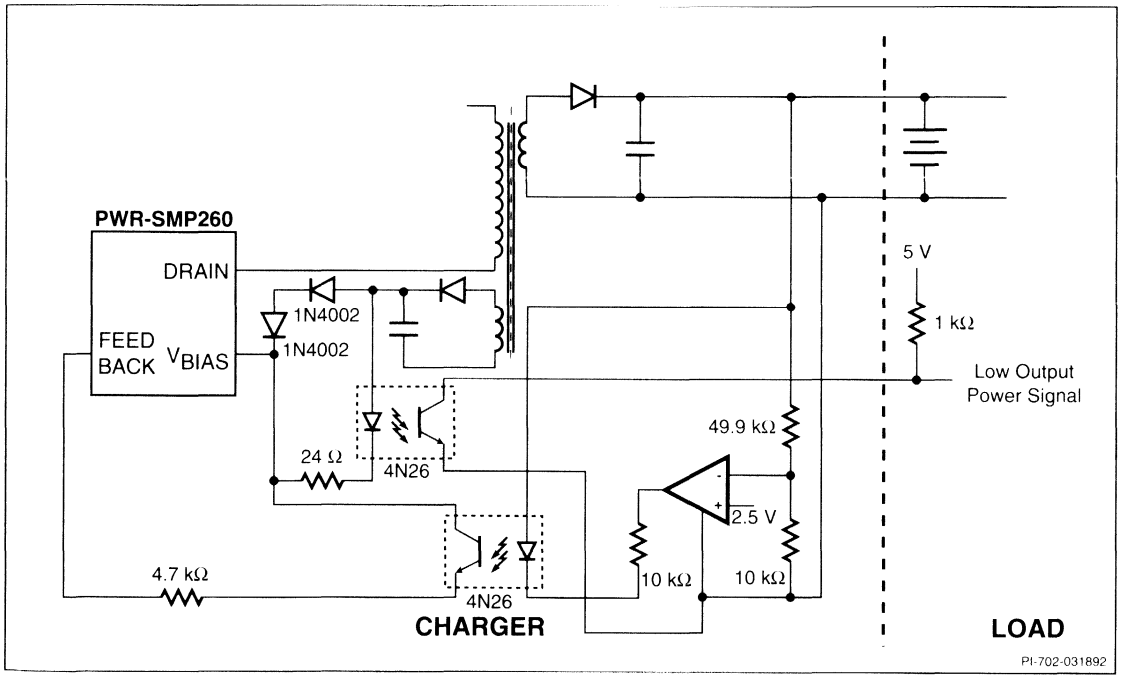


Figure 8. Low Output Power Monitor Circuit.

Die Ordering Information 5

Die Ordering Information

Power Integrations Die Sales Policy

Power Integrations, Inc. makes all of its SMP and INT products available for sale in die form.

Electrical Specifications

All material is 100% electrically probed using Power Integrations test equipment per applicable specification.

Physical Specifications

- Die thickness 15 mils (0.381 mm) typical
- Bonding pad size 4.0 x 4.0 mils (0.102 mm) typical

Die are visually inspected according to commercial standards. Each die surface is protected by a passivation layer except for bonding pads.

Assembly Considerations

Power Integrations recommends storing the die in a clean, dry environment, preferably in an atmosphere of an inert gas such as dry N_2. Also, care should be taken when handling die as electrical and visual defects can be induced by improper handling and storage procedures.

Packaging for Shipment

Power Integrations supplies standard product die in waffle packs.

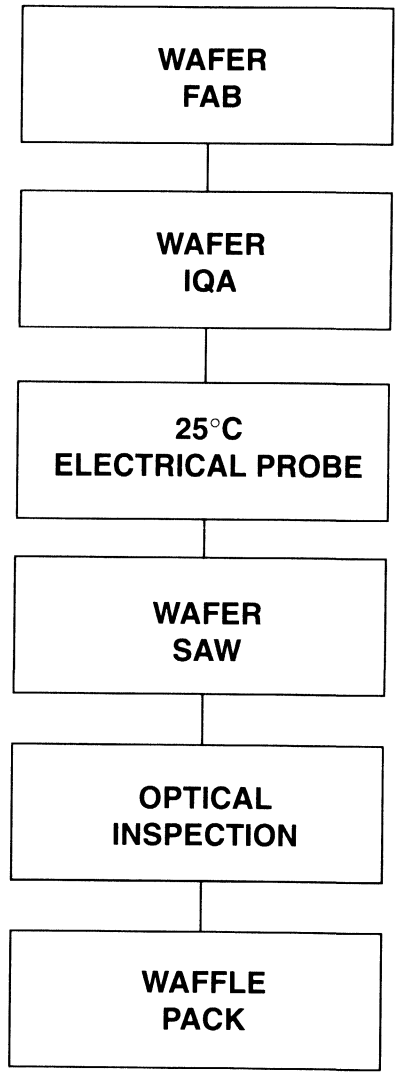
Changes

Power Integrations reserves the right to improve device geometries and manufacturing processes without prior notice.

Ordering Information

Ordering information for die may be found at the front of the databook. Minimum order size is 25,000 units with 5,000 units per line item. Power Integrations regular terms and conditions apply.

Power Integrations Die Flow



R&QA Information 6

INDEX

Reliability and Quality Overview

Quality Pledge

"We at Power Integrations will be judged by our customers based on our ability to satisfy their needs."

"Only by diligently pursuing the highest standards of component quality, customer support, and on-time delivery can we succeed in satisfying and maintaining long-term relationships with our customers."

Dr. Edward C. Ross
President and CEO

Quality Goals

Many definitions of quality have been suggested in a attempt to provide a working meaning. To Power Integrations, quality is a broad subject which covers the entire process of design, manufacture and usage of our products. Quality is not, however, a vague concept. It is a set of measurable attributes that together define a product which will meet our customer's expectations.

Power Integrations is committed to continuous improvement of all aspects of quality. From design to sales, each area of the organization is involved in the achievement of a standard of zero defects. The attainment of quality goals is an integral part of planning for growth and is incorporated in decisions affecting capacity and resources.

Design

It is impossible to build quality products unless the design effort encompasses the principles of quality. Long before the first wafers are started in fab, quality is melded into the design of a new product. Product concepts are reviewed not only for cost and marketability, but also to guarantee that design specifications are within the capability of the manufacturing process. Each engineering group, design, process, manufacturing and customer support, reviews all product proposals before any physical design is initiated.

Design rules and process models ensure that each new design will meet the desired objectives. These rules are incorporated into the state-of-the art tools Power Integrations uses for all designs. In addition to facilitating the designer's efforts, these tools provide design verification through simulation and layout checks. Statistical analysis of wafer fab monitors complete a closed loop feedback of manufacturing providing continuous control of process variance.

Test Development

Concurrently with the design of a new product, test and manufacturing engineers begin development of test capability and production flows. These engineers work closely with the designers to make sure that critical device characteristics are testable, adding special circuitry if required to access internal nodes. Careful attention is paid to repeatability to limit the variability of test results.

Characterization

Once the first pieces of a new product complete manufacturing, they are thoroughly characterized beyond the expected operating conditions to confirm that the design specifications have been met. The measured performance is compared with the simulations and any variance is noted for investigation by engineering to refine the design rules and models.

Applications engineers test the working silicon in a variety of applications to complete the systems level characterization. This evaluation confirms that the new product is suitable for customer use. These results are reported back to the design, test development and process engineering groups to blend into the design rules and process specifications.

An additional area of evaluation is system fault response. The applications engineers check the new product's response to a set of system faults selected to stress the IC to worst case conditions. The information gained from these tests is used to enhance the reliability testing to guarantee failure rates.

The data gathered from these evaluations is distilled into the final device specifications. These limits are set to guarantee that process shifts will not impact product quality. Since some device attributes are impractical to test 100%, these parameters have 6 sigma limits. That is, the limits are double the natural process variance.

Manufacturing

The manufacturing process flow is designed to provide continuous control of product quality. Several checkpoints monitor the quality level after each major operation. In addition, Statistical Process Control (or SPC) is used extensively to create a tightly coupled production system.

Data from selected manufacturing operations is collected into networked databases and analyzed to identify situations requiring immediate reaction. These trends trigger corrective action before an out-of-control process can adversely affect product quality. Similarly, calibration data from the automatic test equipment is tracked to detect maintenance problems before they impact manufacturing operations.

Another important aspect of quality in manufacturing is the relationship established with vendors. Power Integrations works with each supplier of a critical part to create a cooperative environment which enhances the quality of incoming materials. Each new vendor is evaluated for capability, quality and price before approval.

Field Sales

The Sales organization is also an important contributor to the quality effort. They work with our customers to ensure that mutual expectations are communicated and understood. The field representatives relay the customers specifications into Power Integrations, where they are formally reviewed by each affected area. The Applications group also works with customer engineers to assist them in using our products.

Reliability

All products are required to complete a formal qualification program. Product qualification consists of a number of stress tests designed to accelerate potential failure mechanisms, ensuring that the product will meet acceptable maximum failure rates. All product and process changes must complete a similar test plan. These plans incorporate some or all of the listed tests as appropriate.

Regular audits ensure that the initial reliability levels are maintained. Also, when a new technology is first introduced, burn-in is used extensively to guarantee that reliability levels are acceptable.

Typical Qualification Tests

- HTRB @ 150°C
- THBT (85°C/85% RH)
- High Temperature Storage
- Power Cycle
- Temperature Cycle
- Thermal Shock
- X-Ray
- Autoclave (PST)
- Die Penetration
- Lead Integrity
- Mark Permanence

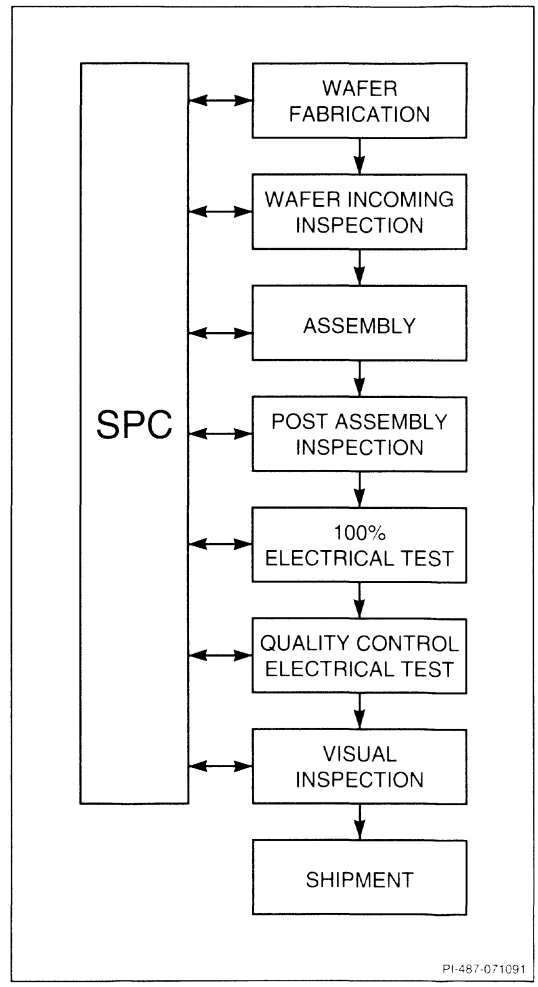


Figure 1. Power Integrations Product Flow.

Product Reliability Report March 1992

RR-92-1

POWER INTEGRATIONS, INC.®

Quality and Reliability Overview:

Power Integrations products are designed to be a cost effective combination of analog and digital control elements combined with high-voltage power devices. Specifically, the product offering includes a line of interface products and a family of off-line power supply control products. The logic and analog sections of these products are designed using standard 5 V, 3 micron CMOS technology. The high voltage device is an NMOS proprietary design technique derived from the conventional CMOS process.

It is Power Integrations' quality and reliability philosophy to ship each part in compliance with the data sheet. To accomplish data sheet compliance, Power Integrations uses a 100% final test screen at a temperature representative of data sheet ambient coupled with the product's typical operating conditions (30-40% of maximum rated power for interface products, 100% or maximum rated power for power supply products), or characterization and production results of six sigma distributions and guardbanding techniques.

For moisture and thermo-mechanical stress failures it is difficult to correlate to end use applications. For that reason moisture and thermo-mechanical stress releases are based on capability rather than on specific end use requirements.

IC Layout/Design Rules:

Power Integrations has fully characterized and modeled all critical parameters to the process extremes of our standard 3 micron CMOS process and the high-voltage NMOS output device. This information has been fully incorporated into a complete device library used to create our designs. All designs receive computer assisted design-rule checking and layout-versus-schematic checking prior to mask generation to assure consistency and quality.

Qualification Requirements Background:

Field failures follow a distribution of time commonly described by a "bathtub curve", as shown in Figure 1. That is, the lifecycle of a part can be divided into the three following regions.

1- Early Failure Rate (EFR): the equivalent of 6 months of continuous operation at a device junction temperature of 55°C.

2- Intrinsic Failure Rate (IFR): failures during the interval of time between 6 months and 20 years from residual defects that have not yet failed in the EFR period, fallout due to unpredictable system or environmental conditions, or premature wearout due to extreme process variability or use conditions.

3- Onset of Wearout (OSW): failures associated with the main population of product caused by such mechanisms as metal electro-migration, hot electron effects, wirebond intermetallics, or thermal fatigue on wirebonds.

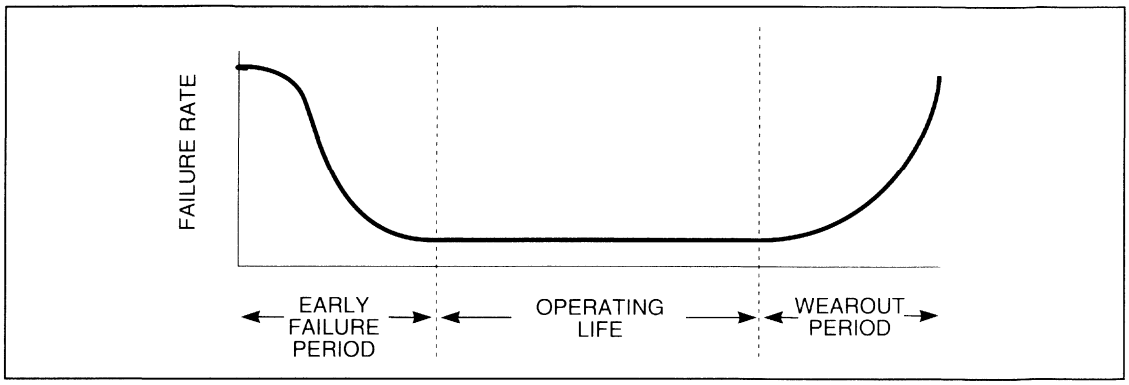


Figure 1. Typical MTBF Curve for Semiconductor Products.

Reliability Measurement Methods:

SHTL (Static High Temperature Life):	Applies a static DC bias to the device at an elevated temperature (also known as HTRB, high temperature reverse bias). This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive the contaminants to the silicon surface.
DHTL (Dynamic High Temperature Life):	Applies AC signals to control logic inputs at an elevated temperature (also known as op-life).
THBS (Temperature, Humidity, Biased Stress):	Normally performed at 85% RH and 85°C with minimum power dissipation and maximum voltage applied.
TMCL (Temperature Cycling- Air to Air):	Temperature extremes of -65°C to 150°C are good to test the overall package and die mechanical capabilities to induce any failures which may occur in a real application.
RTFB (Thermal Cycling):	To test the thermal shutdown feature, devices are forced to cycle in and out of thermal shutdown at approximately 2-second intervals.
ESD (Electrostatic Discharge):	Evaluates the ESD protection circuitry present on all inputs and is measured using MIL- STD 883 criteria, with both the human body model (1.5 kΩ/100 pF).
Latchup:	Measures the ruggedness of the CMOS structure in regard to reverse current flow that can be caused by the incorrect application of external voltages in real applications.

NOTE: Parametric Drift Analysis is performed over the length of the stress tests.

Reliability Data Summary:

Static High Temperature Life Test (STHL) @ 150°C

Device	Fab	Assembly Lot	Package	SS	24 hours Fail	24 hours Pass	168 hours Fail	168 hours Pass	500 hours Fail	500 hours Pass	1000 hours Fail	1000 hours Pass	2000 hours Fail	2000 hours Pass	Cummulative Fail	Cummulative Pass	Cummulative Hours	Note
SMP3	A	P90389	BDIP16	105	0	105	0	105	0	105	0	105			0	105	1000	
SMP3	A	P90401	BDIP16	132	0	132	0	132	0	132					0	132	500	
SMP3	A	P90403	BDIP16	45	0	45	0	45							0	45	240	
SMP3	A	P9E372	BDIP16	127	0	127	0	127	1	126	0	126	0	54	1	127	2000	A,B
SMP3	A	P9E391	BDIP16	101	0	101	0	101	0	101	0	101			0	101	1000	
SMP210	A	P90537	BDIP16	50	0	50	0	50	0	50					0	50	500	
SMP210	A	P90544	BDIP16	49	0	49	0	49	0	49	0	49			0	49	500	
SMP210	A	P90548	BDIP16	50	0	50	0	50	0	50	0	50			0	50	500	
SMP210	A	P90582	BDIP16	50	0	50	0	50	0	50	0	50			0	50	500	
SMP210	A	P90583	BDIP16	48	0	48	0	48	0	48					0	48	500	
SMP210	A	P90589	BDIP16	49	0	49	0	49	0	49					0	49	500	
SMP210	A	P90591	BDIP16	50	0	50	0	50	0	50					0	50	500	
SMP210	A	P90602	BDIP16	49	0	49	0	49	0	49					0	49	500	
SMP210	A	P90603	BDIP16	50	0	50	0	50	0	50					0	50	500	
SMP210	A	P90604	BDIP16	50	0	50	0	50	0	50					0	50	500	
SMP210	B	P9E628	BDIP16	110	1	109	0	109	0	109	0	109			1	109	500	C
SMP210	B	P90636	BDIP16	110	0	110	0	110	0	110					0	110	500	
SMP210	B	P9E659	BDIP16	107	0	107	0	107	0	107					0	109	336	
SMP210	B	P9E658	BDIP16	108	0	108	0	108	0	108					0	109	336	
		Totals		1440	1	1439	0	1439	1	1393	0	590	0	54	2	1442		
		Device Hours				$3.5 \cdot 10^4$		$2.1 \cdot 10^5$		$4.6 \cdot 10^5$		$3.0 \cdot 10^5$		$5.4 \cdot 10^4$		$1.1 \cdot 10^6$		

Notes: A: Sample reduced to 54 pieces at 1000 hours

B: Undervoltage threshold failure

C: BV_{DSS} failure at 24 hours

Temperature & Humidity Bias Stress (THBS) @ 85% RH/85°C

Device	Fab	Assembly Lot	Package	SS	24 hours Fail	24 hours Pass	168 hours Fail	168 hours Pass	500 hours Fail	500 hours Pass	1000 hours Fail	1000 hours Pass	2000 hours Fail	2000 hours Pass	Cummulative Fail	Cummulative Pass	Cummulative Hours	Note
DRV1	B	P9E427	PDIP8	45	0	45	0	45	0	45					0	45	500	
DRV1	B	P9E447	PDIP8	45	0	45	0	45	0	45					0	45	500	
DRV1	B	P9E458	PDIP8	45	0	45	0	45	0	45					0	45	500	
SMP3	A	P9E372	BDIP16	37	0	37	0	37	0	37	0	37			0	37	1000	
SMP3	A	P9E391	BDIP16	38	0	38	0	38	0	38	0	37			0	37	1000	A
SMP3	A	P9E398	BDIP16	43	0	43	1	42	0	42	0	42			1	42	1000	B
SMP210	B	P9E628	BDIP16	107	0	107	1	106	0	106					1	106	500	C
SMP210	B	P90636	BDIP16	77	0	77	0	77	0	77					0	77	500	
		Totals		437	0	437	2	435	0	435	0	116	0	0	2	434		
		Device Hours				$1.0 \cdot 10^4$		$6.3 \cdot 10^4$		$1.4 \cdot 10^5$		$5.8 \cdot 10^4$				$2.8 \cdot 10^5$		

Notes: A: 1 unit lost at 1000 hours

B: Internal Capacitor failure

C: Unit appeared to be damaged during electrical test at 24 hours

6

Reliability Data Summary (continued):

Dynamic High Temperature Life Test (150°C)

Device	Fab	Assembly Lot	Package	SS	24 hours Fail	24 hours Pass	168hours Fail	168hours Pass	500 hours Fail	500 hours Pass	1000 hours Fail	1000 hours Pass	2000 hours Fail	2000 hours Pass	Cummulative Fail	Cummulative Pass	Cummulative Hours	Note
DRV1	B	P9E429	PDIP8	105	0	105	0	105	0	105					0	105	500	
DRV1	B	P9E447	PDIP8	105	0	105	0	105	0	105					0	105	500	
DRV1	B	P9E457	PDIP8	105	0	105	0	105	0	105					0	105	500	
		Totals		315	0	315	0	315	0	315					0	315		
		Device Hours				$7.6 \cdot 10^3$		$4.5 \cdot 10^4$		$1.0 \cdot 10^5$						$1.0 \cdot 10^5$		

TMCL (-65 to 150°C)

Device	Fab	Assembly Lot	Package	SS	10 cycles Fail	10 cycles Pass	50 cycles Fail	50 cycles Pass	100 cycles Fail	100 cycles Pass	150 cycles Fail	150 cycles Pass		Cummulative Fail	Cummulative Pass	Cummulative Cycle	Notes
DRV1	B	P9E427	PDIP8	105	0	105	0	105	0	105				0	105	100	
DRV1	B	P9E443	PDIP8	105	0	105	0	105	0	105				0	105	100	
DRV1	B	P9E456	PDIP8	77	0	77	0	77	0	77				0	105	100	
SMP3	A	P9E391	BDIP16	77	0	77	0	77	0	77	0	77		0	77	150	
SMP210	B	P90636	BDIP16	77	0	77	0	77	0	77				0	77	100	
SMP210	A	P90609	SOIC20	77	0	77	0	77	0	77				0	77	100	
		Totals		518	0	518	0	518	0	518	0	77		0	546		
		Device Cycles				$5.2 \cdot 10^3$		$2.1 \cdot 10^4$		$2.6 \cdot 10^4$		$3.9 \cdot 10^3$			55650		

RTFB (95 to 150°C)

Device	Fab	Assembly Lot	Package	SS	24 hours Fail	24 hours Pass	168 hours Fail	168 hours Pass	500 hours Fail	500 hours Pass	1000 hours Fail	1000 hours Pass	2000 hours Fail	2000 hours Pass	Cummulative Fail	Cummulative Pass	Cummulative Hours	Note
SMP110	B	P90405	BDIP16	45	0	45	0	45	0	45	0	45			0	45	1000	
		Device Hours				$1.1 \cdot 10^3$		$6.5 \cdot 10^3$		$1.5 \cdot 10^4$		$2.3 \cdot 10^4$				45000		
		Thermal Cycles														$5.4 \cdot 10^7$		

Note: Thermal Cycles = approximate number of thermal cycles caused by internal protection circuitry

Reliability Data Summary (continued)

ESD

PRODUCT TYPE	ESD TEST RESULTS	
	HBM 1.5 kΩ/100 pF	CAP ONLY 100 pF
SMP3	>8000 V 700 V - V_{IN}	3000 V 300 V - V_{IN}
SMP210	>8000 V 700 V - V_{IN}	

LATCH-UP

PRODUCT	LATCH-UP CURRENT
SMP3	>250 mA
SMP210	>150 mA

Reliability Data Results

FITs Calculation

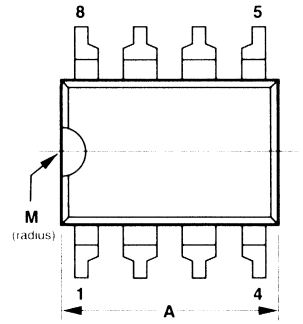
Failure Mechanism	Activation Energy (eV)	Acceleration Factor	Failures			Stress Failure Rate/Mhr		In Use Failure Rate	
			Actual	60% UCL	90% UCL	60% UCL	90% UCL	60% UCL	90% UCL
1 - Contamination	1.00	2816.7	0	0	0	0.0	0.0	$0.0 \cdot 10^{0}$	$0.0 \cdot 10^{0}$
2 - Mean Fail Mech.	0.55	79.0	2	3.11	5.32	3.0	5.0	$3.7 \cdot 10^{-8}$	$6.4 \cdot 10^{-8}$
3 - SiO_2 Defects	0.30	10.8	0	0	0	0.0	0.0	$0.0 \cdot 10^{0}$	$0.0 \cdot 10^{0}$
Total Device Hours			$1.1 \cdot 10^{6}$						
Cumulative Failure Rate								$3.7 \cdot 10^{-8}$	$6.4 \cdot 10^{-8}$
							FITs	37	64

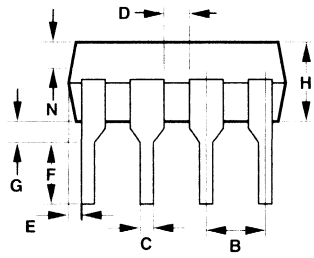
FITs = the number of failures that could be expected in 10^{9} hours of operation at 55°C ambient.

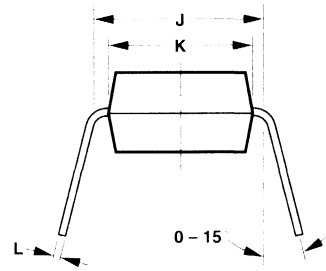
Package Outlines 7

INDEX

DIM	inches	mm
A	.395 MAX	10.033 MAX
B	.090-.110	2.286-2.794
C	.015-.021	.381-.533
D	.040 TYP	1.016 TYP
E	.010-.040	.254-1.016
F	.125 MIN	3.175 MIN
G	.020 MIN	.508 MIN
H	.125-.135	3.175-3.429
J	.300-.320	7.620-8.128
K	.245-.255	6.223-6.477
L	.009-.015	.229-.381
M	.030-.110	.762-2.794
N	.020 TYP	.508 TYP



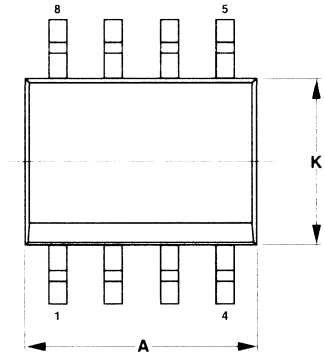


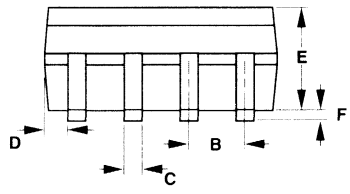


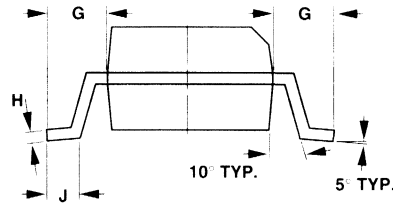
8-Pin Plastic DIP
PF Suffix

PO-001-071289

DIM	inches	mm
A	.188-.197	4.80-5.00
B	.050 TYP	1.27 TYP
C	.014-.018	.35-.45
D	.012 TYP	.305 TYP
E	.053-.069	1.35-1.75
F	.004-.008	.10-.20
G	.039-.043	1.00-1.10
H	.007-.010	0.19-0.25
J	.021-.045	.508-1.143
K	.150-.158	3.80-4.00





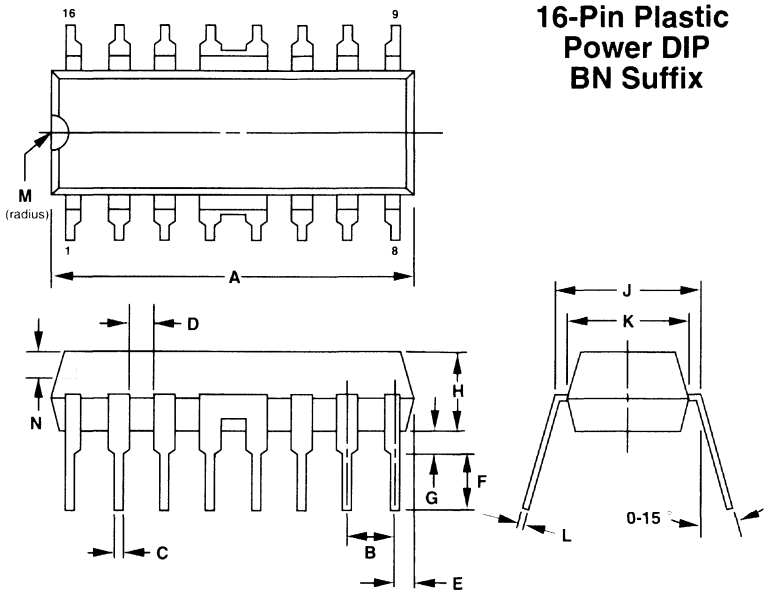


8-Pin Plastic SOIC
TF Suffix

PO-013-123191

7

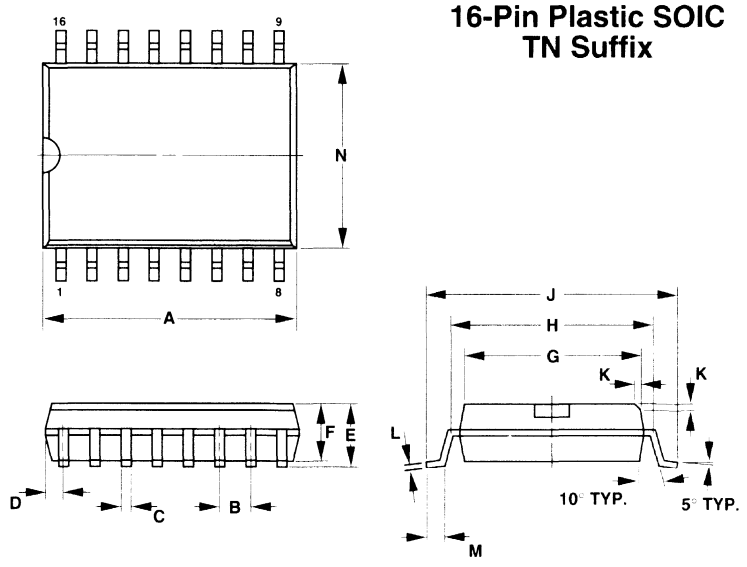
DIM	inches	mm
A	.780 MAX	19.812 MAX
B	.090-.110	2.286-2.794
C	.015-.021	.381-.533
D	.040 TYP	1.016 TYP
E	.010-.040	.254-1.016
F	.125 MIN	3.175 MIN
G	.020 MIN	.508 MIN
H	.125-.135	3.175-3.429
J	.300-.320	7.620-8.128
K	.245-.255	6.223-6.477
L	.009-.015	.229-.381
M	.030-.110	.762-2.794
N	.020 TYP	.508 TYP



16-Pin Plastic Power DIP BN Suffix

PO-002-111589

DIM	inches	mm
A	.405-.409	10.287-10.387
B	.048-.052	1.219-1.321
C	.014-.018	.356-.457
D	.027-.031	.686-.787
E	.99-.101	.2.514-2.565
F	.090-.094	2.286-2.388
G	.293-.297	7.442-7.544
H	.326-.330	8.280-8.382
J	.404-.408	10.262-10.363
K	.015 TYP	.381 TYP
L	.008-.012	.203-.305
M	.030-.034	.762-.864
N	.297-.301	7.544-7.645

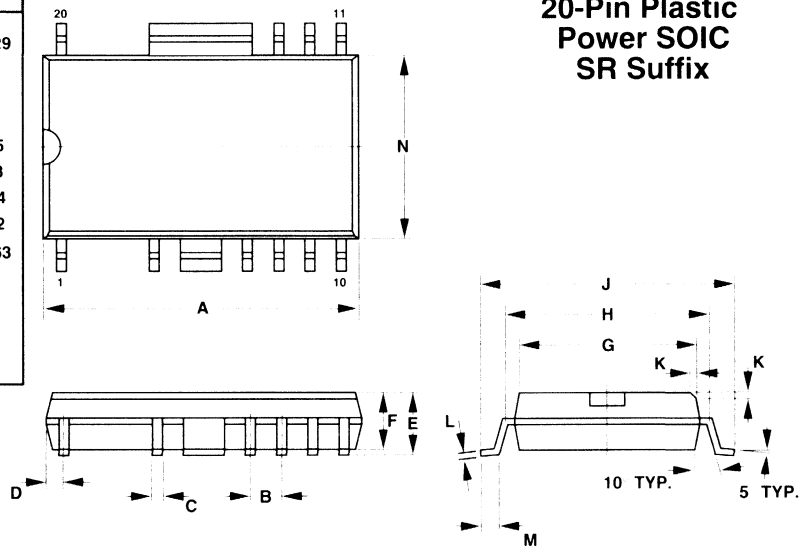


16-Pin Plastic SOIC TN Suffix

PO-010-022791

DIM	Inches	mm
A	.505-.509	12.827-12.929
B	.048-.052	1.219-1.321
C	.014-.018	.356-.457
D	.027-.031	.686-.787
E	.99-.101	.2.514-2.565
F	.090-.094	2.286-2.388
G	.293-.297	7.442-7.544
H	.326-.330	8.280-8.382
J	.404-.408	10.262-10.363
K	.015 TYP	.381 TYP
L	.008-.012	.203-.305
M	.030-.034	.762-.864
N	.297-.301	7.544-7.645

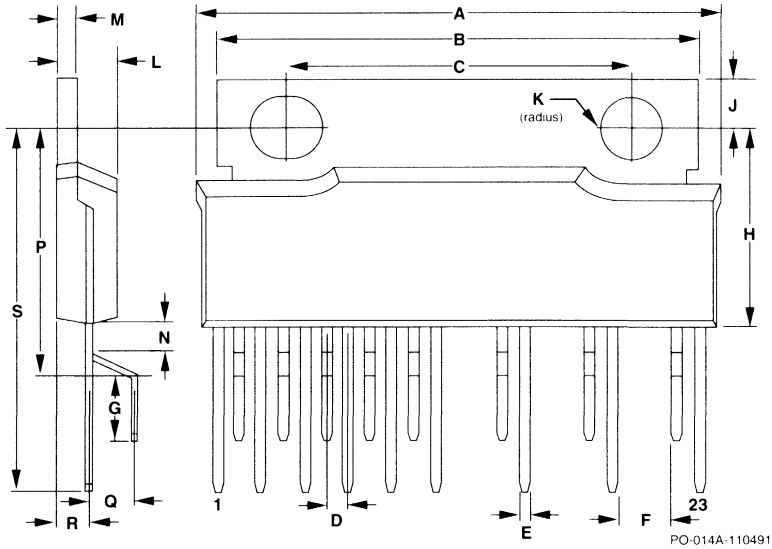
20-Pin Plastic Power SOIC SR Suffix



PO-012A-110191

DIM	Inches	mm
A	1.167-1.191	29.66-30.26
B	1.091-1.114	27.70-28.30
C	.779-.795	19.80-20.20
D	.05	1.27
E	.0197-.0295	0.50-0.75
F	.125-.128	3.18-3.24
G	.177 TYP	4.5 TYP
H	.435-455	11.05-11.55
J	.110 TYP	2.8 TYP
K	. 071 TYP	1.8 TYP
L	.126-.150	3.20-3.80
M	.041-.053	1.05-1.35
N	.041 TYP	1.03 TYP
P	.686 TYP	17.42 TYP
Q	.088-.112	2.24-2.84
R	.074-.077	1.88-1.96
S	.752 TYP	19.1 TYP

23-Pin Plastic SIP WT Suffix

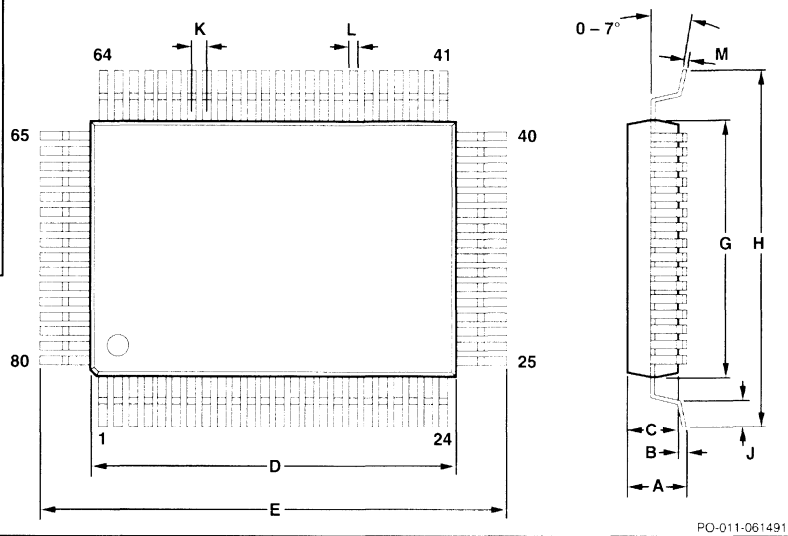


PO-014A-110491

7

DIM	inches	mm
A	.112-.128	2.85-3.25
B	.006-.016	.15-.41
C	.102-.110	2.60-2.80
D	.783-.791	19.90-20.10
E	.931-.951	23.65-24.15
G	.547-.555	13.90-14.10
H	.695-.715	17.65-18.15
J	.026-.037	.65-.95
K	.0315 BSC	.08 BSC
L	.012-.018	.30-.45
M	.006-.008	.15-.20

80-Pin Plastic QFP
EY Suffix



PO-011-061491

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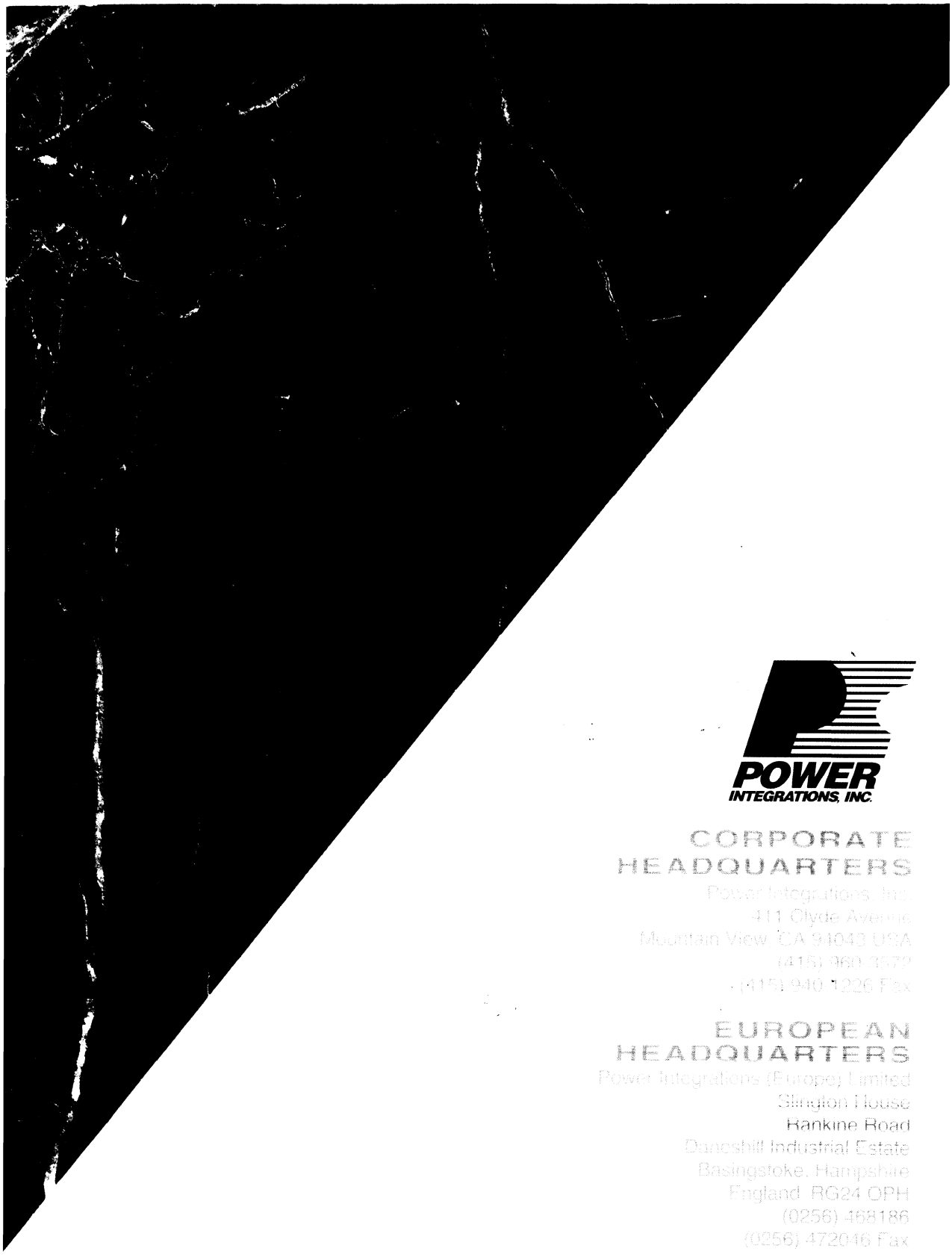

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